Compound Semiconductor Based Micro (Nano) - Electronics

*William E. Stanchina**

**Dept. of Electrical & Computer Engineering*

Swanson School of Engineering
University of Pittsburgh

wes25@pitt.edu; (412) 624-7629

Compound Semiconductor Microelectronics
-- a flash anecdotal history --

Origins: **1970's III-V Compound Semiconductor = Gallium Arsenide**

- **With high electron mobility, GaAs was projected to replace Si ICs for high speed digital applications → First GaAs digital IC reported in mid-70s showing potential for Gb/s data rates**
- **Analog (microwave) technology and applications developed in parallel**

End of processor type digital GaAs in late 1980's → Consumed too much power, wasn't scaling to high enough level of integration with acceptable yield, too expensive. The Si world simply out-ran and/or engineered away every challenge.

III-V RF and analog technology continued to develop and markets developed (e.g. cell phone technology required GaAs PAs) as the defense market declined in the early 1990's. New semiconductors gained prominence through the 90's: e.g. InP for optoelectronics such as 10/40 Gbps optical communication systems, GaN offered potential for 10X improvement over GaAs for μ-wave power applications.

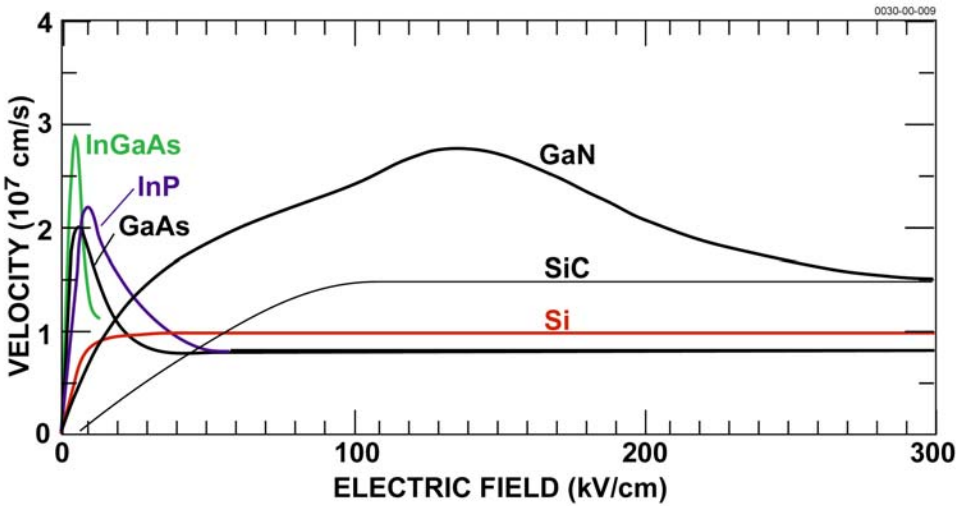
In the 2000's, GaN technology made significant improvements and gained application while other new compounds (e.g. InAs, InSb,…) gained interest and research for higher speed and lower power applications

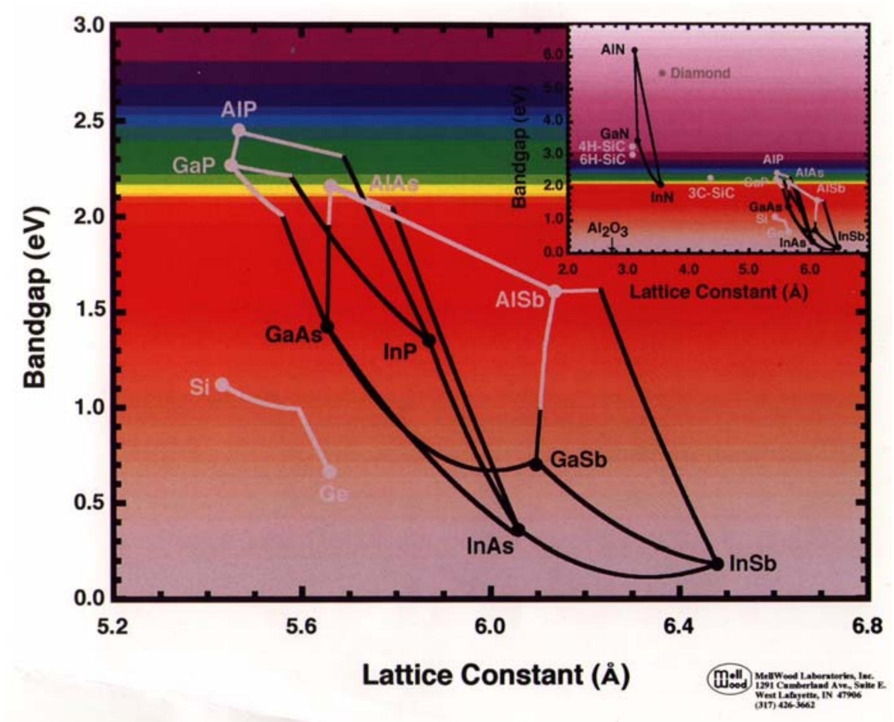
Last few years → "Beyond Si" now includes III-V again as a candidate for digital

Department of Electrical & Computer Engineering

Over 40 years of research has uncovered that Compound Semiconductors possess some uniquely useful properties

Compound semiconductors exhibit the highest peak electron velocities: Important for high operating frequency devices



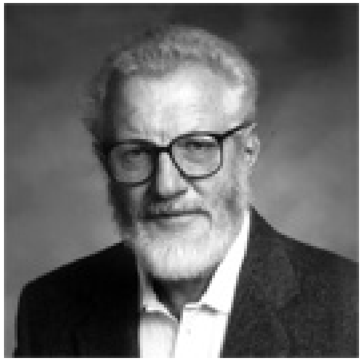


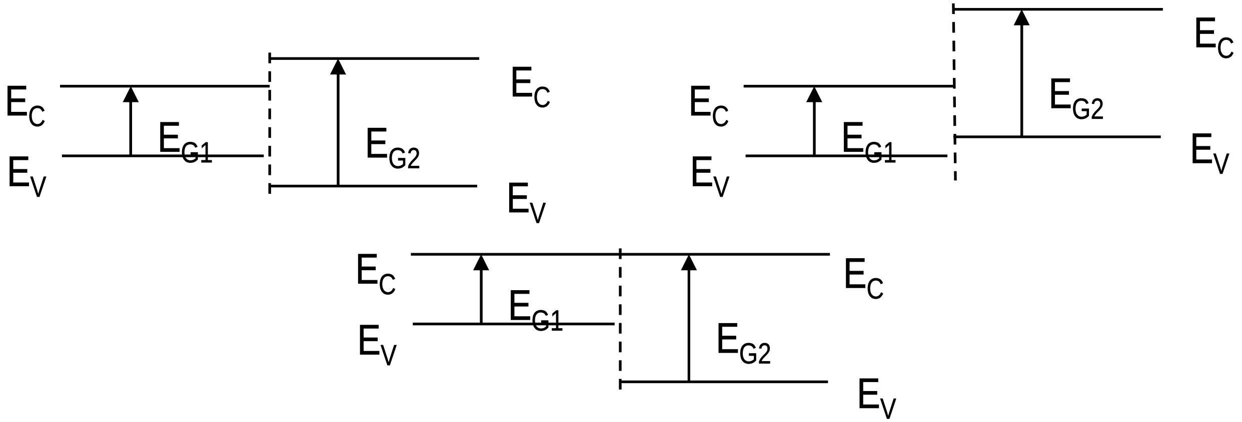
Identification of lattice-matched ternary and quaternary compounds and reproducible and controllable ways to grow them has led to even better material transport properties and the ability to detect/emit photonic wavelengths from UV through IR

W.E. Stanchina
wes25@pitt.edu

Semiconductor Bandgap Engineering opened a new world of III-V device prospects

Prof. Herb Kroemer (ECE Dept. – U. of California at Santa Barbara) -- 2000 Nobel Prize in Physics "for developing semiconductor heterostructures used in high-speed- and opto-electronics"



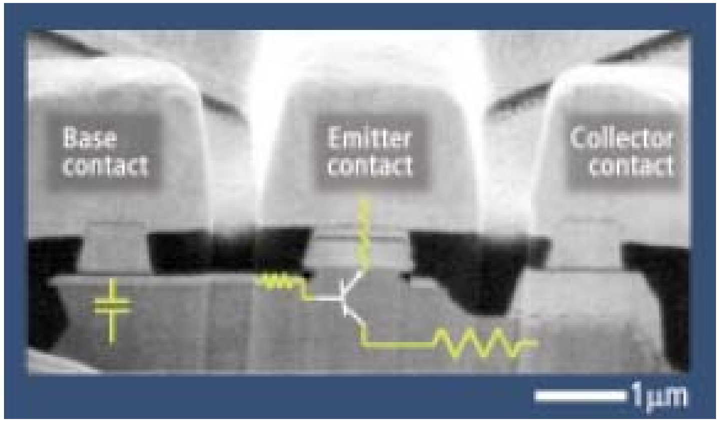


Many possible choices of differing semiconductor bandgaps and band edge alignments has led to a variety of useful new "bandgap engineered" devices and quantum well devices with the most prominent to date being:

- **Heterojunction Bipolar Transistors**
- **Heterojunction Field Effect Transistors (HFETs, HEMTs, MODFETs, …)**

W.E. Stanchina
wes25@pitt.edu

e.g. State-of-the-Art III-V HBTs have utilized a variety of semiconductors



GaAs - Based HBTs

Emit.	AlGaAs	GaInP
Base	GaAs	GaAs
Coll.	GaAs	GaAs

InP - Based npn HBTs

(grown by MBE & GSMBE; Be & C acceptor dopants)

AlInAs	InP	**Emit.**	AlInAs	InP	InP
GaInAs	GaInAs	**Base**	GaInAs	GaInAs	GaAsSb
GaInAs	GaInAs	**Coll.**	InP	InP	InP

SHBTs **DHBTs**

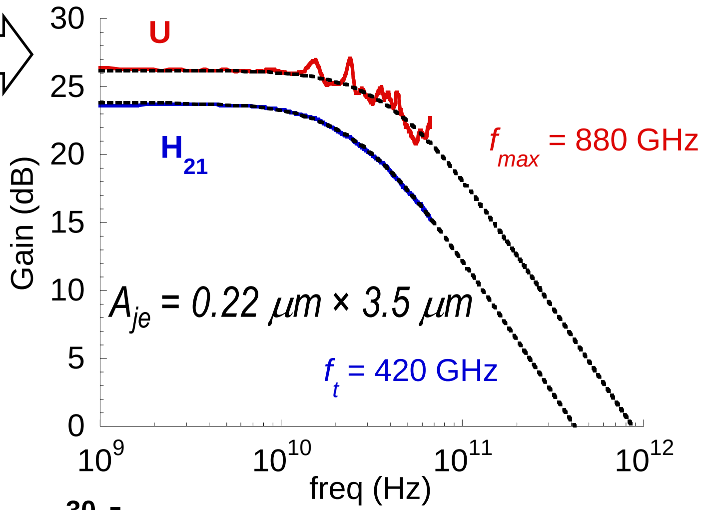
W.E. Stanchina
wes25@pitt.edu

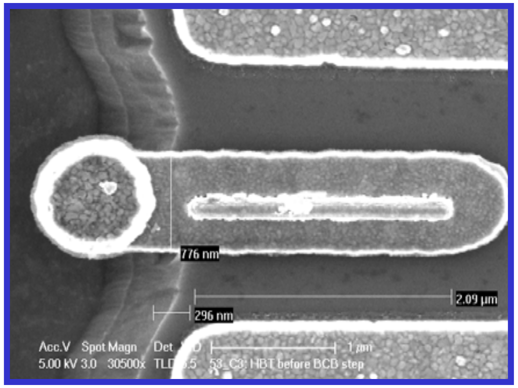
In recent years…..
III-V HBTs advanced by scaling and materials and process innovation

Courtesy of : Prof. Mark Rodwell et al, 2010 Device Research Conference 6/21/2010

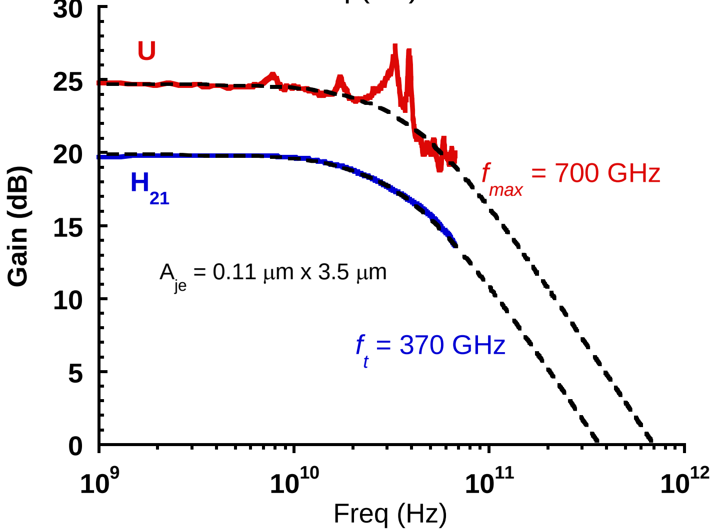
Closest agreement with scaling rules

emitter	512	256	128	64	32 nm width
	16	8	4	2	1 Ω·µm² access ρ
base	300	175	120	60	30 nm contact width,
	20	10	5	2.5	1.25 Ω·µm² contact ρ
collector	150	106	75	53	37.5 nm thick,
	4.5	9	18	36	72 mA/µm² current density
	4.9	4	3.3	2.75	2-2.5 V, breakdown
f_τ	370	520	730	1000	1400 GHz
f_{max}	490	850	1300	2000	2800 GHz



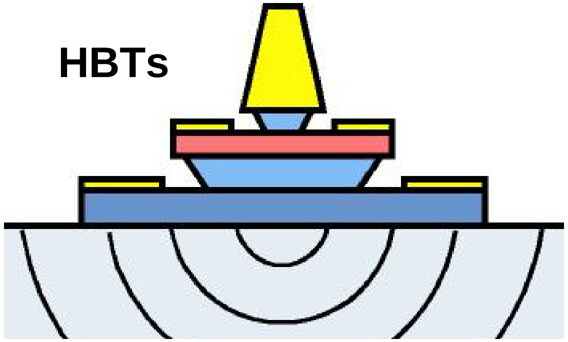


Refractory Contact HBT Process



III-V Fabrication Processes Must Change... Greatly

Courtesy of : Prof. Mark Rodwell et al, 2010 Device Research Conference 6/21/2010

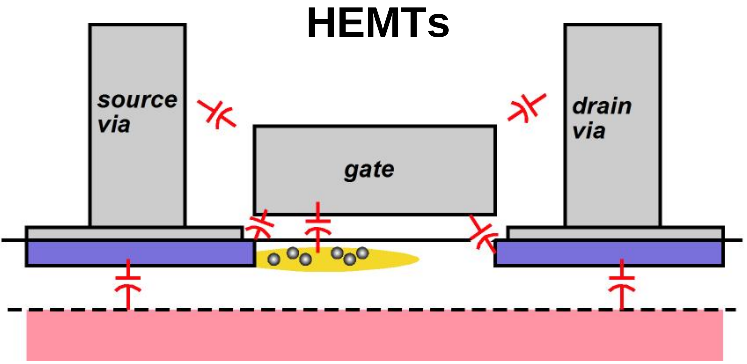


32 nm base & emitter contacts...self-aligned

32 nm emitter junctions

1 Ω–μm^2 contact resistivities

70 mA/μm^2 → refractory contacts



high-K dielectric replaces heterojunction

15 nm gate length

15 nm source / drain contacts...self-aligned

< 10 nm source / drain spacers (sidewalls)

1/2 Ω–μm^2 contact resistivities

3 mA/μm → 200 mA/μm^2
contacts above ~ 5 nm N+ layer
→ refractory contacts !

High-Current L & Γ-L FETs

Courtesy of : Prof. Mark Rodwell et al, 2010 Device Research Conference 6/21/2010

III-V channels; standard Γ-valley transport:

- *low m*→ high velocities→ increases current* ☺
- *low m*→ low channel charge → decreases current* ☹
- *density-of-states bottleneck: for small EOT, Si beats III-V's* ☹ *(Solomon & Laux IEDM 2001)*

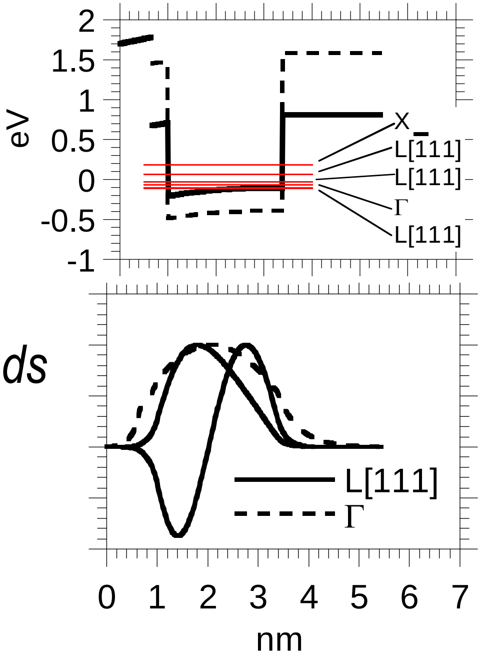
Use the L valleys to increase the III-V channel density of states

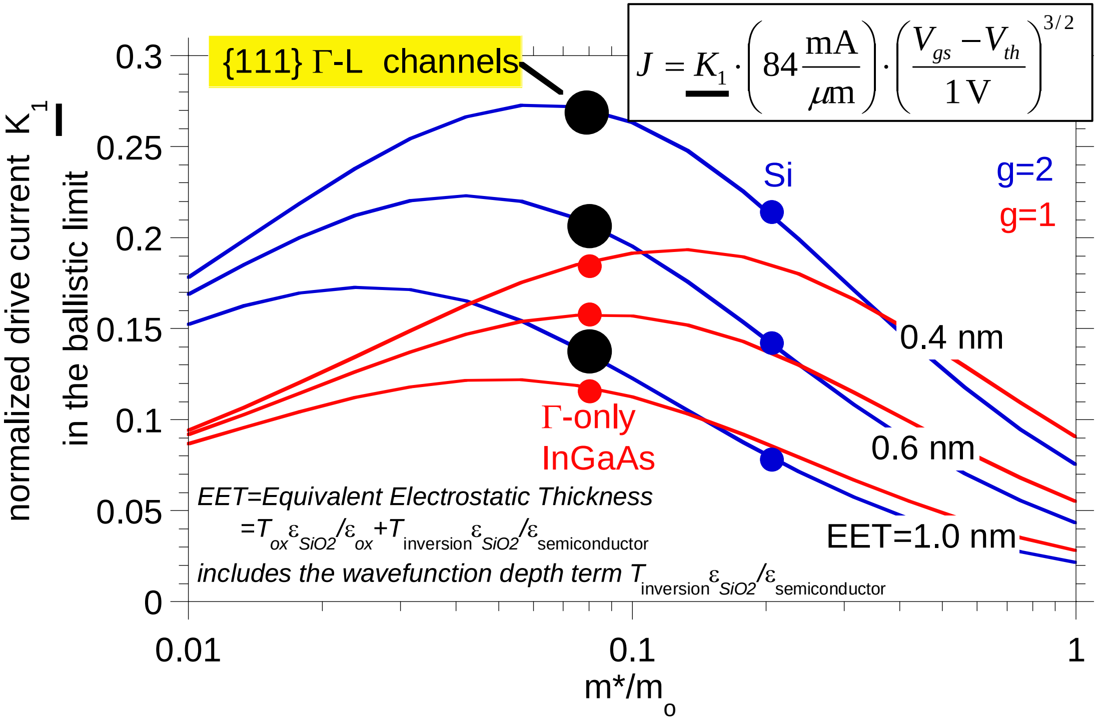
- *{111} or {110}*
- *low transport mass → high* $v_{carrier}$
- *multiple or anistropic valleys → high DOS*
- *→ high current densities* ☺

Example:

{111}-oriented GaAs channel 2 nm thick

*3 occupied bands all with low m**





$$J = \underline{K_1} \cdot \left(84 \frac{\text{mA}}{\mu\text{m}}\right) \cdot \left(\frac{V_{gs}-V_{th}}{1\,\text{V}}\right)^{3/2}$$

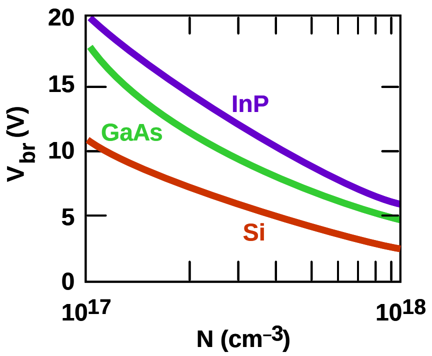
EET=Equivalent Electrostatic Thickness $=T_{ox}\varepsilon_{SiO2}/\varepsilon_{ox}+T_{inversion}\varepsilon_{SiO2}/\varepsilon_{semiconductor}$

includes the wavefunction depth term $T_{inversion}\varepsilon_{SiO2}/\varepsilon_{semiconductor}$

III-V Technology Development: Scaling from micro to nano

The last couple charts have been indicative of the direction of progress in most III-V compound semiconductors – i.e. scale to smaller dimensions to achieve higher frequency performance and/or lower power consumption.

- **1 THz (f_{max}) InGaAs PHEMT on InP (L_g=50 nm, 10 nm thick channel → to maximize channel current and minimize parasitics): g_m = 1.7 S/mm; – Teledyne Scientific**
- **Smallest L_g reported at 20 nm by Fraunhofer IAF (A. Tessman et al., <u>Compound Semiconductor</u>, Oct. 2010, pp.21-24); mHEMT with f_T = 515 GHz where Lg=35 nm used in MMICs that demonstrated 16 dB gain at 460 GHz**
- **GaN HFET on SiC subs. with L_g = 40 nm → f_T = 440 GHz, f_{max} = 220 GHz – HRL Laboratories, LLC**



	Si	GaAs	GaN
Bandgap (eV)	1.1	1.4	3.4
Bradkdown Fld (10^5 V/cm)	2	4	30
Max. Velocity (10^7 cm/s)	1	2	3

*

Here's the appeal of GaN

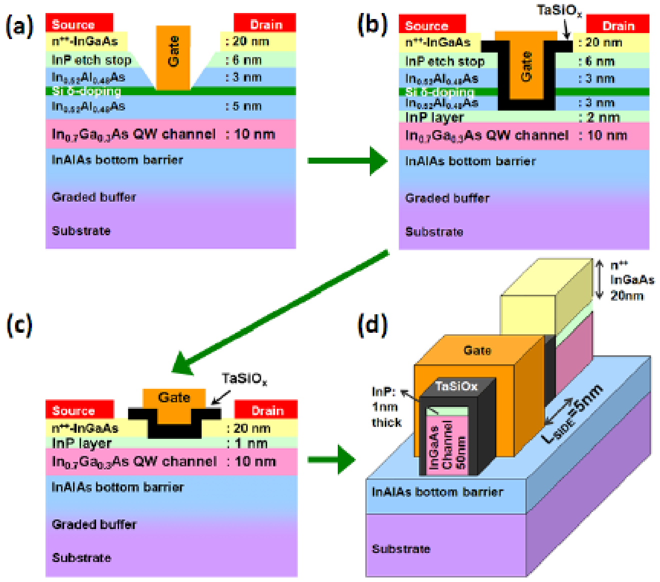
- **"IEDM to Showcase Record-Breaking III-Vs," <u>Compound Semiconductor</u> (October 2010, p6) at www.compoundsemiconductor.net**

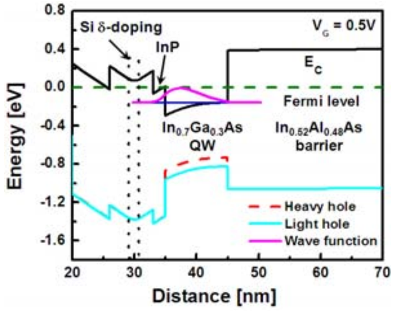
*** Binari, S.C. and Deitrich, H.B., "III-V Nitride Electronic Devices (Chp 12)," <u>GaN and Related Materials</u>, S.P. Pearton (Ed.), Vol 2 of Series: Optoelectronic Properties of Semiconductors and Superlattices – M.O. Manasreh (Ed.), Gordon and Breach Science Publishers, 1997.**

W.E. Stanchina
wes25@pitt.edu

A more recent trend:
III-V Transistor Materials and Bandgap Engineering are being explored within the Si Infrastructure

InGaAs QWFET (Intel and IQE)





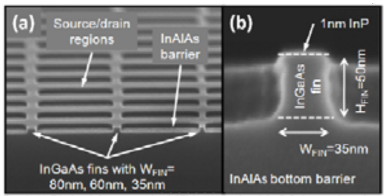


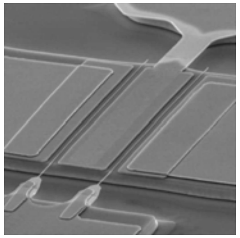
Fig. 6: (a) Tilted and (b) cross-sectional SEM micrographs of the InGaAs non-planar device structures after fin formation. In this work three different fin widths (W_{FIN}) are used as shown in (a): 80nm, 60nm and 35nm. Fig. 6(b) shows an InGaAs fin structure with W_{FIN}=35nm and fin height (H_{FIN}) =50nm.

Ref: http://download.intel.com/technology/silicon/IEDM-2010-paper-III-V-non-planar.pdf
M. Radosavljevic, G. Dewey, J. M. Fastenau*, J. Kavalieros, R. Kotlyar, B. Chu-Kung, W. K. Liu*, D. Lubyshev*, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, and Robert Chau, "Non-Planar, Multi-Gate InGaAs Quantum Well Field Effect Transistors with High-K Gate Dielectric and Ultra-Scaled Gate-to-Drain/Gate-to-Source Separation for Low Power Logic Applications," presented at 2010 IEDM

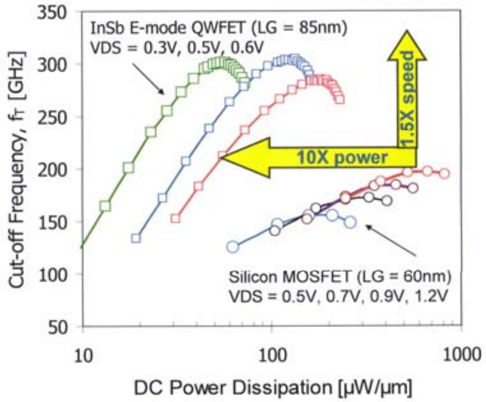
InSb QWFET (Intel and QineteQ)

Relative electron mobilities of semiconductors

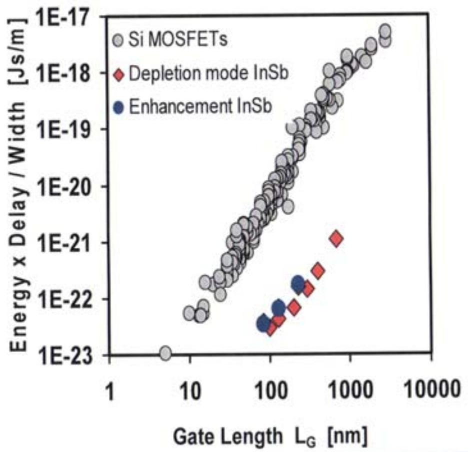
Si	GaAs	InAs	InSb
1	8	33	50



2 Gate finger InSb QW FET grown on SI GaAs substrate



Ref:
http://download.intel.com/technology/silicon/InSb_IEDM_presentation.pdf
S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, "Enhancement and Depletion mode InSb Quantum Well Transistors for High Speed and Low Power Logic Applications," 2005 Intern. Electron Devices Meeting,
presented at 2005 IEDM



W.E. Stanchina, wes25@pitt.edu

Another more recent trend:
Growth of III-V Nano-structures for Electronic Devices

InP nanowire / Si hetero-diode*

Philips Res. Lab and Delft Nano Inst. of Tech.

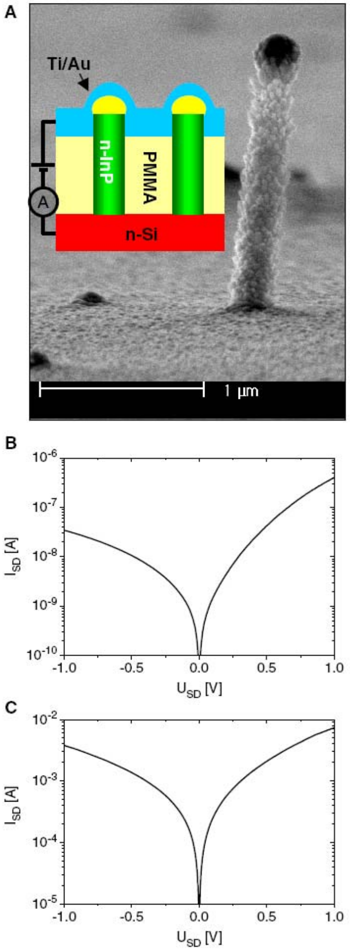


Figure 6. (a) SEM image of an n-InP wire protruding from the PMMA layer that has been electrically contacted with a Ti/Al metal stack. (b) I–V characteristic of p-InP nanowires grown on a highly p-doped Si substrate and (c) n-InP nanowires on a highly n-doped Si substrate.

*Ref: A.L. Roest et al. "Position controlled epitaxlai III-V nanowires on Si," **Nanotechnology 17** (2006), S271-S275; doi:10.1088/0957-4488/17/11/S07

Vertical Wrap-Gated Nanowire Transistors**

Lund Univ. and Chalmers Univ. of Tech.

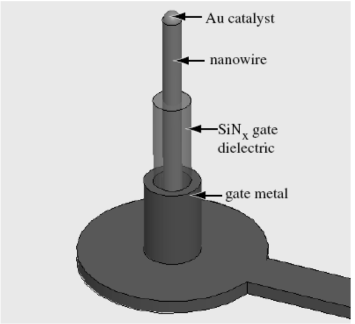


Figure 2. Schematic layout of the transistor. The gate wraps around the base of the wire, and is isolated from the nanowire by a layer of SiN_x. Only one wire is shown in the schematic diagram, while a matrix of wires is used in our actual devices.

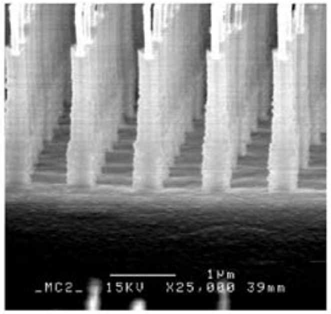


Figure 4. The nanowire channels after the gate is formed and a protective layer of SiN_x has been deposited. The protective SiN_x layer has been etched away from the uppermost part of the wires to allow for drain contact formation.

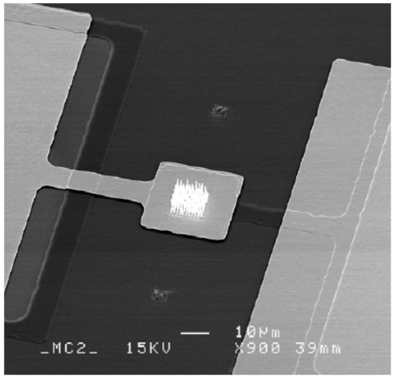


Figure 6. SEM image of the completed device showing the gate and drain fingers and the nanowire channels.

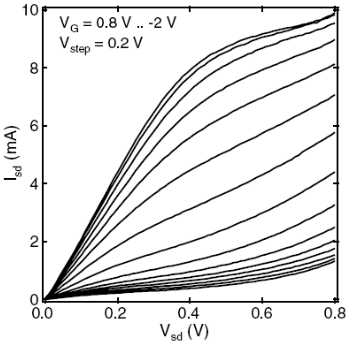


Figure 8. I–V characteristics of a transistor with ∼120 nanowire channels. The measurement is done in the common source configuration with the substrate acting as the source. The curves are recorded in one sweep from positive to negative gate voltage to avoid the hysteresis that is otherwise present.

Can each nanowire be fabricated into a single transistor and all interconnected into ICs?

** Ref: T. Bryllert al. "Vertical Wrap-Gated Nanowire Transistors," **Nanotechnology 17** (2006), S227-S230; doi:10.1088/0957-4488/17/11/S01

W.E. Stanchina
wes25@pitt.edu

A Summary of the Material Presented and some Other Interesting Developments

What we've seen:

1. ***Scaling of dimensions to 10's of nm along with development of new materials for contacts, dielectrics, etc. along with new processes for III-V HBTs and HFETs. There are a variety of III-V heterostructure material choices and variations in device physics employed.***

2. **Incorporation of III-V materials synergistically with Si for higher speed n-channel and p-channel MOSFETs (i.e. getting the III-V on the Si)…..recent new reports**
    - **InGaAs MOSFET (with 3.5 nm channel) on S.I. substrate and wafer bonded to Si; good on/off characteristics (~107) – University of Tokyo [ref: "IEDM to Showcase Record-Breaking III-Vs," Compound Semiconductor (October 2010, p6) at www.compoundsemiconductor.net**
    - **Compound semiconductor-on-insulator ("XOI") transistors – InAs nanoribbons (10 nm long x 18 nm high x 300 nm wide) removed from GaSb donor (growth substrate) and "stamped" onto a Si/SiO2 receiver substrate. InAs XOI FETs showed peak transconductance of ~1.6 mS/μm and on/off ~10,000. – UC Berkeley, Lawrence Berkeley Natl Lab, National Tsing Hua Univ., Univ. of New Mexico, and Ulsan Natl. Inst. of Sci. & Tech. [ref: K. Hyunhyub et al. "Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors," Nature, Vol.468 (Nov. 2010), pp. 286-289; doi: 10.1038/nature09541]**

3. **Growth of III-V nanostructures (wires …) and research into nano device development**

    -- How to make single nanotransistors and interconnect into useable circuits??

> > > > > > > > > > > > >

A couple of other intriguing recent III-V developments to ponder:

(i) GaMnAs that exhibits "spin-Seebeck" effect (or combination of thermo-electricity and spintronics)

-- [reported by J. Heremans and R. Myers at Ohio State Univ. and reported in Nature Materials; summary found at www.compoundsemiconductor.net October 2010]

(ii) AlGaAs/InGaAs QW structure forming a "Transistor Laser" → produces an electrical output and optical laser output with an electrical input. [ref: H.W. Then et al., J. Appl. Phys. 107, 094509 (2010) and M. Feng, "The Transistor Laser: a radical, revolutionary device," www.compoundsemiconductor.net, Nov/Dec 2010]

W.E. Stanchina
wes25@pitt.edu

Questions?

Discussion