

Session 4 - Si-based Nanoelectronics (I)

The following points were discussed:

➔ Traditional scaling

- Scaling is a reality: 90nm ➔ 45 nm ➔ 22nm
- Lithography as a key enabler: From 65-32nm: 193nm laser line, below: EUV

➔ Equivalent scaling (MOSFET): Challenge of the introduction of new concepts

- Increase of mobility by strain
- Increase of C_{ox} ➔ low EOT ➔ high k materials
- Scaling down of L_g (lithography), result: short channel effects ➔ Need for new transistor architectures

➔ Memory: what drives the technology

- Integration density (use of 3rd dimension)
- Consumption (read/write: speed, stand-by: non-volatility)
- Correction of a defective information storage

Si-based Nanoelectronics (II)

➔ The “universal” memory

- Dense (DRAM)
- Fast (SRAM)
- Non-volatile (NAND, NOR)
- Scalable
- Low power
- Reliable

Future potential candidates: Charge trapping devices (flash, FeRAM), Resistive devices (PCRAM, MRAM, RRAM...)

➔ Interconnects: a major challenge

- No technological breakthrough is expected in the short term
- Find design and manufacturing solutions

➔ Physical limits

- Present CMOS – limits at the atom scale
- Other ideas on how to process information should emerge
- No visible alternative technology at present

(RTD- '80s: never achieved high complexity circuits, SETs - '90s: Convincing demonstration₂ only on special devices of low complexity)

Si-based Nanoelectronics (III)

➔ Economical challenge

- Monthly sales are reduced
- Evolution of product diversity
- Each company has its own priorities

➔ Design – technology interaction: Wishful thinking or real need?

- Problem of variability with scaling down
- Circuits are more sensitive to technology
- Design-technology interaction is a must

➔ More than Moore: the next frontier?

- MtM vs. MM market share ~20%
- A wide diversity of products. No established CMOS-like legacy process/device
- Roadmapping? Effort started (in ITRS and in Catrene). Led by Societal needs, Lead markets, Applications