Analog/Mixed-Signal (AMS) Design

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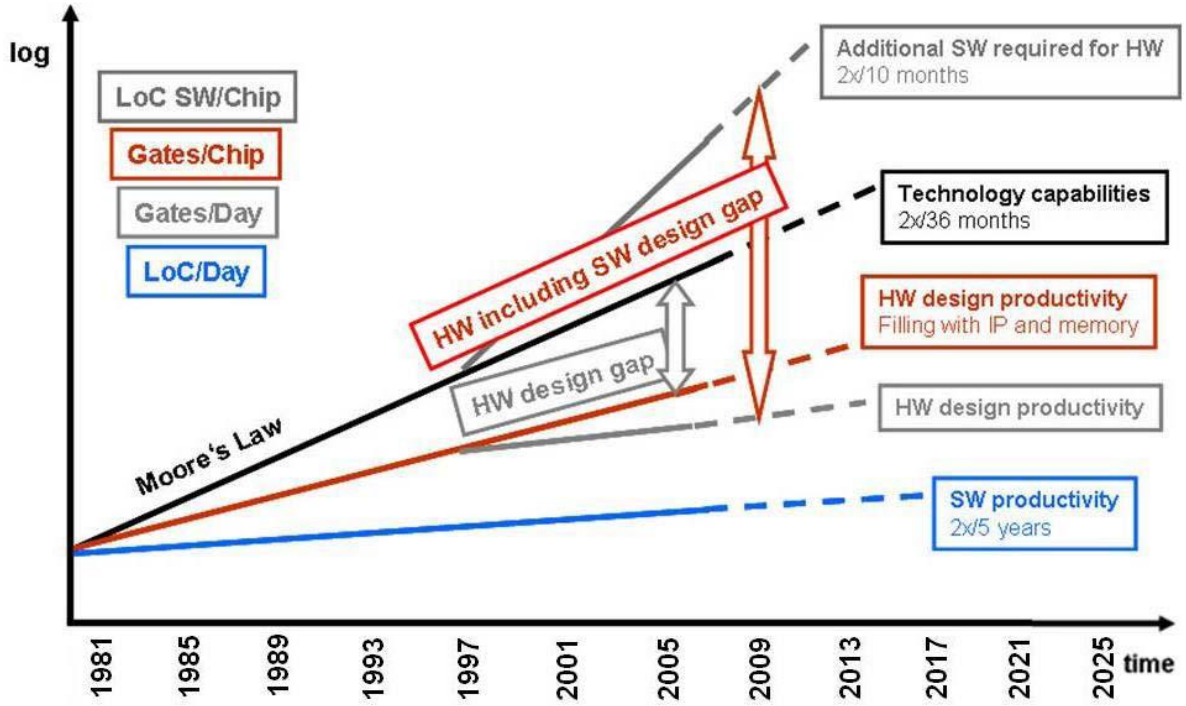
Overview

- Introduction
- From device to circuit
- Models, simulation, design
- Variability (manufacture, operation)
- Reliability (aging)
- ITRS analog/mixed-signal design technology trends
- Conclusion

Microelectronics – Progress



Source: International Technology Roadmap for Semiconductors 2009

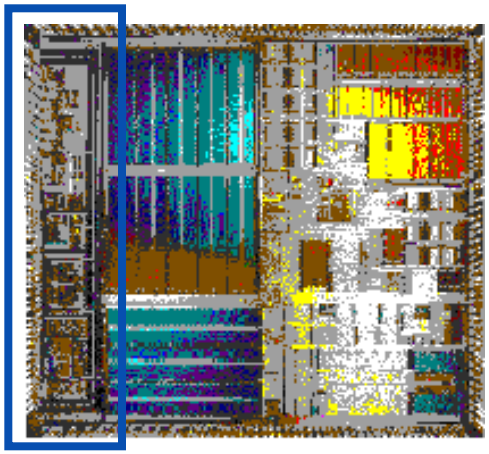
- Progress in design technology necessary: electronic design automation (EDA)
  - Transform technological progress of ever smaller devices into products
  - Time to market
  - Design quality

Progress based on

- Process technology
  - Ever smaller devices
  - High production yield
  - High reliability (lifetime of chip)
- System heterogeneity
  - System on Chip (SoC): memory (RAM), processor (CPU), application-specific integrated circuit (ASIC), digital signal processors (DSP), interface (I/O), bus
  - Analog, digital, RF, hardware, software, MEMS
- Design technology
  - Complex component libraries (bottom-up)
  - System synthesis (top-down)

Analog/Mixed-Signal (AMS) Circuits

AMS

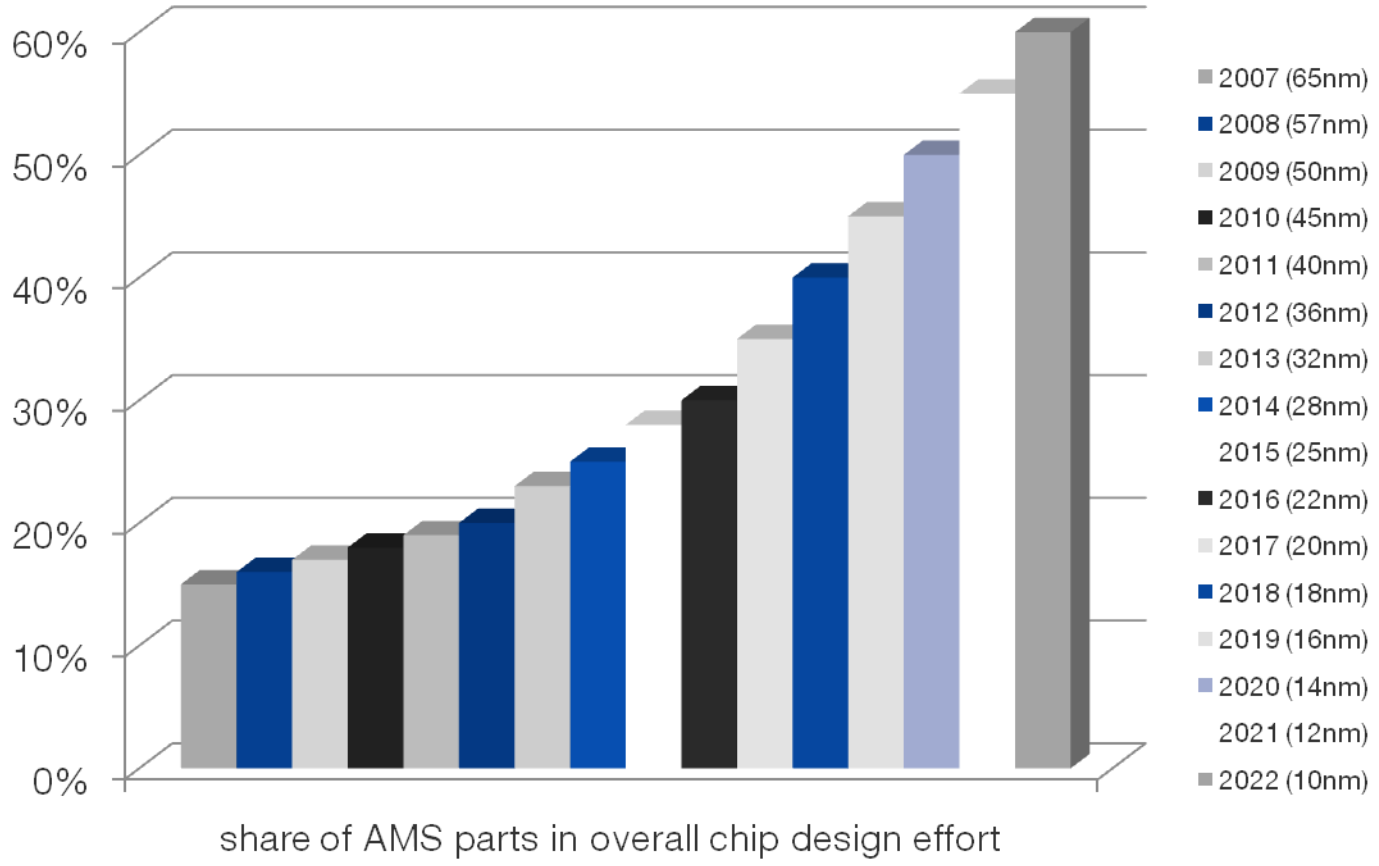


GSM base band chip “E-Gold+”
Infineon Technologies AG
(1990ies)

AMS:
on 75% of ICs
20% of chip area
40% of design effort
50% of redesigns

(EDA Weekly, 21 March 2005)

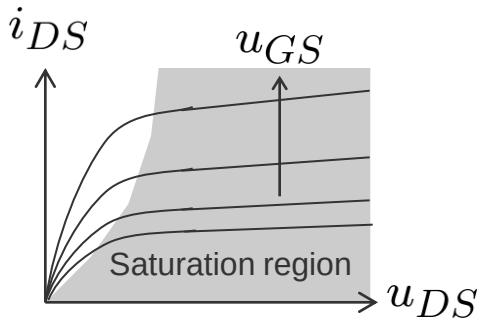
Analog/Mixed-Signal (AMS) Circuits

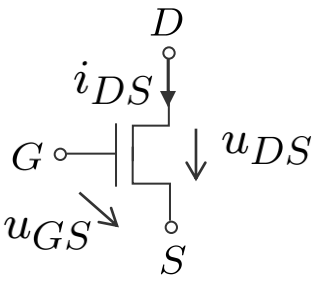


International Roadmap for Semiconductors 2007
http://www.itrs.net/Links/2007ITRS/2007_Chapters/2007_Design.pdf

From Device To Circuit

MOS Transistor („Device“)





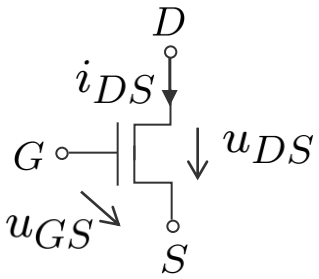
works as voltage-controlled current source …

$$i_{DS} = K \cdot \frac{W}{L} \cdot (u_{GS} - U_{th})^2 \cdot (1 + \lambda \cdot u_{DS})$$

… if

$$u_{DS} - (u_{GS} - U_{th}) \geq U_{satmin}$$
$$u_{GS} - U_{th} \geq 0$$
$$u_{DS} \geq 0$$

MOS Transistor



Manufacturing-induced variation in i_{DS} …

$$\frac{\sigma^2_{iDS}}{i^2_{DS}} = \frac{A_K}{W \cdot L} + \frac{\sigma^2_W}{W^2} + \frac{\sigma^2_L}{L^2} + \frac{4}{(u_{GS} - U_{th})^2} \cdot \frac{A_{Uth}}{W \cdot L}$$

… is small if

$$W \cdot L \geq A_{minA}$$
$$W \geq W_{minA}$$
$$L \geq L_{minA}$$

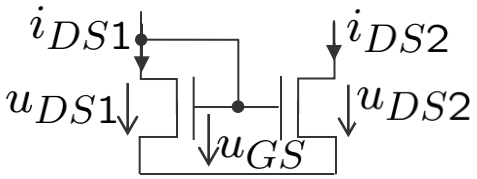
$$\sigma^2_{iDS} = \sum_{\mu \in \{K,W,L,U_{th}\}} \left(\frac{\partial i_{DS}}{\partial \mu}\right)^2 \cdot \sigma^2_\mu$$

(K, W, L, U_{th} uncorrelated)

$$\left(\frac{\sigma_K}{K}\right)^2 = \frac{A_K}{W \cdot L}, \quad \sigma^2_{Uth} = \frac{A_{Uth}}{W \cdot L}$$

[Lakshmikumar et al. IEEE JSSC 1986]

Current mirror



$$\frac{i_{DS2}}{i_{DS1}} = \frac{W_2/L_2 \cdot (u_{GS} - U_{th2})^2 \cdot (1 + \lambda \cdot u_{DS2})}{W_1/L_1 \cdot (u_{GS} - U_{th1})^2 \cdot (1 + \lambda \cdot u_{DS1})} \stackrel{!}{=} q$$

provides a fixed ratio between two drain-source currents …

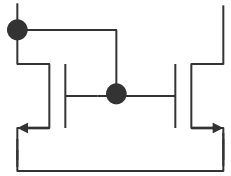
… if

$$|u_{GS} - U_{th1/2}| \geq U_{GSmin}$$

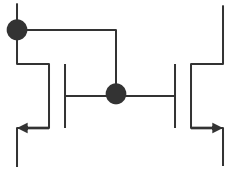
$$|u_{DS2} - u_{DS1}| \leq \Delta U_{DSmax}$$

MOS Transistor Pairs

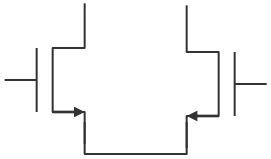
- 203 alternatives
- 8 of which have a design relevant function



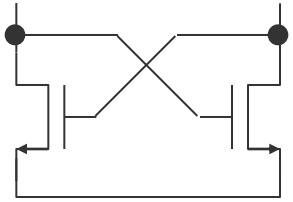
2-transistor current mirror



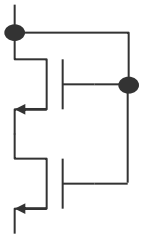
level shifter



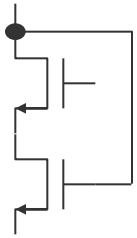
differential pair



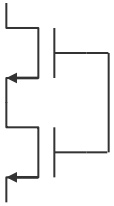
cross pair



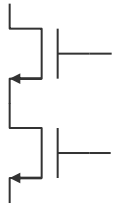
voltage reference 1



voltage reference 2

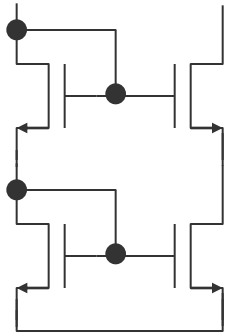


current mirror load

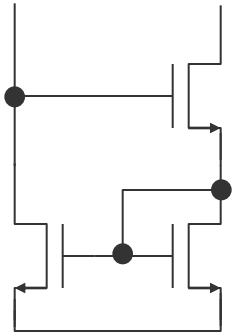


cascode pair

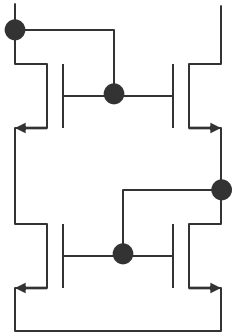
MOS Transistor Groups



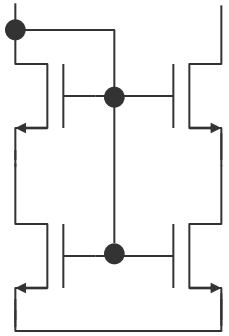
cascode current mirror (CM)



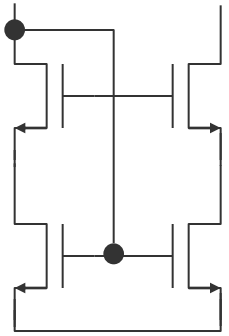
Wilson CM



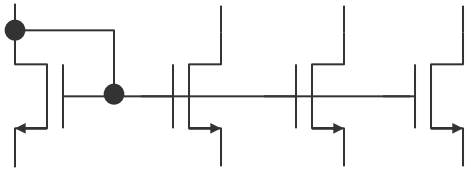
Wilson CM 2



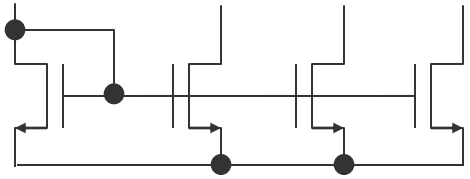
4-transistor CM



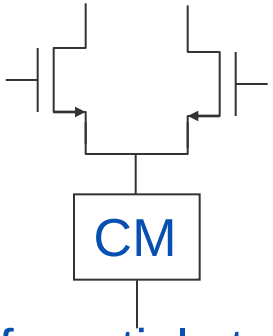
wide-swing cascode CM



level shifter bank

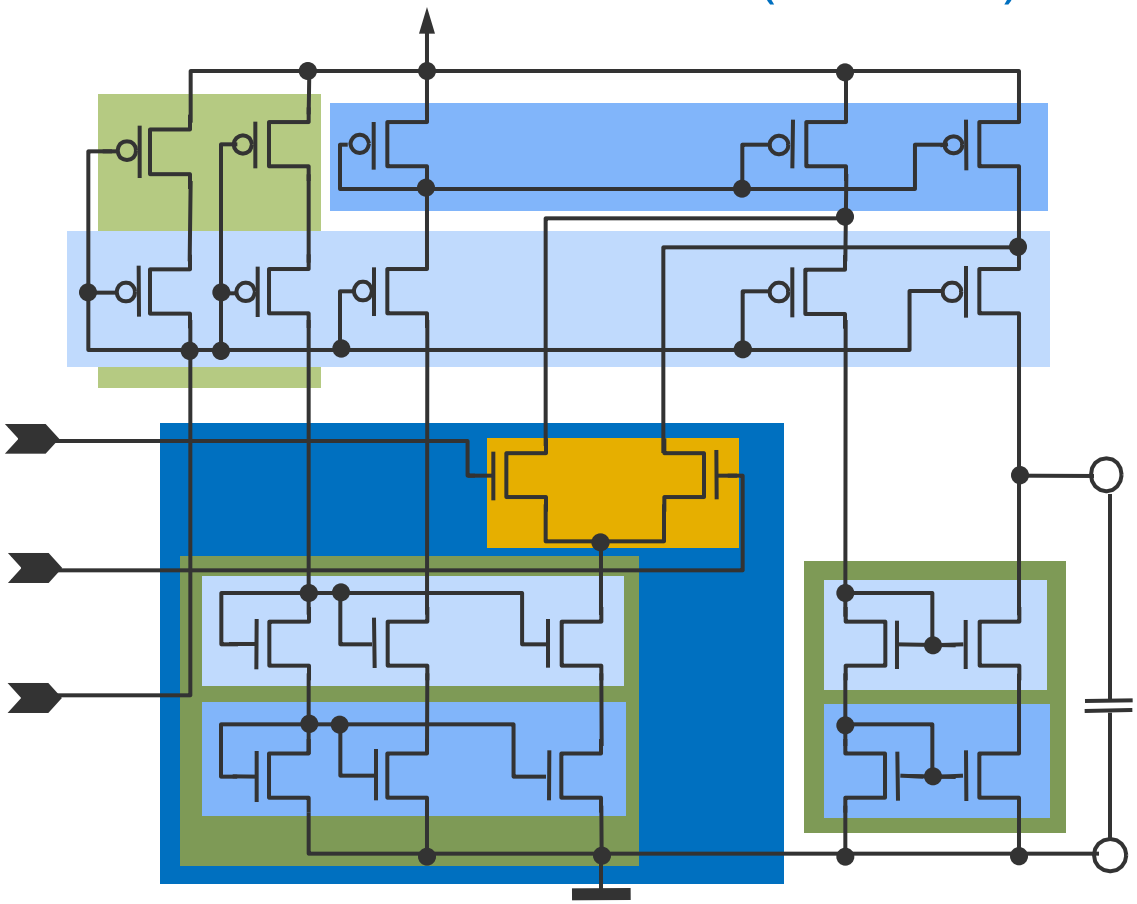


CM bank



differential stage

MOS Transistor Netlist („Circuit“)



differential pair

4-transistor current mirror

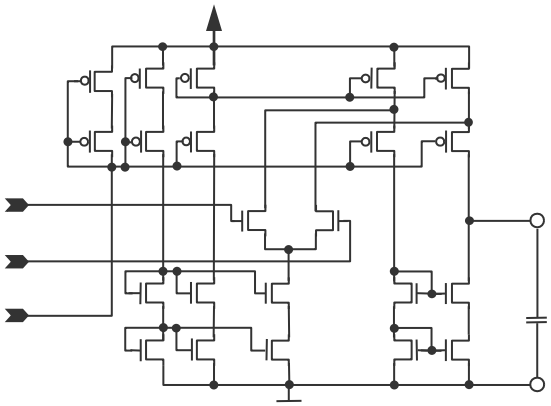
current mirror

level shifter

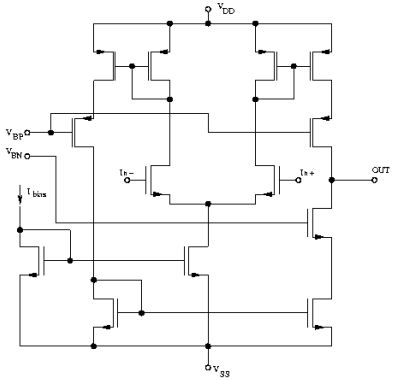
cascode current mirror

differential stage

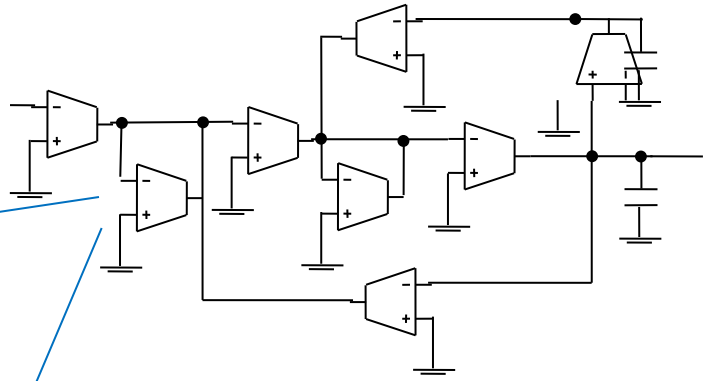
AMS Circuits – Examples



CMOS folded cascode operational amplifier



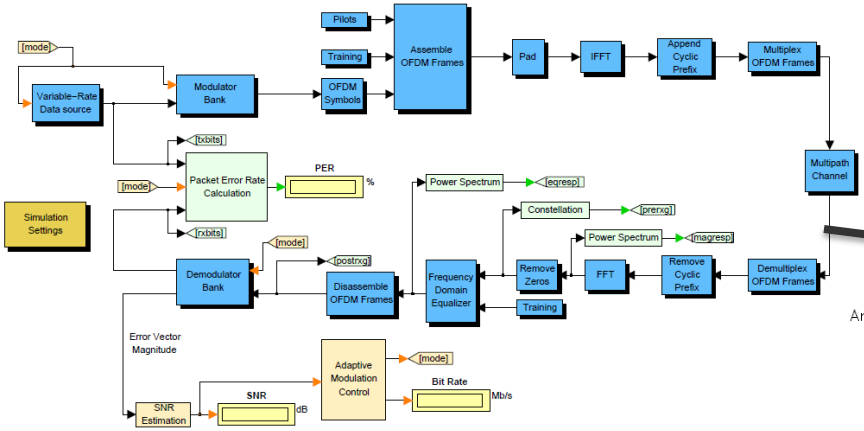
CMOS transconductance operational amplifier (OTA)



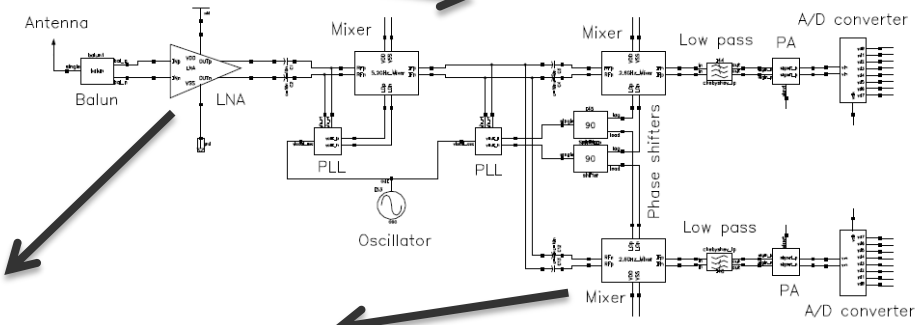
OTA-C biquad filter

AMS Circuits – Examples

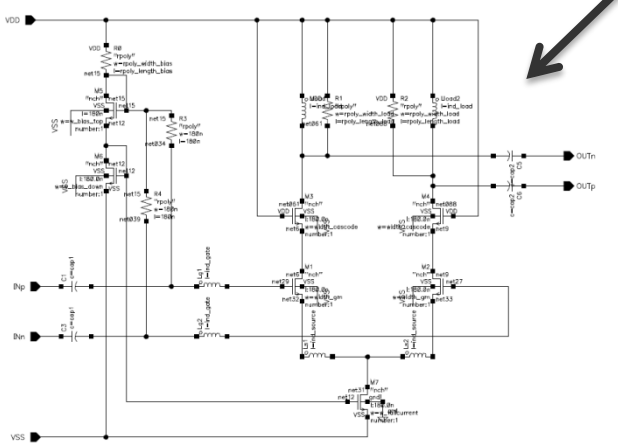
Communication system

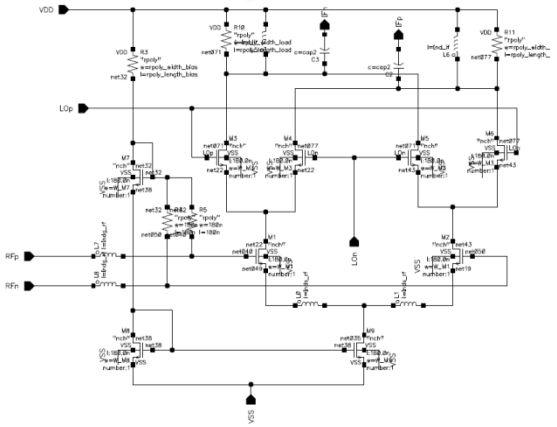


Analog receiver front end



Low noise amplifier

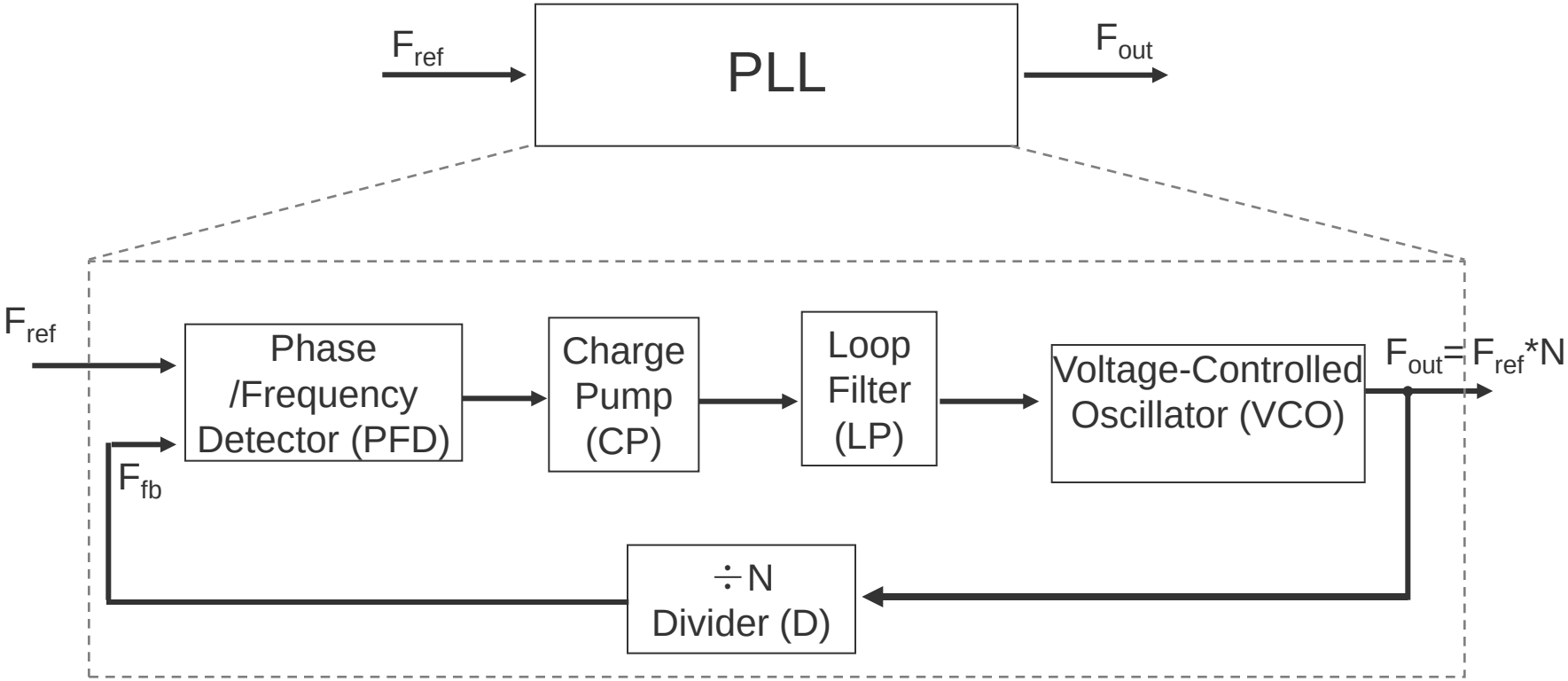




Mixer

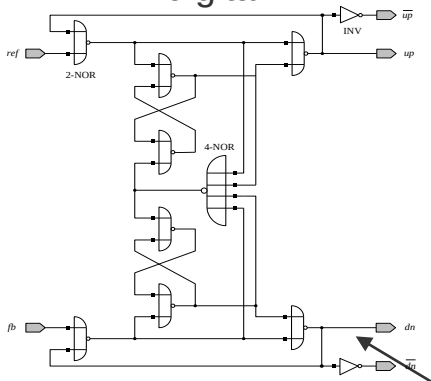
AMS Circuits – Examples

- Phase locked loop (PLL)

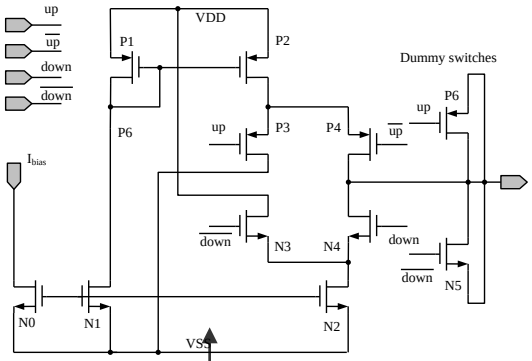


PLL on Transistor Level

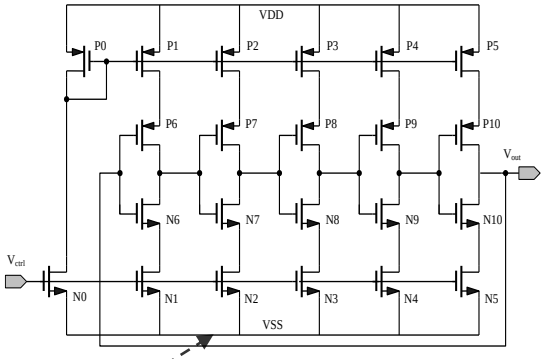
digital PFD

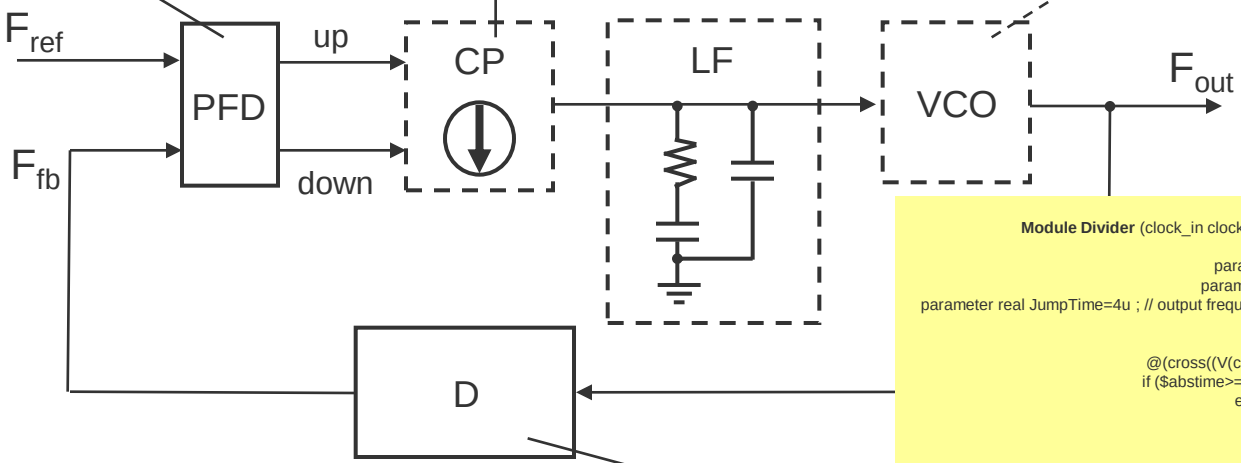


externally biased CP



five-stage single-ended VCO





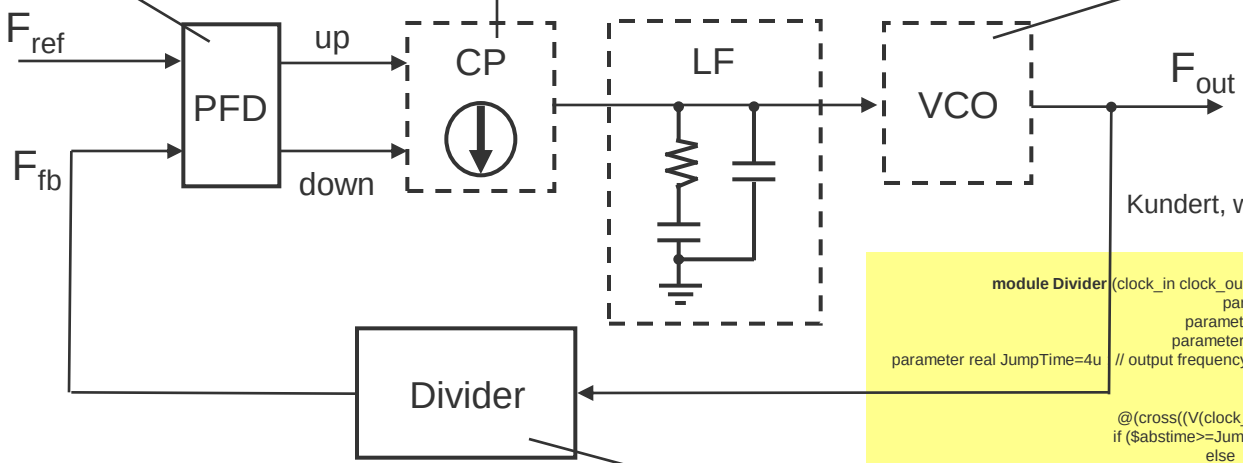

```
Module Divider (clock_in clock_out)
                                    parameter real td = 0;
                                    parameter real N_min = 6 ;
                                    parameter real N_max = 20 ;
parameter real JumpTime=4u ; // output frequency jump time integer
                                    count, n, M;
                                    analog begin
                                    @(cross((V(clock_in)-v_th),1)) begin
                                    if ($abstime>=JumpTime) M=N_max;
                                    else   M=N_min;
                                    count=count+1;
                                    if (count>=M) count=0;
                                    n = (2*count >= M);
                                    end
                                    V(clock_out)<+ transition(n? v_high : v_low, td, tt);
                                    ……
                                    endmodule
```

PLL on Behavioral Level

```
module pfd (ref, fb, u, d);
  output u, d; input ref, fb;
  electrical u, d, ref, fb;
  parameter real v_high=1.5;
  parameter real ttol=10p;
  parameter tt=120p;
  ....
  integer state;
  analog begin
  @(cross(V(ref)-v_high/2), +1,ttol)
    if (state <1)  state = state +1;
  @(cross(V(fb)-v_high/2), +1,ttol)
    if (state >-1)  state = state - 1;
  V(u) <+ transition((state==+1) ? v_high : 0.0, td_u, tt);
  V(d) <+ transition((state==-1) ? 0.0 : v_high, td_d, tt);
  .....
endmodule
```

```
module ChargePump (Iout, Down, N_Down, N_Up, Up, V_bias_n, V_bias_p);
  output Iout; input Down, N_Down, N_Up, Up, V_bias_n, V_bias_p;
  electrical Iout, Down, N_Down, N_Up, Up, V_bias_n, V_bias_p;
  ......
  parameter real Ip=25.0e-6;
  parameter real v_max=1.3, v_min=0.2;
  ....
  integer state;
  analog begin
  @(cross(V(Up)-v_th, 1))      begin  state = -1;  end
  @(cross(V(Down)-v_th, 1))    begin  state = 1;   end
  @(cross(V(Up)-v_th, -1))     begin  state =0;    end
  @(cross(V(Down)-v_th, -1))   begin  state =0;    end
  @(cross(V(Iout)-v_max, 1))   begin  state =0;    end
  @(cross(V(Iout)-v_min, -1))  begin  state =0;    end
  I(Iout)<+transition(Ip*state*(1+state*Mis), Delay, TransTime);
  ......
endmodule
```

```
module VCO (V_tune, VCO_out)
  ......
  parameter real Vmax=Vmin+1 from(Vmin:10e5);
  parameter real Fmin=1 from(0:10e9);
  parameter real Fmax=2*Fmin from(0:10e9);
  parameter real ttol=1u/Fmax from(0:1/Fmax);
  real freq, phase;
  real kvco;
  analog begin
  kvco= (Fmax-Fmin)/(Vmax-Vmin)
  freq=(V(V_tune)-Vmin)*kvco+Fmin;
  if(freq>Fmax) freq=Fmax;
  if(freq<Fmin) freq=Fmin;
  phase=idtmod(freq, 0.0, 1.0, -0.5);
  @(cross(phase-0.25,1,ttol))begin  Vout=vhi;  end
  @(cross(phase+0.25,1,ttol))begin  Vout=vlo;  end
  V(VCO_out)<+transition(Vout,0,tt);
  ......
endmodule
```



Kundert, www.designers-guide.com

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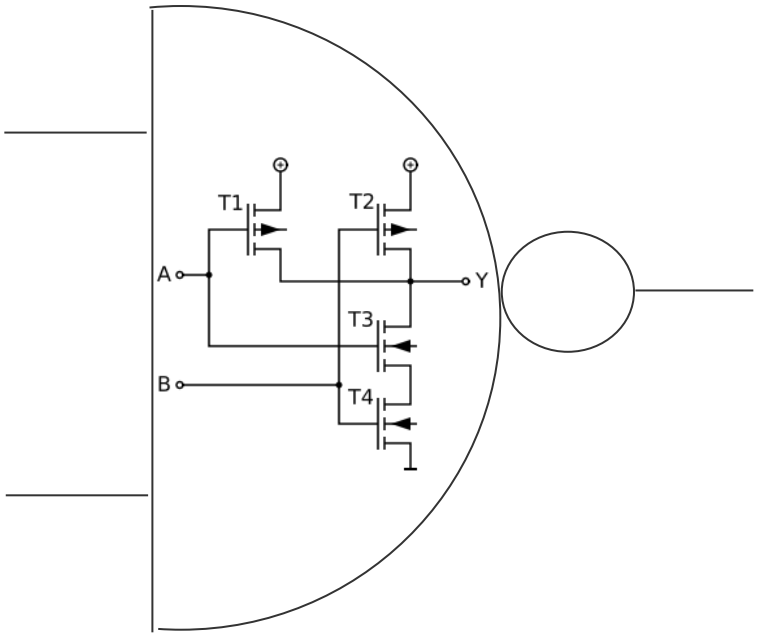
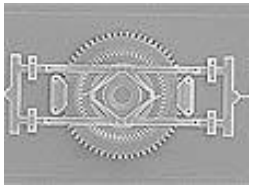
  parameter real N_min = 6 ;
  parameter real N_max = 20 ;
parameter real JumpTime=4u  // output frequency jump time integer
  count, n, M;
  analog begin
  @(cross((V(clock_in)-v_th),1)) begin
  if ($abstime>=JumpTime) M=N_max;
    else   M=N_min;
      count=count+1;
    if (count>=M) count=0;
      n = (2*count >= M);
      end
  V(clock_out)<+ transition(n? v_high : v_low, td, tt);
  ......
endmodule
```

AMS Circuits – Examples

NAND
Gate



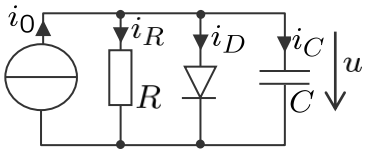
MEMS
step motor

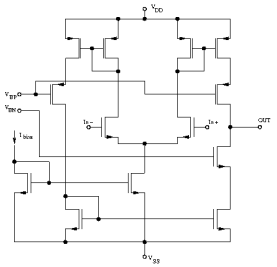


Courtesy of Sandia National Laboratories,
SUMMiT™ Technologies, www.mems.sandia.gov

Models, Simulation, Design

AMS Modeling





$$\dot{u} + \frac{1}{RC}u + \frac{I_S}{C}\left(\exp(\frac{u}{U_T}) - 1\right) - \frac{1}{C}i_0 = 0$$

```
ENTITY ota is
GENERIC
(gdm:real;Cin:real;CT:real;Cout:real;Rout:real;);
PORT ( terminal Tplus, Tminus, Tout, Tvdd, Tvss
, Tibias: electrical);
END ENTITY ota;
architecture behavioural_simple of ota is
…
```

Structural modeling with lumped elements

- transistor/circuit netlist
- block diagram

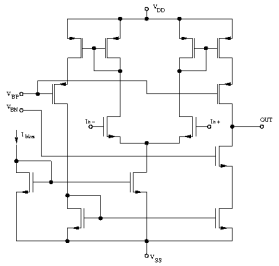
Behavioral modeling e.g.

- nonlinear differential equations
- behavior description code (VHDL, …)

Hierarchical modeling

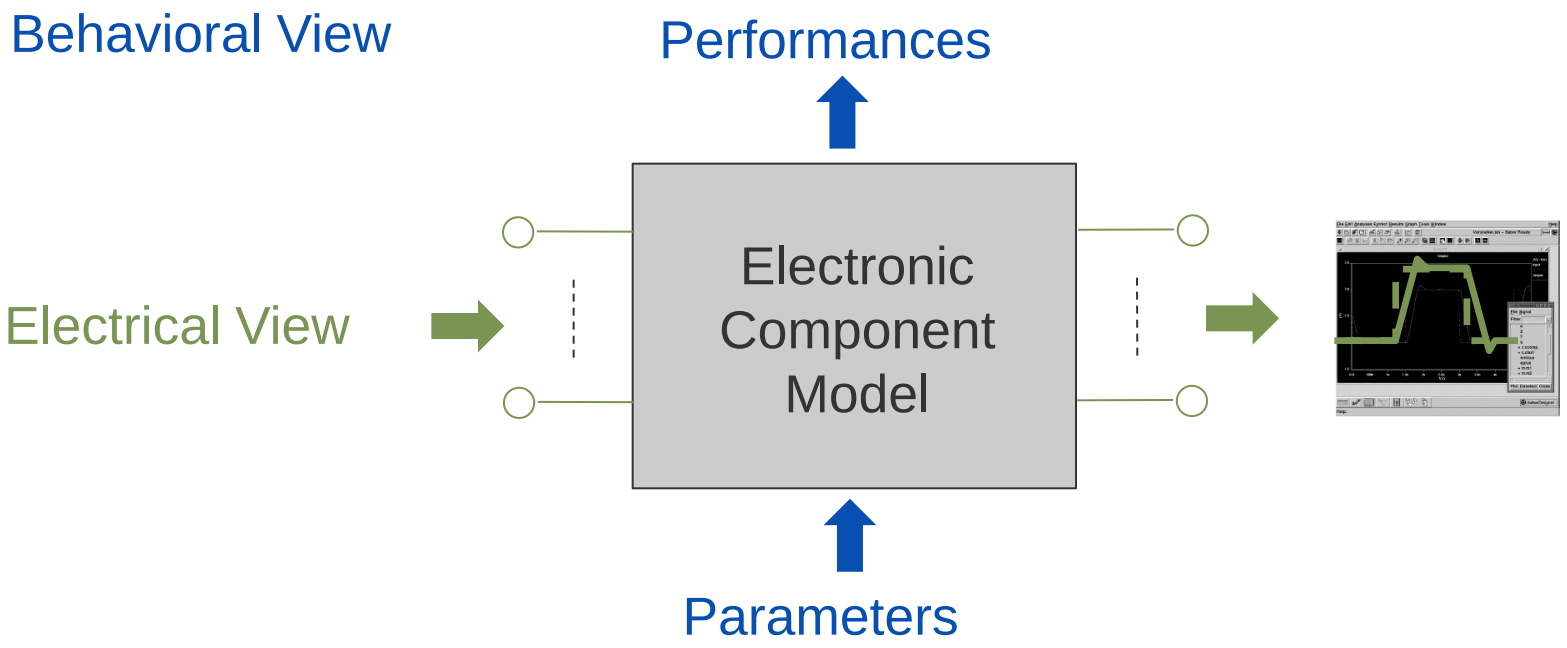
- Abstraction of physical effects
- Switch between structural/behavioral modeling

AMS Circuit Simulation



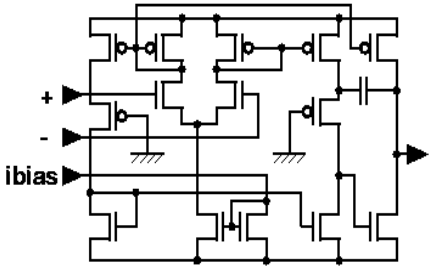
- Numerical solution of differential algebraic equations (DAEs)
- Eventually, of partial differential equations (PDEs)
- Modified nodal analysis:
- DC (operating point) analysis — ***V*** constant
- AC (small-signal) — ***V*** depending on frequency
- TR (large-signal transient) analysis — ***V*** depending on time
- HB, PSS, …
- Map ***V*** on performance values ***f***

AMS Circuit Simulation

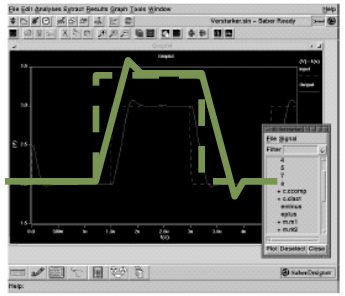


AMS Circuit Simulation

- Performances $\mathbf{f} \in \mathbb{R}^{n_f}$, sizing constraints $\mathbf{c}(\mathbf{x}_d) \geq \mathbf{0}$
  - Gain, bandwidth, matching, ...
  - Simulator output

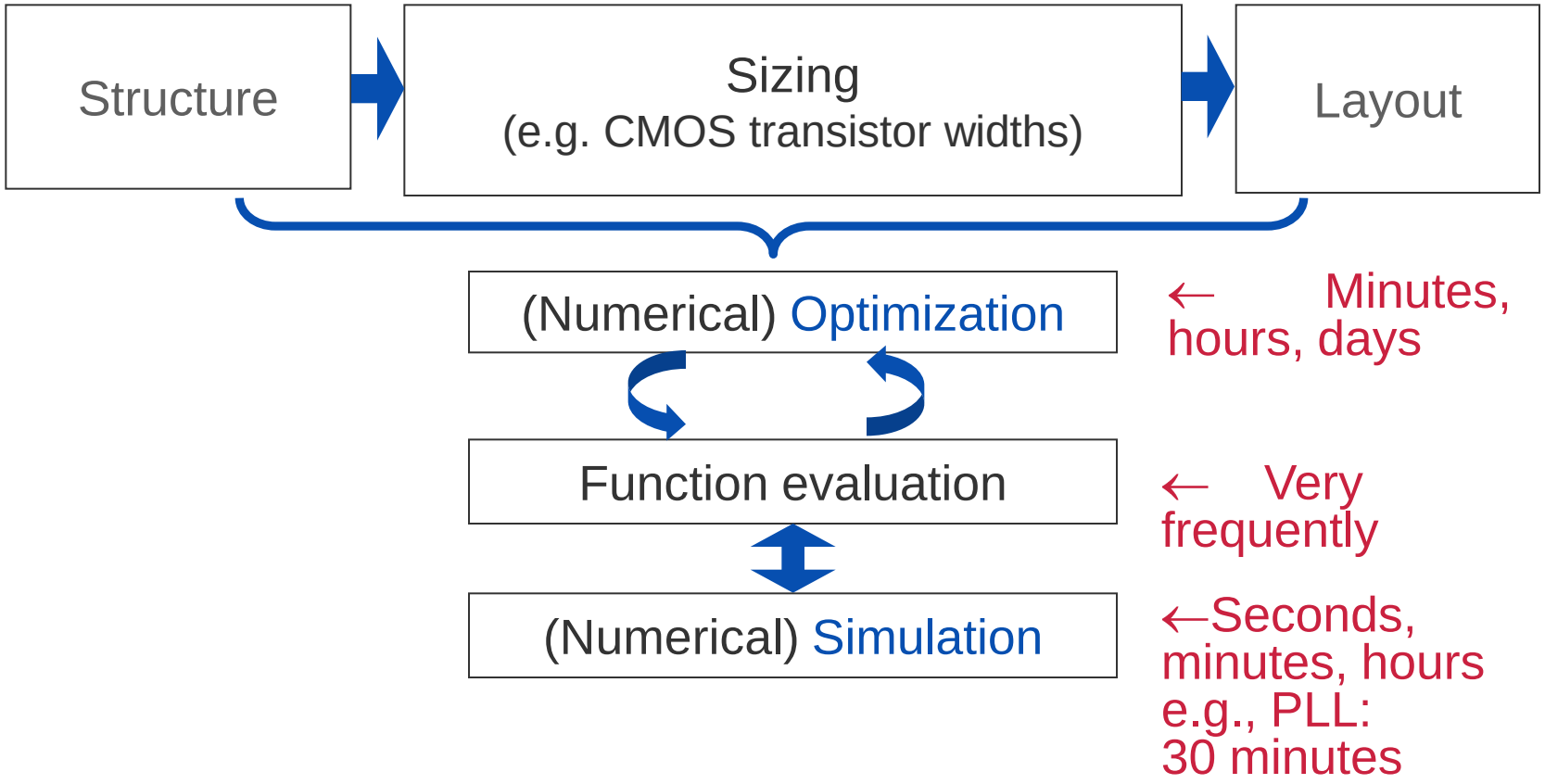


- Parameters $\mathbf{x} \in \mathbb{R}^{n_x}$
  - Design parameters (transistor widths, ...) $\mathbf{x}_d \in \mathbb{R}^{n_{xd}}$
  - Statistical parameters (threshold voltage, oxide thickness, …) $\mathbf{x}_s \in \mathbb{R}^{n_{xs}}$
  - Range parameters (supply voltage, temperature, ...) $\mathbf{x}_r \in \mathbb{R}^{n_{xr}}$
  - Simulator input



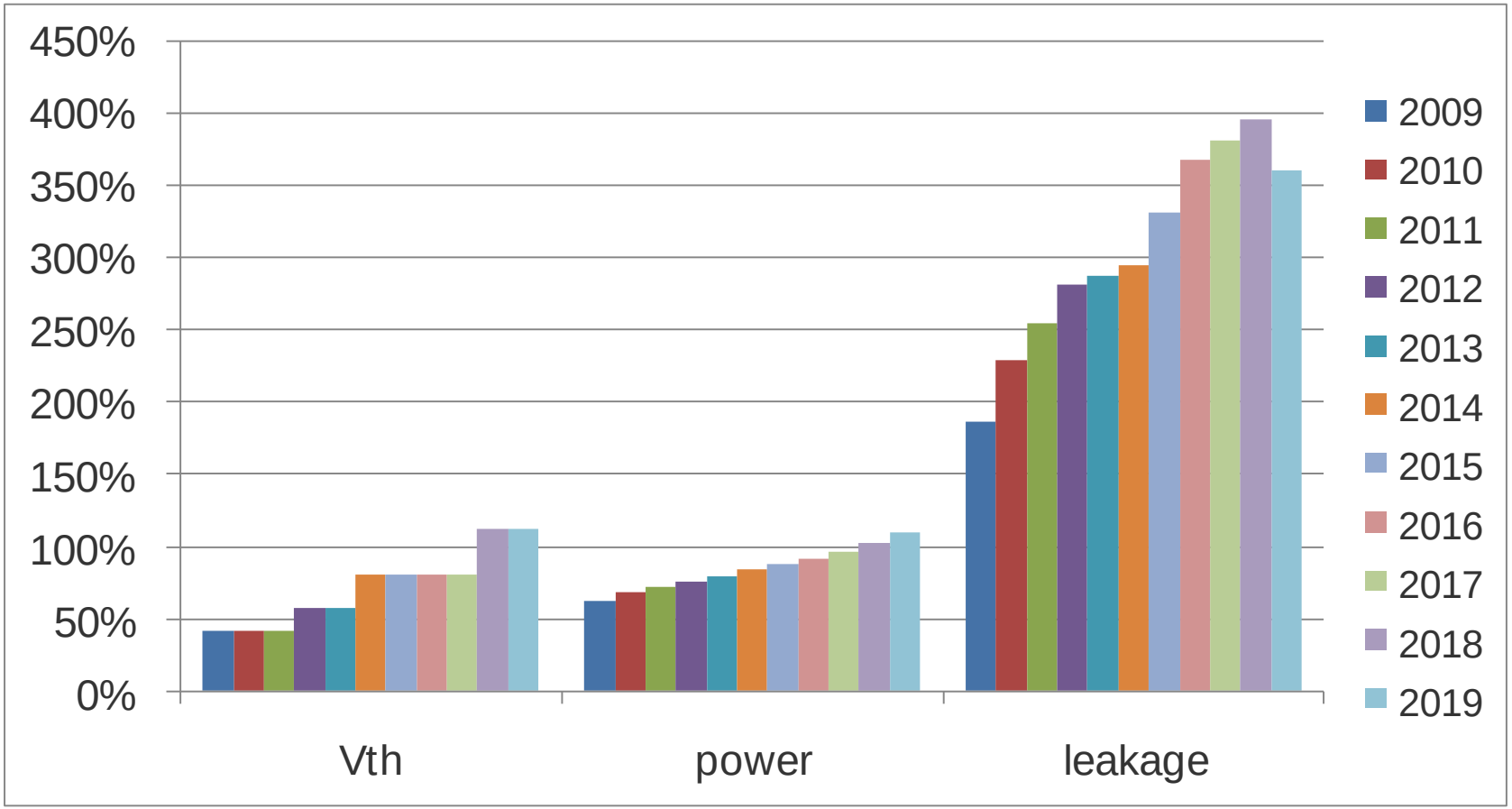
- Simulation $\mathbf{x} \mapsto \mathbf{f}$
  - Netlist, simulation bench, process technology
  - Abstraction from the physical level

AMS Design Steps



Variability (Manufacture, Operation)

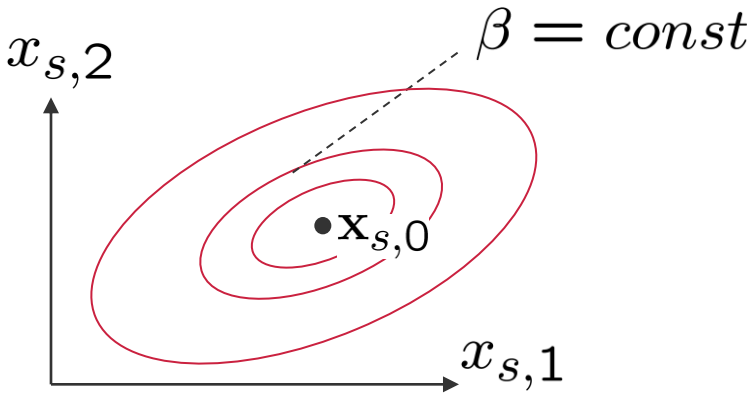
Manufacturing Variability (Source: ITRS 2009)

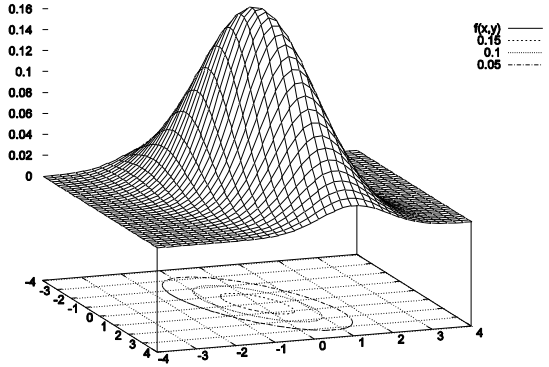


Process Variation Modeling on Circuit Level

- Statistical distribution of transistor parameters
  - e.g. variation of channel length/width ΔL, ΔW, oxide thickness t_{ox}, channel doping N_n, N_p, charge mobility μ_n, μ_P, junction capacitance C_{jn}, C_{jp}, junction depth x_{jn}, x_{jp}, series resistance R_n, R_p [Müller-Liebler, PASTA, Int. J. Circuit Theory and Appl., 1995]
  - e.g. ΔL, ΔW, oxide capacitance C_{ox}, flat band voltage V_{fb} [Hocevar, Cox, Yang, Parametric Optimization for MOS, IEEE Trans. CAD. 1988]
  - oxide thickness t_{ox}, threshold voltage V_{thn}, V_{thp} (global + lokal), charge mobility μ_n, μ_P (global + lokal), square resistance R_{sq} [MunEDA]
- Yield: percentage/portion of manufactured ICs that pass the production test

Statistical Parameter Distribution



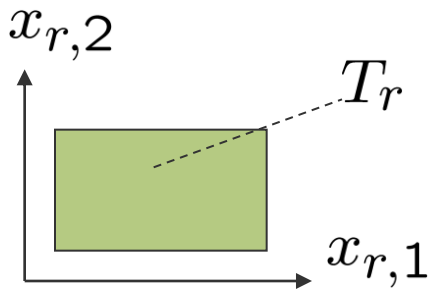


$$pdf(\mathbf{x}_s) = \frac{1}{\sqrt{2\pi}^{nxs}\sqrt{\det \mathbf{C}}} \exp(-\frac{1}{2}\beta^2(\mathbf{x}_s))$$

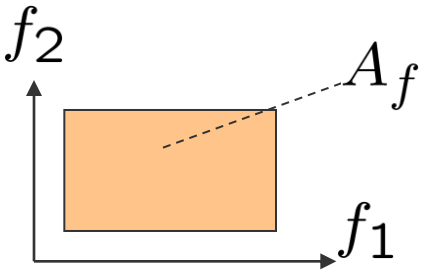
$$\beta^2(\mathbf{x}_s) = (\mathbf{x}_s - \mathbf{x}_{s,0})^T \mathbf{C}^{-1} (\mathbf{x}_s - \mathbf{x}_{s,0})$$

- Transformation in normal distribution of $\mathbf{x}_s \in \mathcal{R}^{nxs}$ with
  - mean vector $\mathbf{x}_{s,0}$
  - covariance matrix $\mathbf{C}$

Operating Range, Performance Specification

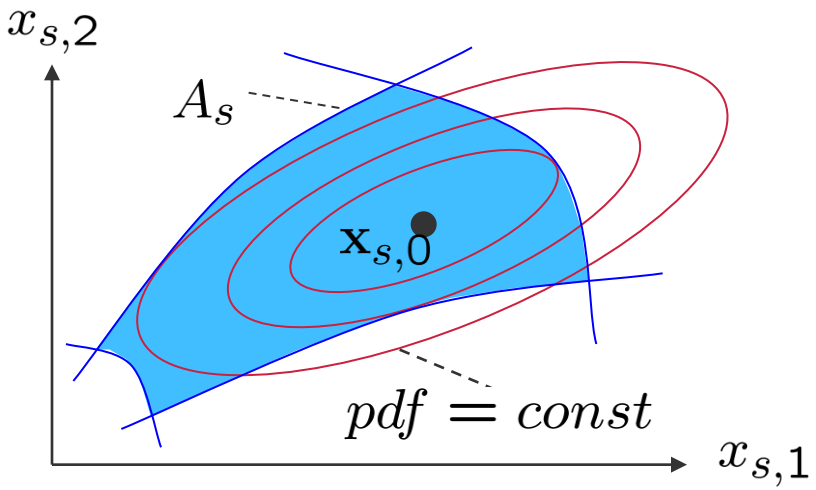


- Operating range
  - Bounds for environmental parameters
    $x_{r,i} \geq x_{r,L,i},\ i = 1, \ldots, 2n_{xr}$
    $(x \leq x_U \Leftrightarrow -x \geq -x_U)$
  - Simulator input



- Performance specification
  - Bounds for performances
    $f_i \geq f_{L,i},\ i = 1, \ldots, 2n_f$
  - Simulator output

Yield



- Gaussian bell cut by specs
- Integral of pdf over acceptance region
- Estimation by Monte-Carlo analysis
- Approximation by Worst-Case Distances

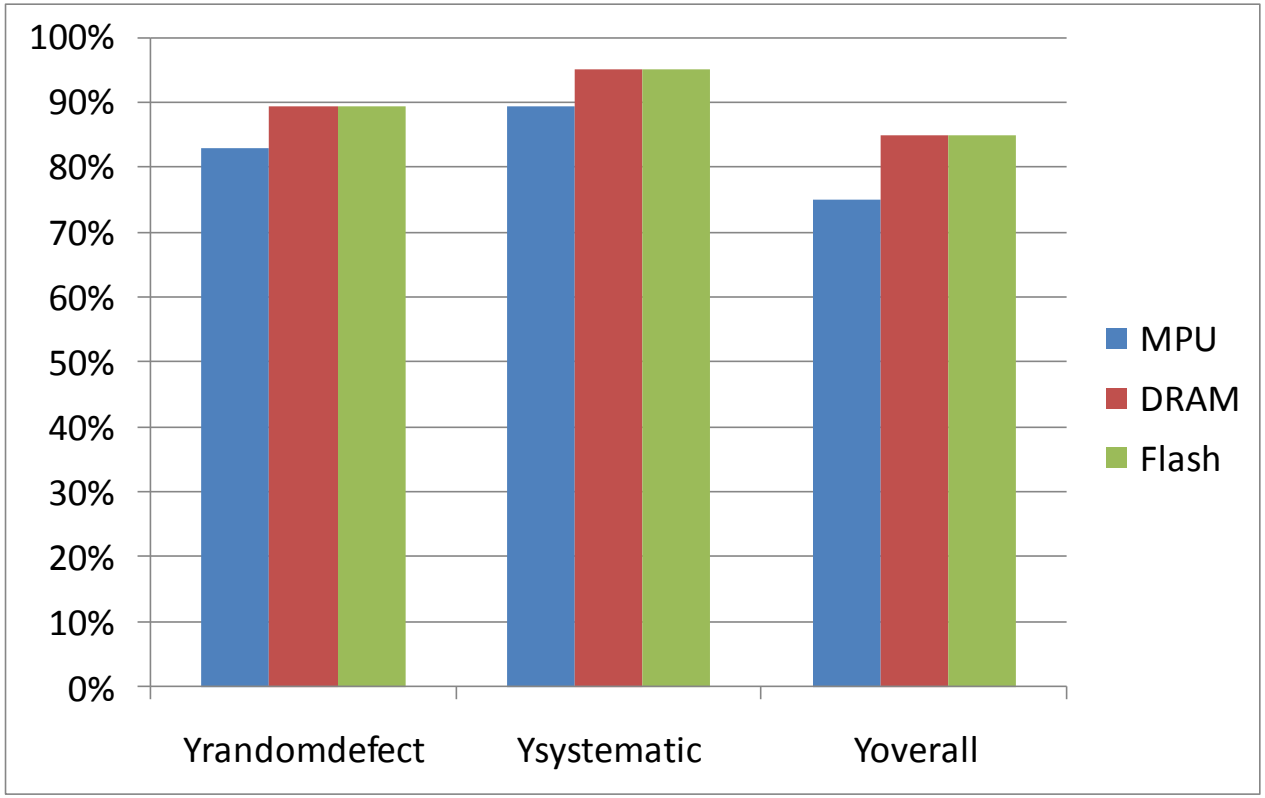
$$Y = \int \dots \int_{A_s} pdf(\mathbf{x}_s) d\mathbf{x}_s$$

$$A_s = \left\{ \mathbf{x}_s \;\middle|\; \forall_{\mathbf{x}_r \geq \mathbf{x}_{r,L}} \mathbf{f}_L \leq \mathbf{f}(\mathbf{x}_d, \mathbf{x}_s, \mathbf{x}_r) \leq \mathbf{f}_U \right\}$$

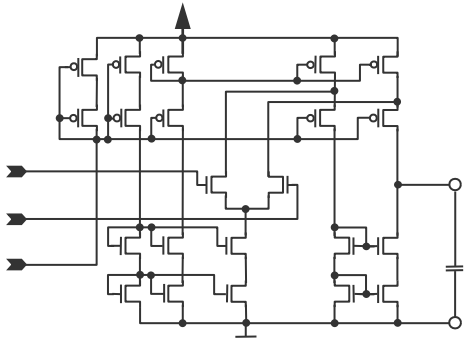
Yield Budget (Source: ITRS 2009)

"Design for manufacturability"

Layout! Sizing!



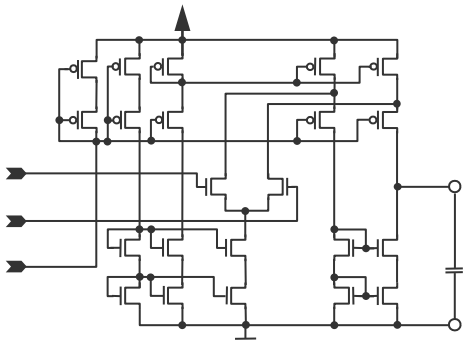
Yield Optimization – Example

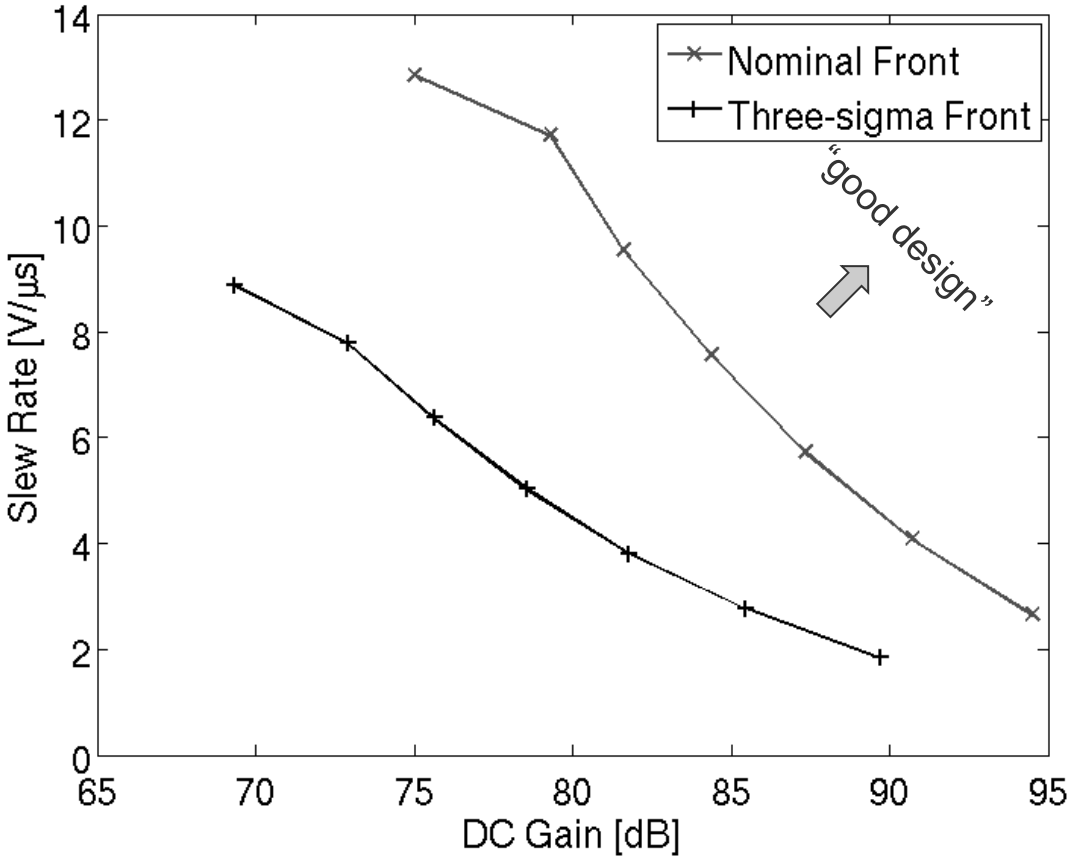


Performance	Specification	Design 1		Design 2	
Gain	≥ 65dB	76dB	(2.5σ)	76dB	(4.2σ)
Transit frequency	≥ 30MHz	67MHz	(7.7σ)	58MHz	(4.5σ)
Phase margin	≥ 60°	68°	(1.8σ)	71°	(3.9σ)
Slew rate	≥ 32V/μs	67V/μs	(6.3σ)	58V/μs	(3.9σ)
DC power	≤ 3.5 mW	2.6μW	(1.1σ)	2.3μW	(4.2σ)
	Yield		**82.9%**		**99.99%**

- K. Antreich and J. Eckmueller and H. Graeb and M. Pronath and F. Schenkel and R. Schwencker and S. Zizala *WiCkeD: Analog Circuit Synthesis Incorporating Mismatch*, IEEE CICC 2000
- H. Graeb: Analog Design Centering and Sizing, Springer Verlag 2007

Trade-off Design – Example

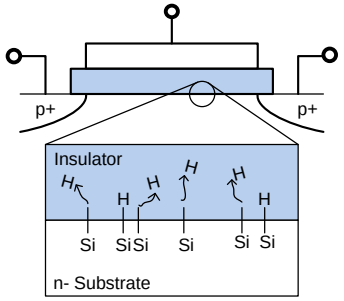


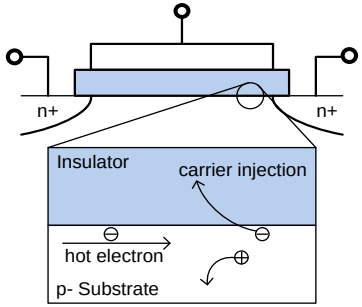


- D. Mueller-Gritschneder, H. Graeb Computation of Yield-optimized Pareto Fronts for Analog Integrated Circuit Specifications, DATE 2010

Reliability (Aging)

Aging Effects



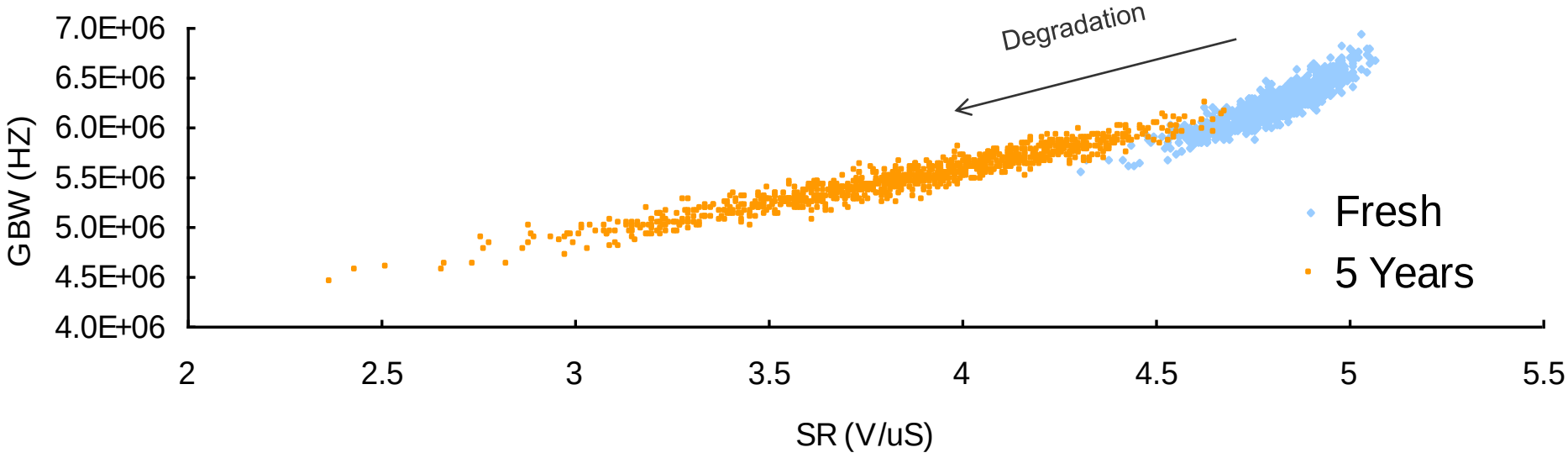


- Negative Bias Temperature Instability (NBTI)
- Si-H bonds break at Si/SiO_2 interface

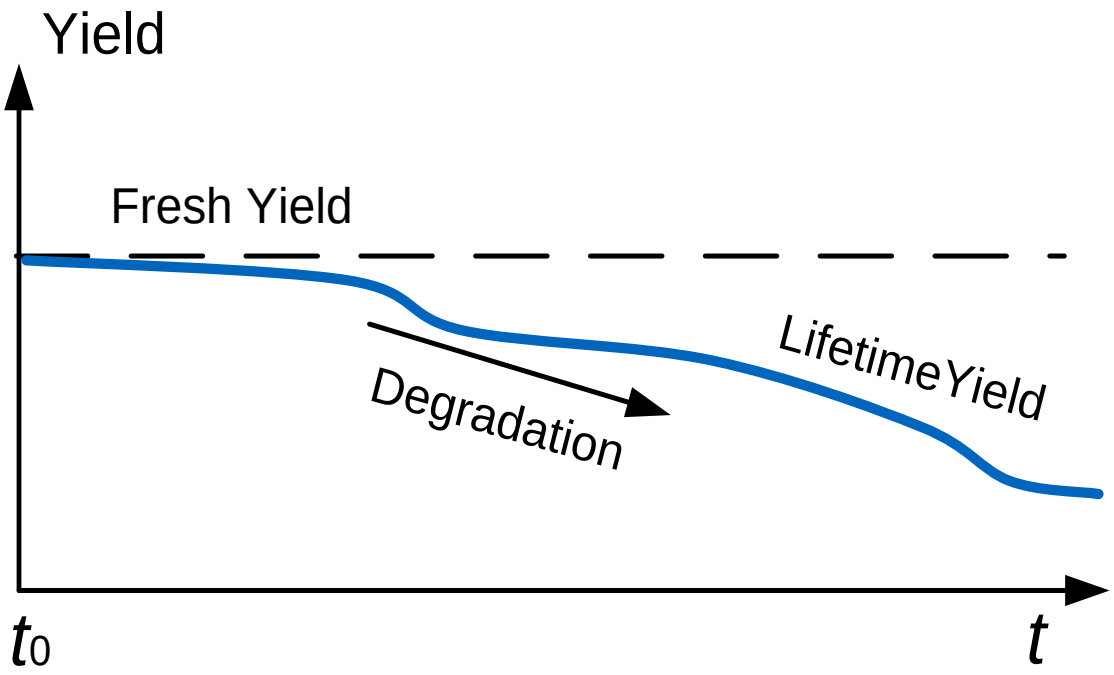
- Hot Carrier Injection (HCI)
- Electron-Hole pairs break due to collisions with hot channel carriers (Impact Ionization)

- Shift threshold voltage and transconductance

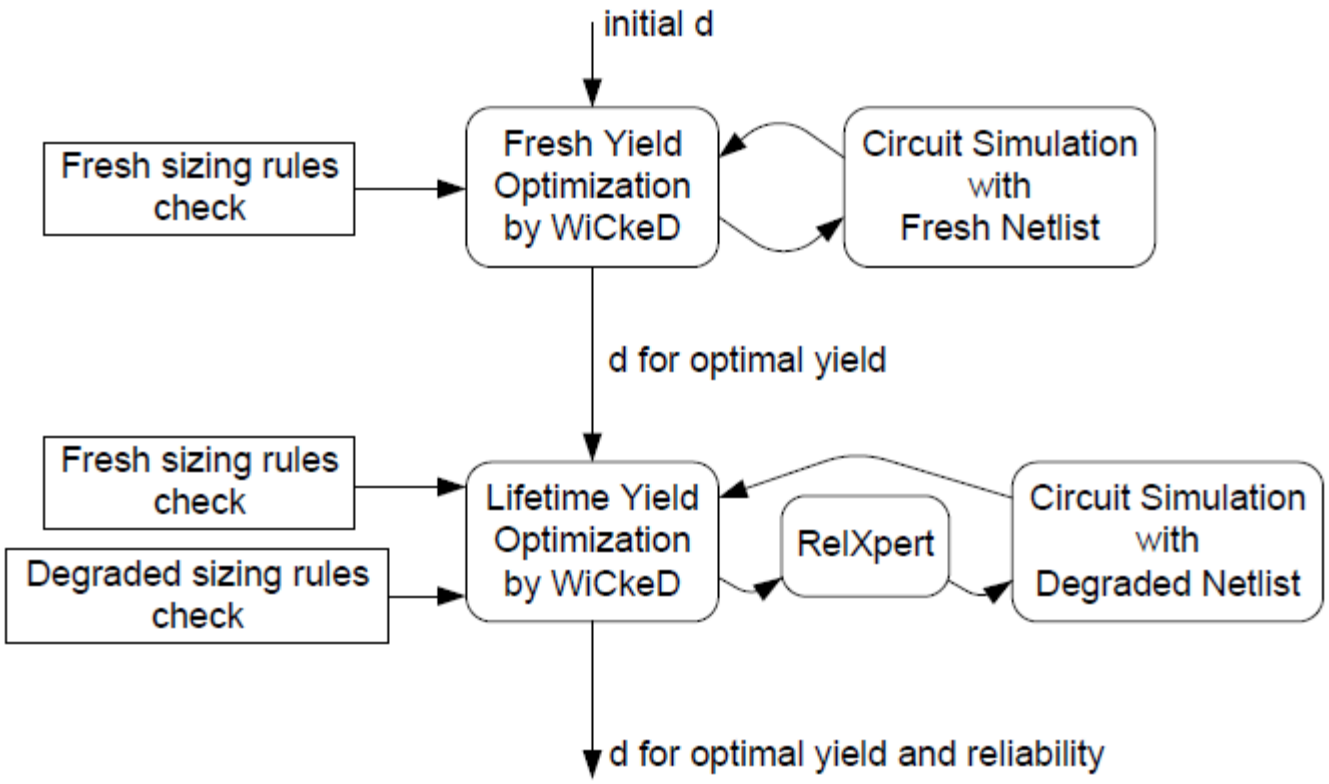
Variability over Lifetime



Lifetime Yield



Analog Sizing for Reliability – Flow



- Xin Pan, H. Graeb: Lifetime Yield Optimization of Analog Circuits Considering Process Variations and Parameter Degradations, in: Advances in Analog Circuits, InTech - Open Access publisher, to appear 2011

Analog Sizing for Reliability – Example

- Miller OpAmp, 180nm, 1.7V

	yield-optimal		reliability-optimal	
	fresh	10 years	10 years	fresh
Gain≥80dB	4.0	3.9	3.9	3.9
Slew Rate $\geq 3V/\mu s$	4.2	1.9	3.4	5.8
GBW $\geq$ 2MHz	5.8	5.7	5.8	5.9
Phase Margin$\leq 120deg$	5.2	4.3	5.1	5.9
Power$\leq 2mW$	5.9	5.8	6.2	6.6
CMRR≥80dB	3.4	2.2	3.3	4.2
Relative Area	100%		107%	
Lifetime Yield	99.96%	94.50 %	99.93%	99.99%

ITRS 2010: AMS Design Technology Trends and Challenges

- Interactive and semiautomatic AMS design
- Parametric models and simulation of complex AMS blocks
- Standardized modeling and analysis of physical effects and complex performance features
- Appreciation of simulation as THE abstraction from the physical layer in AMS design
- Appreciation of simulation as THE interface for design automation in AMS design
- Provide simulators with sensitivity analysis capabilities
- Education of AMS design engineers and EDA tool developers
- AMSRF design tools are not for a flow but for a class of design problems

ITRS 2010: AMS Design Technology Trends and Challenges

- Interactive design aids for the generation and selection of circuit structures
- Interactive design aids for place & route
- Interactive design for yield and reliability
- Discrete optimization (e.g. layout fingers, manufacturing grid)
- Closer interaction between structural synthesis and layout synthesis
- Design space exploration
- Enhanced simulation speed

Conclusion

New device technologies require

- Models for all types of circuit simulation and analysis
- Circuit techniques with basic building groups (e.g. current mirror)
- Sufficient circuit manufacturing yield
- Sufficient circuit lifetime
- New design technologies