Nanoelectronics Trends for the Next Decade

January, 2011

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Director, SRC Nanoelectronics Initiative

Presentation Sources:
Nanotechnology Research Directions for Societal Needs in 2020: Retrospective and Outlook
Chapter 8. Applications: Nanoelectronics and Nanomagnetics (J. Welser, S. Wolf, P. Avouris, T. Theis)

- Full Report to be published (Springer, Boston and Berlin, 2010)
- PDF Version available online: http://www.wtec.org/nano2/

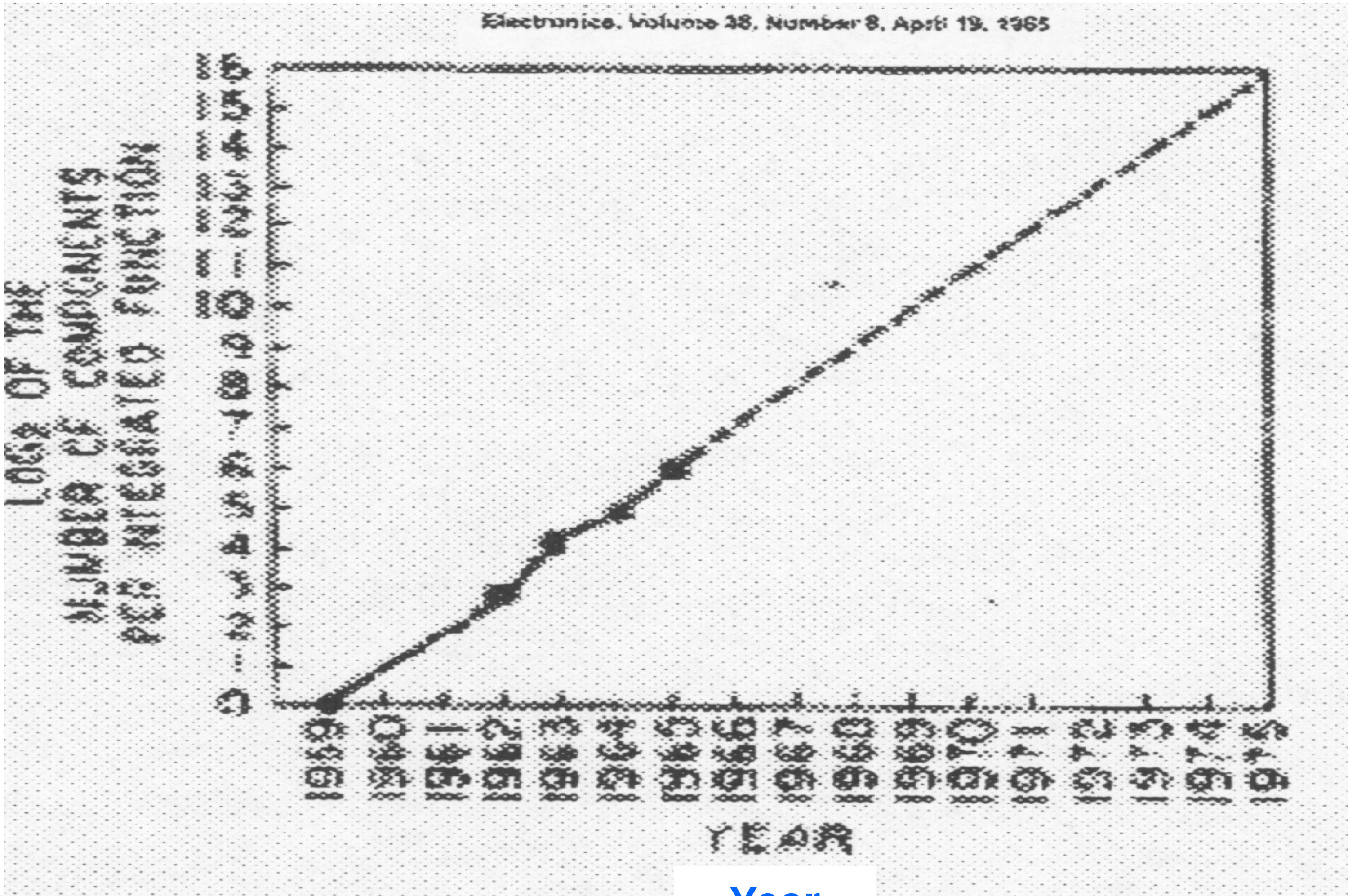
Semiconductor Research Corporation (SRC) Nanoelectronics Research Initiative
http://nri.src.org

Additional References:
International Technology Roadmap for Semiconductors (ITRS)
Emerging Research Devices (ERD) and *Emerging Research Materials (ERM)* Chapters
http://www.itrs.net/Links/2010ITRS/Home2010.htm

Moore's Law

Electronics, Volume 38, Number 8, April 19, 1965

Log of the Number of Components Per Integrated Function

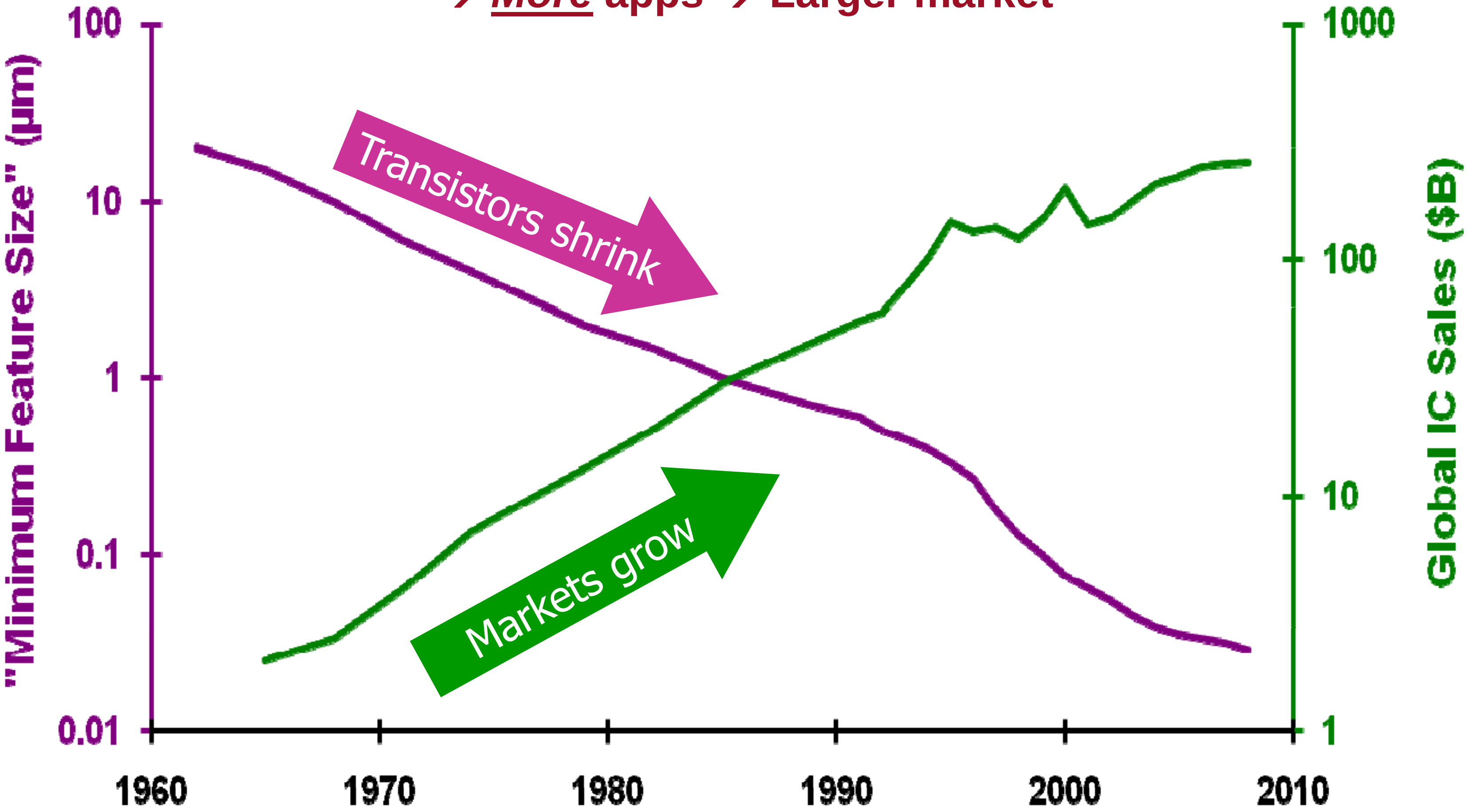


Year

Nanoelectronics Most Visible Impact

Scaling Drives the Semiconductor Industry

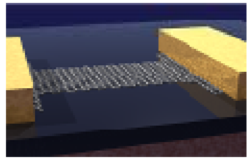
Smaller features → Better performance & cost/function → *More* apps → Larger market



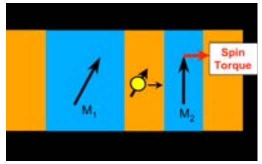
Courtesy of R. Doering, Texas Instruments;
Data from Semiconductor Industry Association, http://www.sia-online.org

Advances in Last Ten Years:
From Science to Product

- Science/Engineering Level:
  - Expansion of Carbon Electronics: (Re-)discovery of graphene; advances in nanotube fabrication and selection

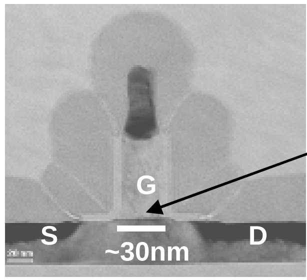


  - Emergence of Spintronics:
    - Demonstration of Spin Torque switching
    - Discovery of magnetoelectric / multiferroic materials
    - Discovery of the Spin Hall Effect
    - Demonstrations of spin injection and readout from semiconductors



  - Advances in resistive memory: Phase-Change, metal oxides
  - Fundamental understanding of semiconductor nanowire growth

- Product Level:
  - CMOS and FLASH scaled down to ~30nm
  - Magnetic Tunnel Junctions (MTJs)
    - Read Heads for Magnetic Recording; Magnetic RAM
  - Phase Change High Density Memory

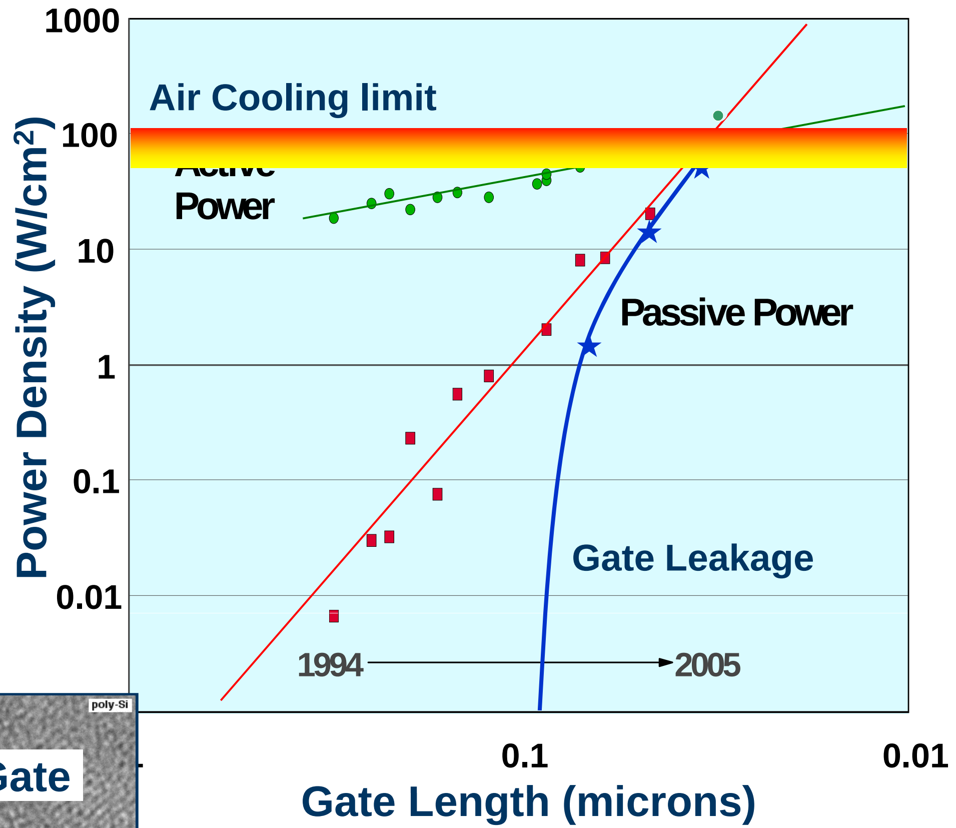


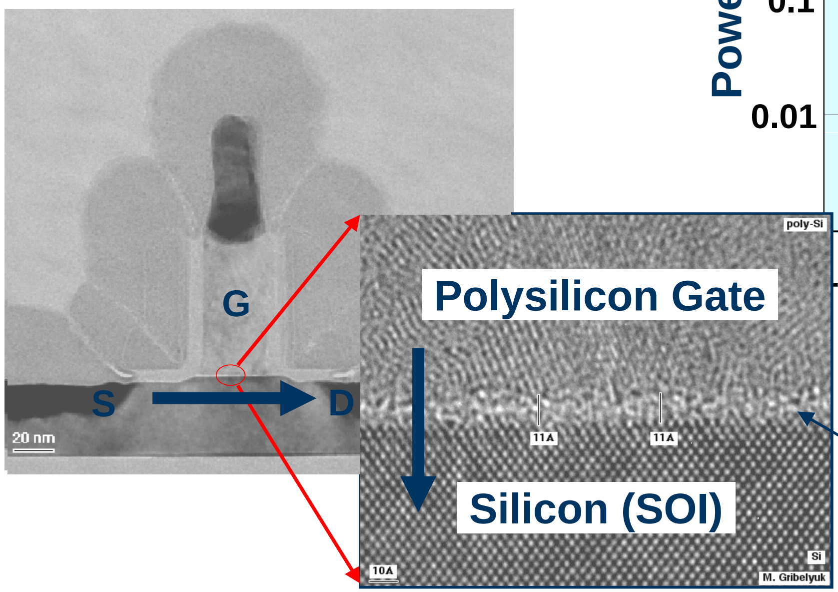
Insulator:
SiON ~ 1nm or
High-k ~3nm

- Impact: Exponential increase in the capability and mobility of electronic devices:
  A cellphone is now a computer, internet access device, stereo, video camera, game machine, GPS, etc.

Future Scaling: Power is ***THE*** Issue
Must find a lower energy device

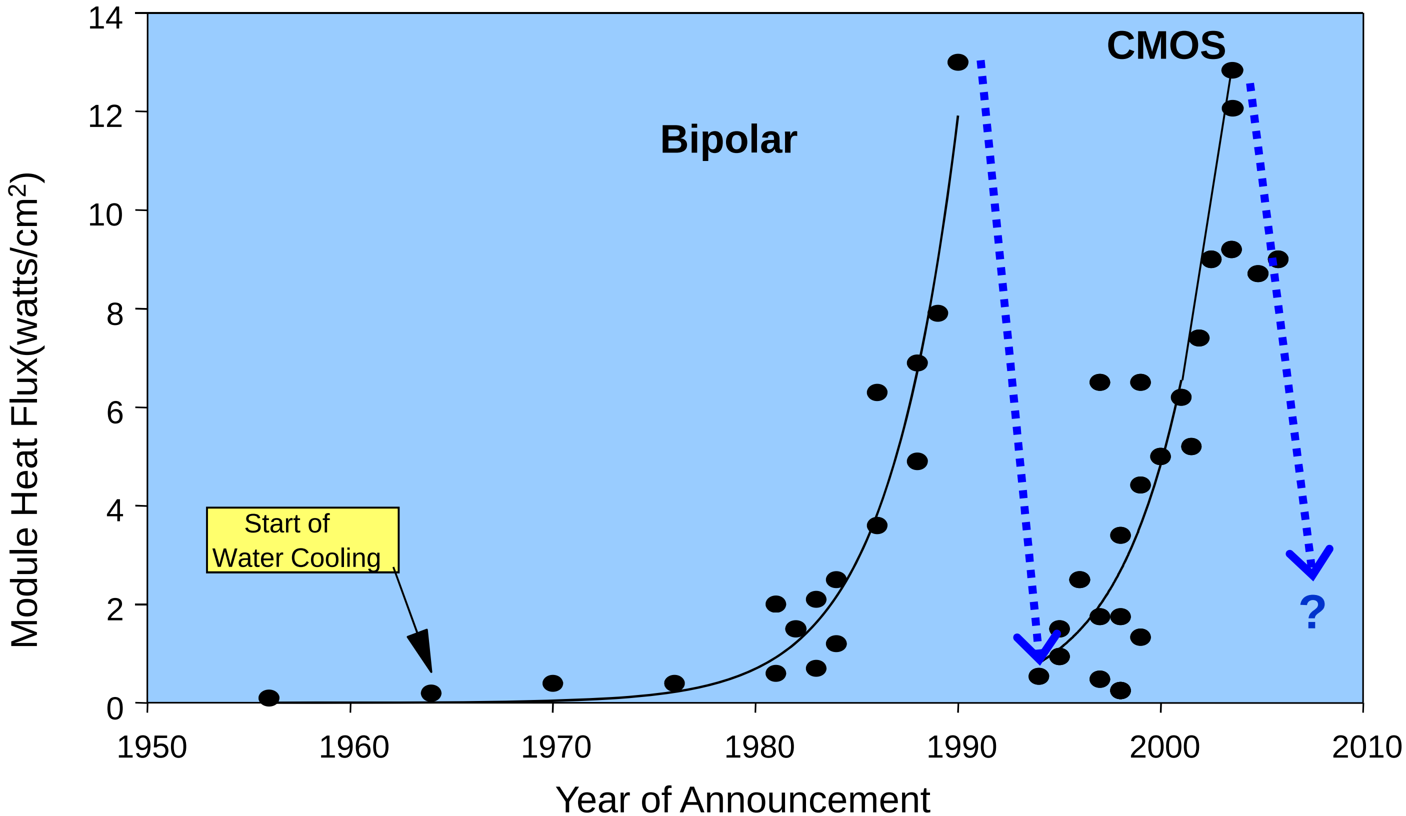
- Power components:
  - Active power
  - Passive power
    - Gate leakage
    - Source - Drain leakage





Gate Oxide

Has This Ever Happened Before?



- 2005 ~ 2015: New technology enhancements → Mainstream university and industry Research
  - Continued CMOS shrinking, low-power FET devices, multi-core chips, 3D packaging, new memory devices, etc.

> 2015? : New device technology → NRI Research

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Nanoelectronics Research Initiative
Mission Statement

NRI Mission: Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.

- These devices should **show significant advantage over ultimate FETs** in power, performance, density, and/or cost to enable the semiconductor industry to **extend the historical cost and performance trends** for information technology.
- To meet these goals, NRI pursues **five research vectors**, focused on discovering and demonstrating new devices and circuit elements for doing computation.
- Finally, it is desirable that these technologies be **capable of integrating with CMOS**, to allow exploitation of their potentially complementary functionality in heterogeneous systems and to enable a smooth transition to a new scaling path.

Beyond CMOS Logic: What to look for?

- **To beat the power problem requires:**
  - **A device with a lower energy, room temperature switching mechanism**

or

  - **A system that operates out of equilibrium or recovers operation energy as part of the logic computation**

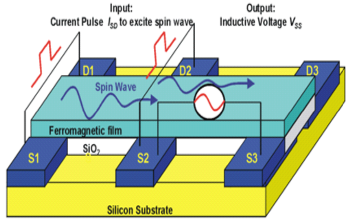
- **Required characteristics:**
  - **Scalability**
  - **Performance**
  - **Energy efficiency**
  - **Gain**
  - **Operational reliability**
  - **Room temp. operation**
- **Preferred approach:**
  - **CMOS process compatibility**
  - **CMOS architectural compatibility**

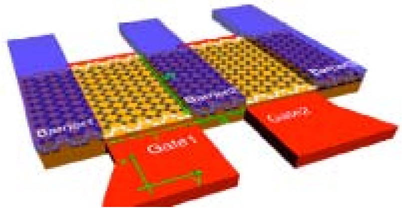
Alternative state variables

- **Spin–electron, nuclear, photon**
- **Phase**
- **Quantum state**
- **Magnetic flux quanta**
- **Mechanical deformation**
- **Dipole orientation**
- **Molecular state**

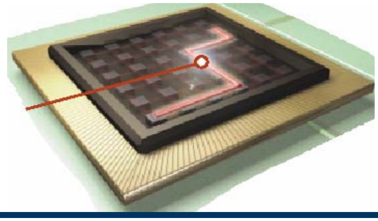
NRI Primary Research Vectors

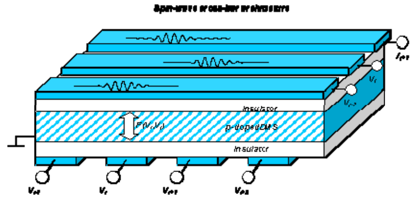
- NEW DEVICE
  Device with alternative state vector



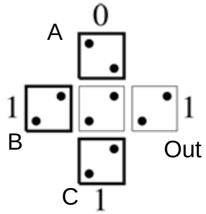


- NEW WAYS TO CONNECT DEVICES
  Non-charge data transfer

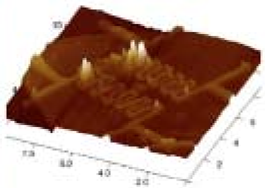




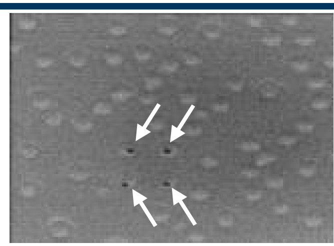
- NEW METHODS FOR COMPUTATION
  Non-equilibrium systems



- NEW METHODS TO MANAGE HEAT
  Nanoscale phonon engineering



- NEW METHODS OF FABRICATION
  Directed self-assembly devices



NRI Funded Universities

Finding the Next Switch

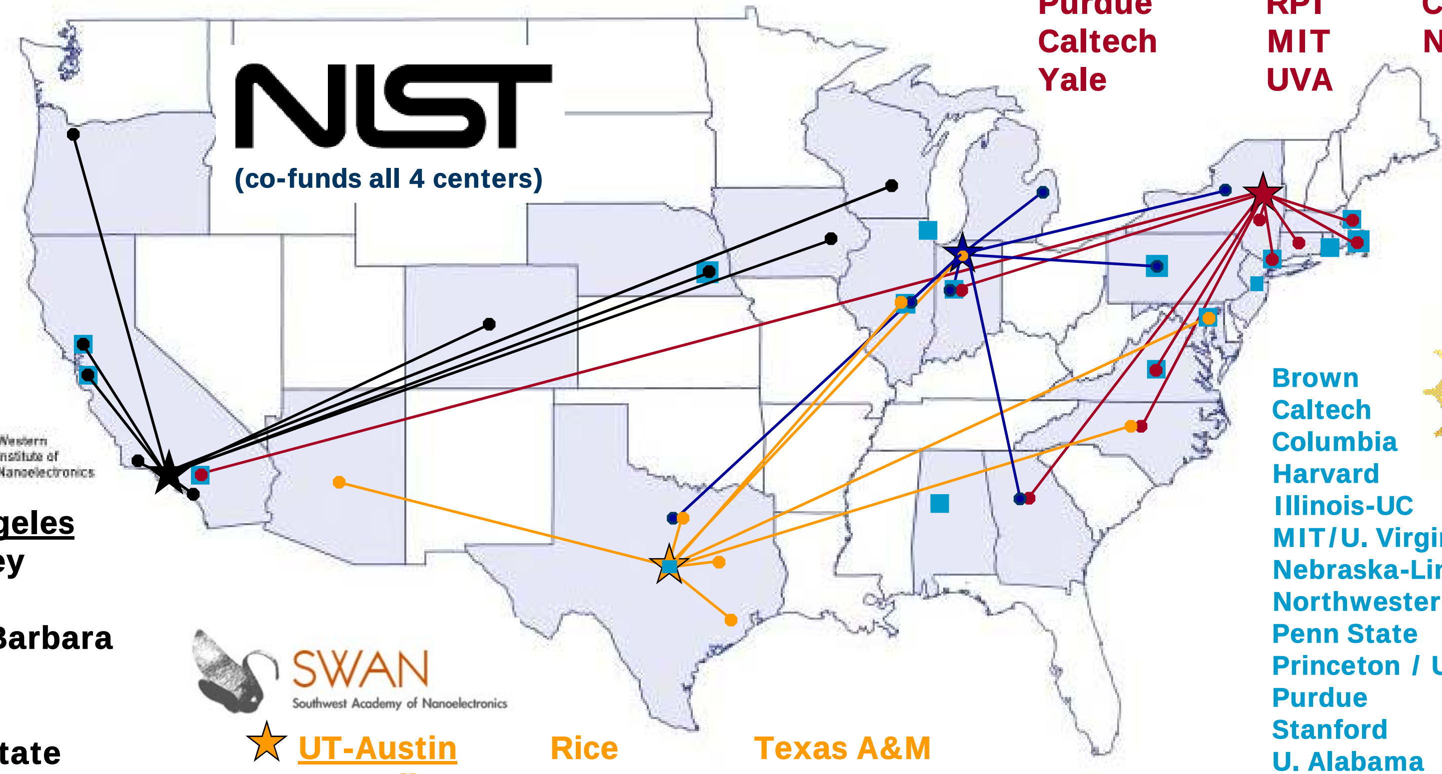
MIND — Nanoelectronics • Architectures — Midwest Institute for Nanoelectronics Discovery

★ <u>Notre Dame</u>
Illinois-UC
Michigan
Cornell
Purdue
Penn State
UT-Dallas
GIT

INDEX — Institute for Nanoelectronics Discovery and Exploration

★ <u>SUNY-Albany</u>
Purdue
Caltech
Yale
GIT
RPI
MIT
UVA
Harvard
Columbia
NCSU

NIST
(co-funds all 4 centers)



WIN — Western Institute of Nanoelectronics

★ <u>UC Los Angeles</u>
UC Berkeley
UC Irvine
UC Santa Barbara
Stanford
U. Denver
Portland State
U. Iowa
U. Nebraska-Lincoln
U. Wisconsin-Madison

SWAN — Southwest Academy of Nanoelectronics

★ <u>UT-Austin</u>
UT-Dallas
U. Maryland
Rice
ASU
NCSU
Texas A&M
Notre Dame
Illinois UC

NSF

Brown
Caltech
Columbia
Harvard
Illinois-UC
MIT/U. Virginia
Nebraska-Lincoln
Northwestern
Penn State
Princeton / UT-Austin
Purdue
Stanford
U. Alabama
UC Berkeley
U. Maryland

Over 35 Universities in 22 States

NRI Research Centers

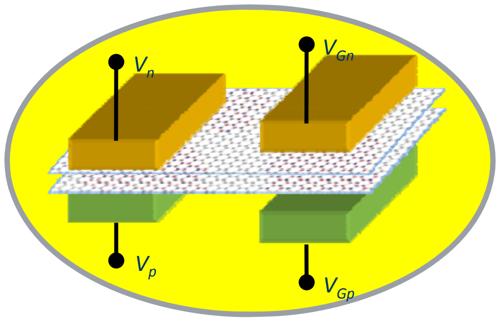
In Partnership with NIST

- Leveraging industry, university, and both state & fed government funds, and driving university nanoelectronics infrastructure

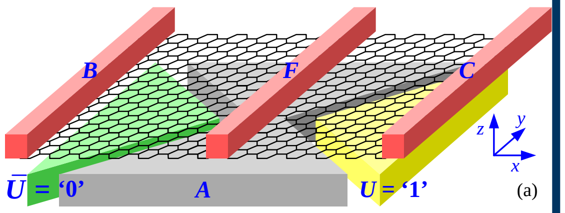
WIN Western Institute of Nanoelectronics	**INDEX** Institute for Nanoelectronics Discovery & Exploration	**SWAN** SouthWest Academy for Nanoelectronics	**MIND** Midwest Institute for Nanoelectronics Discovery
UCLA, UCSB, UCB, UC-Irvine, Stanford, U Denver, Iowa, Portland State, U Nebraska, U Wisconsin	**SUNY-Albany**, GIT, RPI, Harvard, MIT, Purdue, Yale, Columbia, Caltech, NCSU, UVA	**UT-Austin**, UT-Dallas, TX A&M, Rice, ASU, Notre Dame, Maryland, NCSU, Illinois-UC	**Notre Dame**, Purdue, Illinois-UC, Penn State, Michigan, UT-Dallas, Cornell, GIT
Spin devices Spin circuits Benchmarks & metrics Spin Metrology	Novel state-variable devices Fabrication & Self-assembly Modeling & Architecture Theory & Simulation Roadmap Metrology	Logic devices with new state-variables Materials & structures Nanoscale thermal management Interconnect & Arch Nanoscale characterization	Graphene devices: Thermal, Tunnel, & Spin Interband Tunnel Devices NanoMagnetic Logic Non-equilibrium Systems Model / Measurement Nanoarchitecture

Post CMOS Device Examples

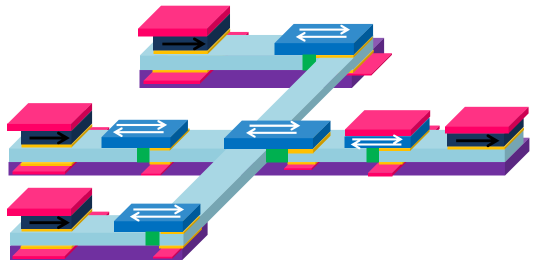
Graphene Bilayer pseudoSpin FET
UT Austin



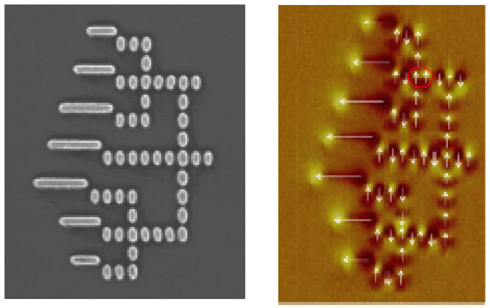
Graphene PN Junction
SUNY Albany



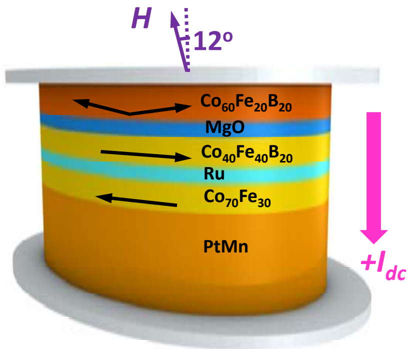
All-Spin Logic
Purdue U.



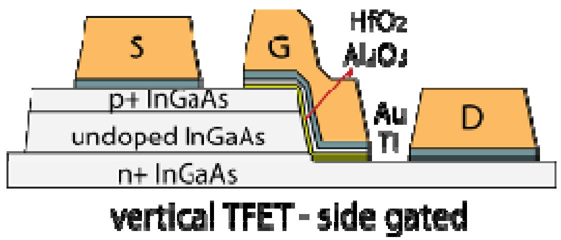
Nanomagnet Logic
Notre Dame, Berkeley



Spin-Torque Device
UCLA



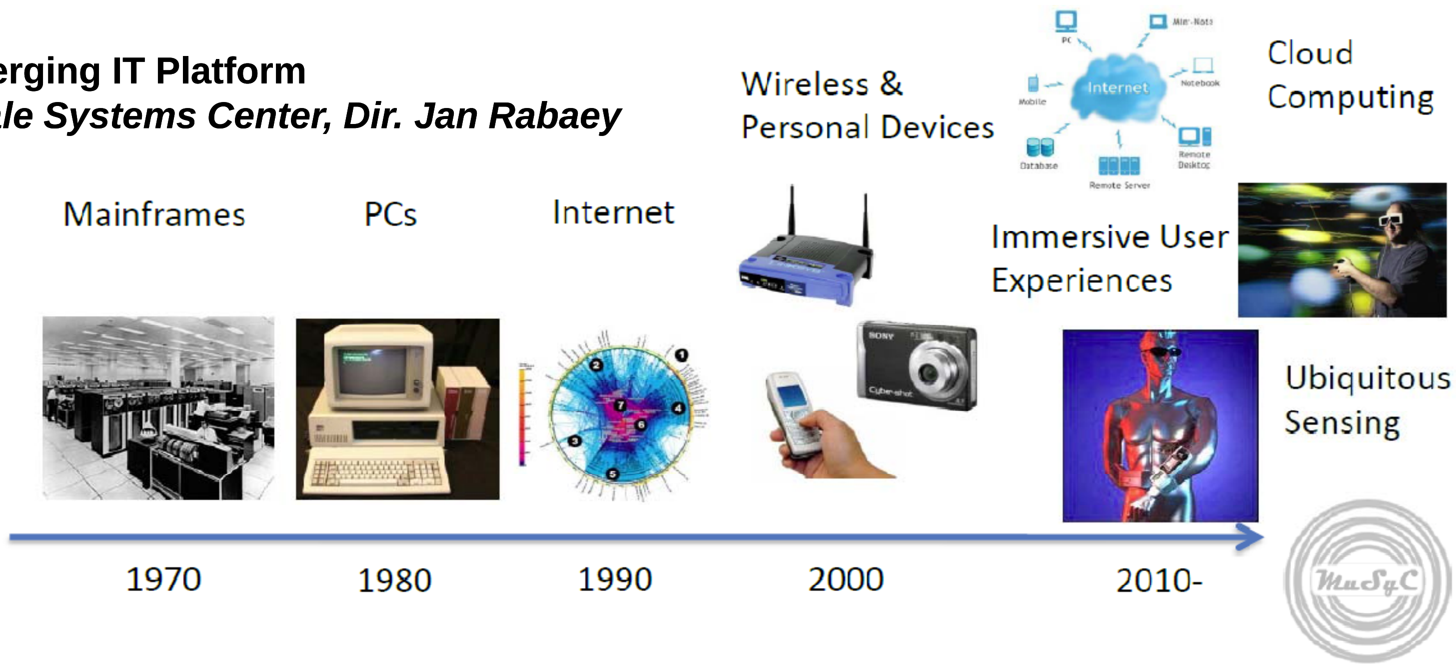
Heterojunction TFET
Penn. State, Notre Dame



Vision Changes in Last Ten Years:
From How to Build → What to Build

- Barrier to future scaling changing from just "how do we make them smaller?" to "how do we reduce their power to make them usable?"
  - Shift from breaking below 100nm Si CMOS to breaking below 10nm
- Discovery of myriad new materials with new physics and properties driving new ideas for device functionality
- Shift from single device focus to circuits and architecture integration
- Increased emphasis on other application areas, beyond logic and memory for Information Technology (IT) infrastructure

The Emerging IT Platform
Multiscale Systems Center, Dir. Jan Rabaey



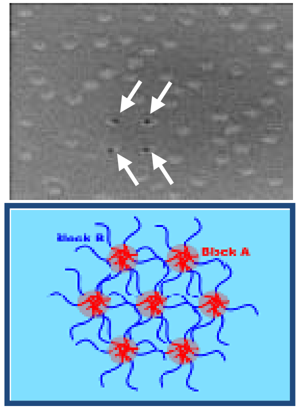
Vision for the Next Ten Years:
Major Directions

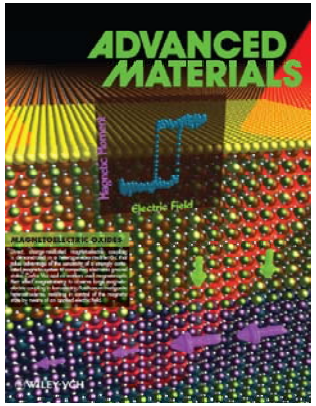
- Increased focus on utilizing new nanoscale physics for device functionality, rather than just fighting it to continue current device scaling
  - Alternate state variables for logic & memory
- Increased focus on architecture and alternative ways to do computation
  - Dealing with lower speeds for lower power: Multi-bit logic? Increased parallelism?
  - Dealing with increased variability: Analog / Statistical / "Almost Right" computation?
  - Tighter integration – and blurring – between memory and logic: Non-volatile transistors, memristors, memory-in-logic, reconfigurable logic, FPGAs
- Increased focus on spin, magnetics, Magnetic Tunnel Junctions – especially spin torque based structures
  - STT-RAM, Nano-oscillators, Magnetic Sensors, Spin Torque MTJ Logic, magnetic cellular automata, reconfigurable arrays
- Increased focus on Carbon based devices
  - Exploiting physics of graphene, carbon nanotubes, fullerenes, defects in diamond
- Increased focus on non-IT applications – future driver of the industry
  - Energy, healthcare, sensors everywhere, always-on connectivity, mobile devices

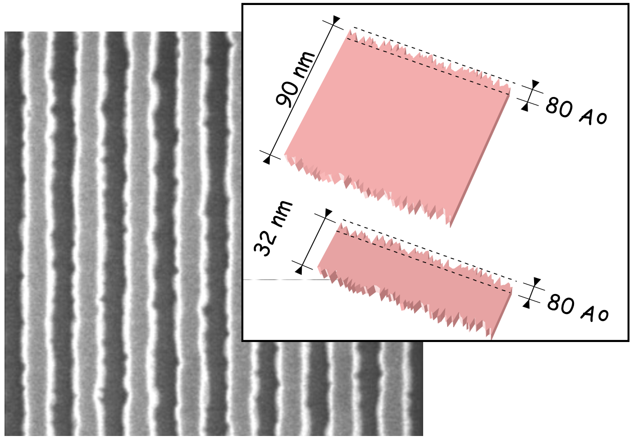
Goals for 2020:
Fabrication

- Achieve 3D near-atomic-level control of reduced-dimensional materials
  - Includes mono-layer growth, nano wire/tube/dot growth and placement, custom materials (e.g. complex metal oxides, multiferroics), and meta-materials (e.g. ferroelectric lattice with embedded ferromagnetic particles)

- Combine lithography and self-assembly to pattern semi-arbitrary structures down to 1nm precision
  - Requires both top-down control of litho for ~10nm-scale arbitrary structures, and bottoms-up control of self-assembly of 1nm-scale regular structures, plus improved inter-layer registration







- Requires continued advances in:
  - Tools for growth, etching and placement at near-atomic levels
  - Chemistries for self-assembly
  - Metrology tools, including in-situ, dynamic characterization & in-line, non-invasive monitoring
  - Predictive modeling of materials and interfaces from atomic level up

Goals for 2020:
Devices

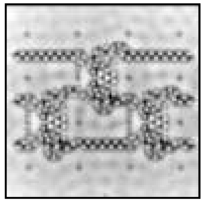
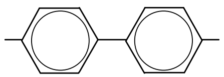
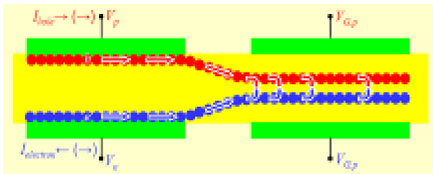
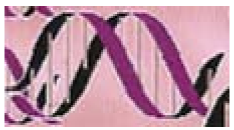
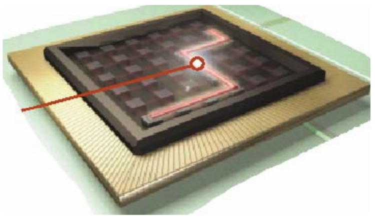
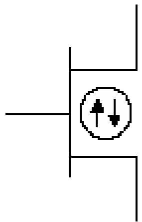
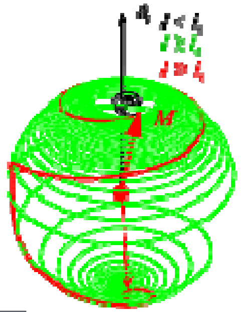
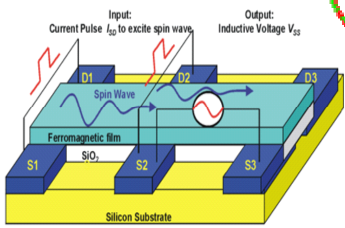
- Discover devices for logic and memory that operate with greatly reduced energy dissipation: 10,000kT → ~10kT
  - Power density is the primary limiter of future scaling. Requires:

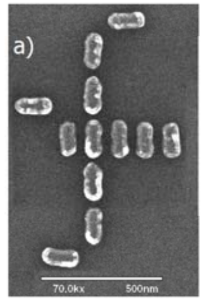
    A device with a lower energy, room temperature switching mechanism

    and/or

    A system that operates out of equilibrium or recovers operation energy as part of the logic computation

- Exploit spin for memory, logic, and new functionality
  - Spin and nano-magnetics offer unique attributes (non-volatility, precession, low power, spin-spin interaction) already utilized in memory and storage
  - New materials and nano-scale control should enable logic, solid state quantum computing, oscillators, sensors, and other functionality

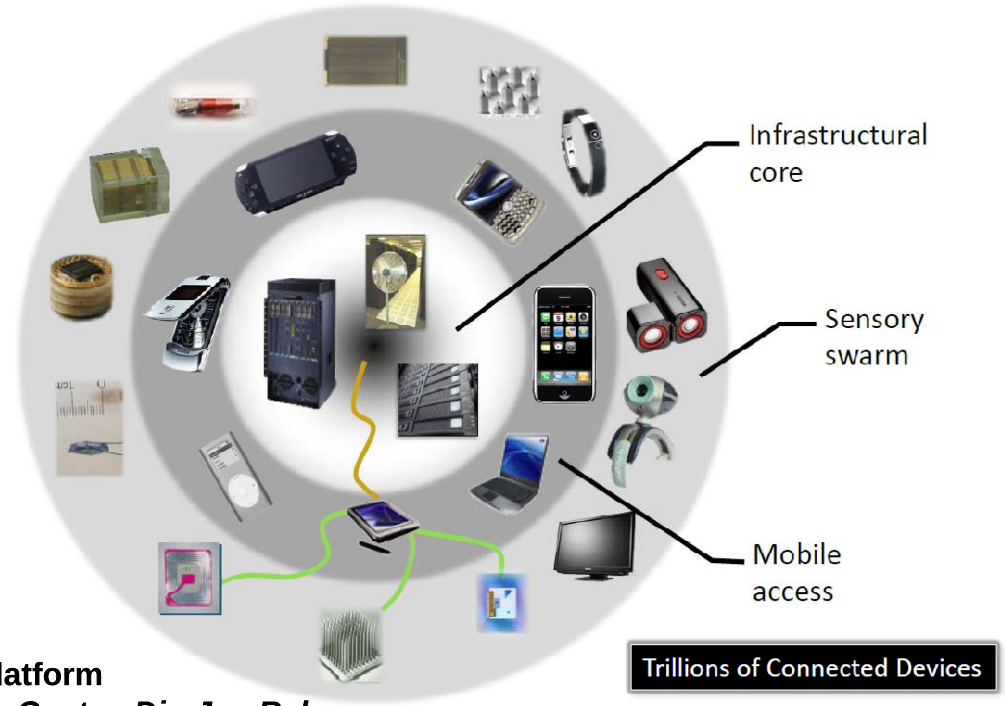











- Challenges:
  - Finding appropriate architectures and state variables (spin, charge, collective effects, etc.)
  - Maintaining speed, noise robustness, signal strength, gain/drive

Goals for 2020: *Architectures*

- Integrate architecture and nanoscale device research for unique computation functionality
- Increase focus on emerging, non-IT applications
  - Previous research has focused on the device first, but most challenges are in the large-scale integration of any new device
  - Energy, healthcare, security, communications, sensors, flexible electronics all drive different needs at device and architecture level
  - Drives need for interdisciplinary teams – materials, chem/bio/physics, engineering, circuit design – working together on basic research driven by the application



The Emerging IT Platform
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International Perspective
Insights from the EU and Asia Workshops

- International workshops reinforced the primary goals, and added additional emphasis in complementary areas
  - Potential to work together on common themes and build off each other's work
- EU Workshop, Hamburg, Germany (C. Sotomayor Torres, J. Welser)
  - Increased emphasis on "More-than-Moore" applications of nanoelectronics, particularly in analog devices, to enhance functionality
  - Strong focus on basic science research to discover new phenomena
- Japan-Korea-Taiwan Workshop, Tsukuba, Japan (M.-H. Hong, S. Wolf)
  - Also emphasized "More-than-Moore", but with more focus on exploring novel state variables and materials (e.g. topological insulators, orbitronics, superconductivity, etc.)
  - Strong interest in quantum computing
- Australia-China-India-Singapore, Singapore (A. Wee, S. Wolf)
  - Strong emphasis on full quantum information systems, for computation and communication
  - Increased interest in molecular electronics, as well as heterogeneous materials integration
- All groups emphasized the need for interdisciplinary teaming, focusing on the application as the driver, and continued strong investment in both research and infrastructure for nanoelectronics work

NRI Benchmarking New Switch Technologies
General Observations

Information Token
Spin waves
Spin (Single / Few)
Magnetic Field (Collective Spin)
PseudoSpin
Heat
Excitons
Plasmons
Charge

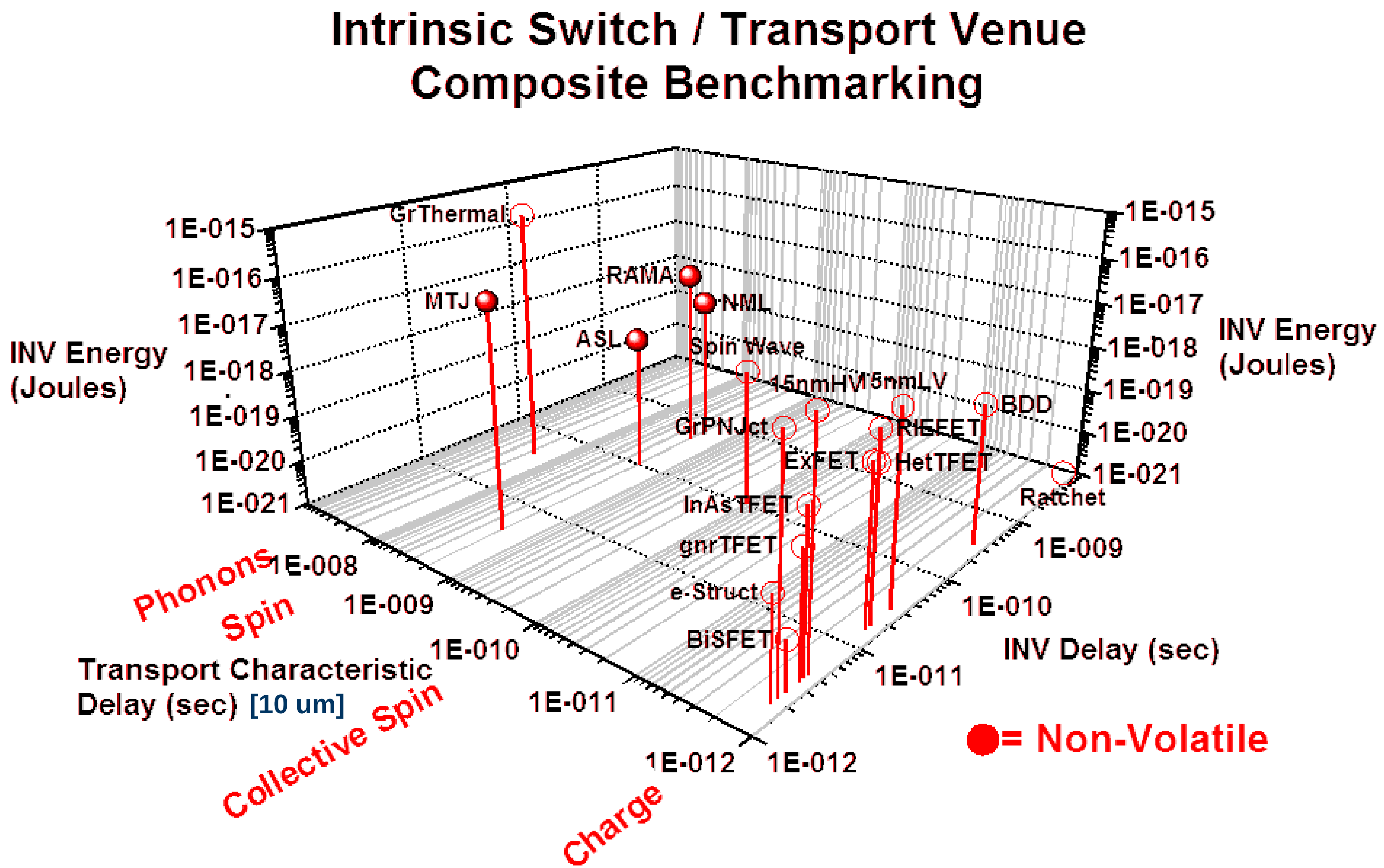
Transport Mechanism
Drift
Diffusion
Ballistic Transport
Spin Conduction
Electromagnetic Waves
Simple Conduction Band Transport
EM quasi-particle in surface plasmon-polariton mode

- Maturing of devices over the past year; more understanding of intrinsic responses
- Substantial clustering of data across multiple tokens
- Token transfer (interconnect) becoming even more important
  - Can influence relative device value
- NRI Architecture results make clear the emerging need for parallelism
  - Important for teams to add circuit designers and to consider non-Von Neumann and/or application-specific architectures
  - Positive Sign: Schematics and SPICE now regularly appear in PI reports

- No clear “winner” – but clearer understanding of device capability has emerged
  - Primary advantages: Power, Area; Primary challenges: Speed
- Increased focus on circuit implementations to take advantage of novel device attributes (e.g. non-volatility, complex functions) required
  - Will continue to refine benchmark process to include relevant parameters – not eliminating ideas based solely on our current CMOS-based metrics

NRI Benchmarking
Typical Data

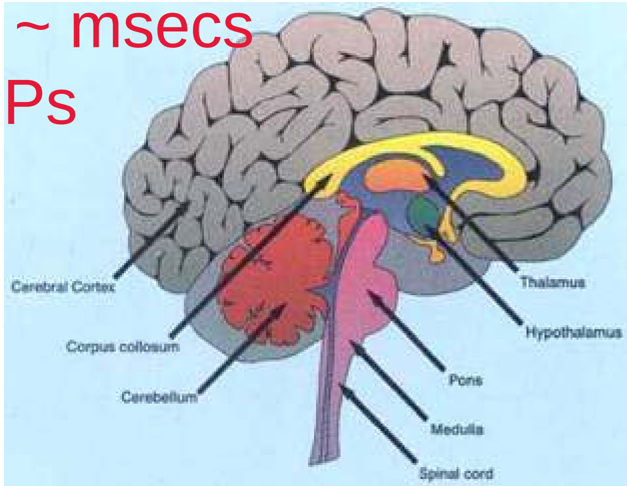
Invited Paper: "Device and Architecture Outlook for Beyond CMOS Switches," K. Bernstein, R.K. Cavin, W. Porod, A. Seabaugh, and J. Welser, *Proceedings of the IEEE Special Issue - Nanoelectronics Research: Beyond CMOS Information Processing,* Vol. 98, No. 12, December 2010.



Computing with Alternate State Variables

- Many different device ideas being considered – some 'likely' attributes compared to CMOS:
  - Slower
  - Denser / 3D
  - Local interconnect focused
  - Uniform arrays / sea-of-gates
  - Variability still an issue

'Switch' ~ msecs
~10^8 MIPs
~30W

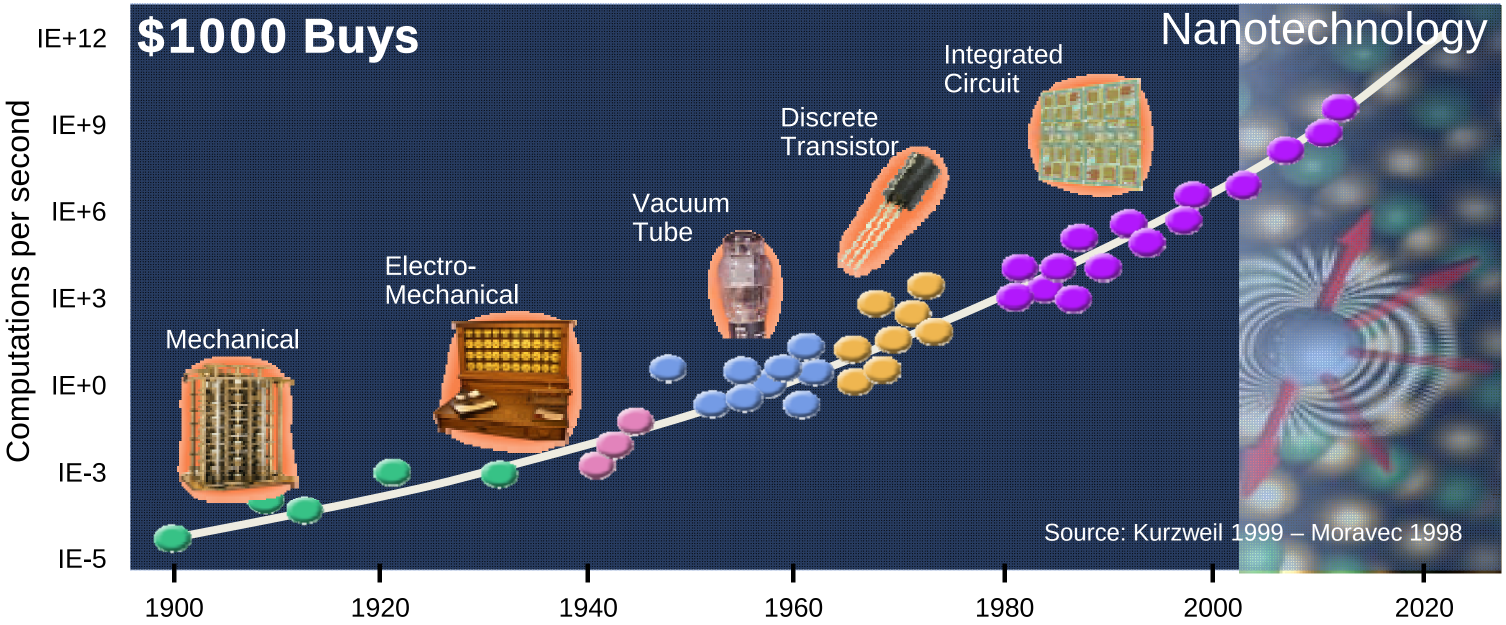


Proof of concept?

- Architecture / System Question:
  - How to get high computation throughput with these attributes?

Nanoelectronics Impact on Society:
To Continue the Benefits, Continue the Curve

- Nanoelectronics plays a major role in tackling most of society's challenges
  - High Performance Computing: behind every major scientific advance
  - Energy: low energy devices, sensors, "smart" appliances & energy grid
  - Bio / Health: in vivo sensors, health monitoring, drug delivery, drug discovery
- Increased proliferation of mobile devices, sensors, and always-on connectivity will alter how we interact with each other and the planet
  - More remote interactions, workforce globalization, remote delivery of services
  - Continued focus on environmental & societal impact of embedded devices
- Microelectronics was THE economic driver for the last half of the 20th century Nanoelectronics is poised to drive the first half of the 21st



Backups

Semiconductor Research Corporation

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SRC®

New & Emerging Research Initiatives

Global Research Collaboration

Ensuring vitality of current industry

Focus Center Research Program

Breaking down barriers to extend CMOS to its limits

Nanoelectronics Research Initiative

Beyond CMOS – identifying next information element

Energy Research Initiative

Emphasis on Photovoltaic and Smart Grid technologies

National Institute for Nano-Engineering

Nano-engineering collaboration with Sandia

Education Alliance

Attracting and educating the next generation of innovators and technology leaders

Nanoelectronics Research Initiative Origins

- 2001-2004: Defining Research Needs
  - ITRS-Emerging Research Device Technical Working Group
  - NSF-SRC Ind-Academia-Govt "Silicon Nanoelectronics and Beyond" Workshops
  - SIA Technology Strategy Committee workshops
  - ➢ *Defined 13 Research Vectors for finding the "next switch"*
  - ➢ *SIA Board passes resolution for formation of NRI*
- Current Member Companies:
- Sep 2005: First NRI and NRI-NSF Solicitations released
- Jan 2006: Research Programs started
- Sep 2007: NIST joins NRI
- NRI partnership model highlighted in as sidebar in the National Nanotechnology Initiative (NNI) Strategic Plan (NNCO, 1/08)
  - Also called out in the House Appropriation Committee report (FY2008)
  - NRI showcased in Small Times' annual nanotechnology university issue