Memristors

J. Grollier

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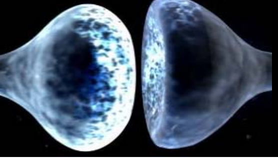
Nanobrain



Memristor

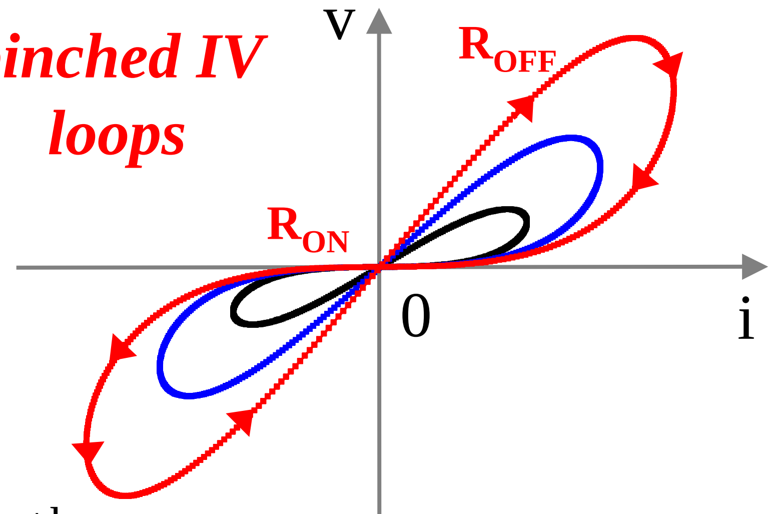
L. O. Chua, "memristor – the missing circuit element" IEEE Trans. Circuit Theory (1971)

$$\boxed{v = M(q)\, i}$$

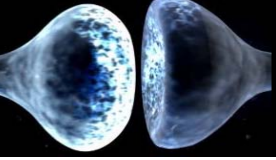
M is a resistance that "remembers" how much current was injected, and how long

continuously tunable between R_{ON} and R_{OFF}

pinched IV loops



M=aq+b



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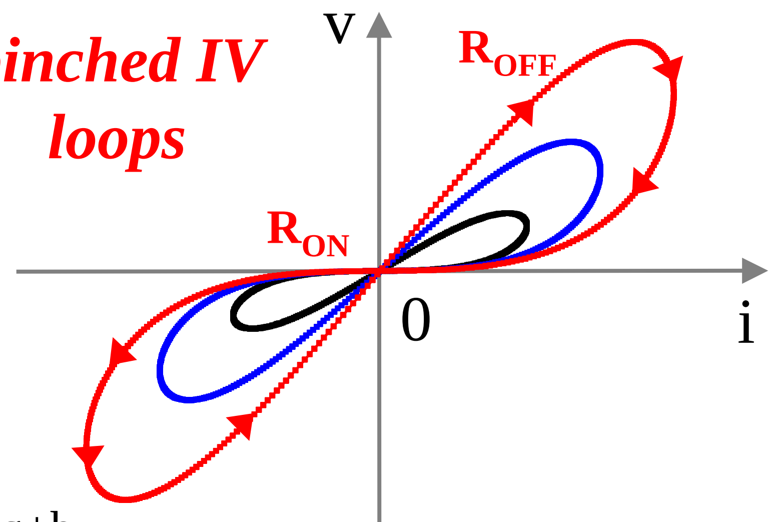
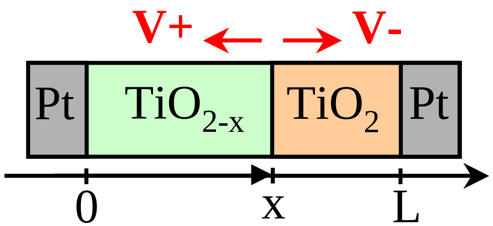


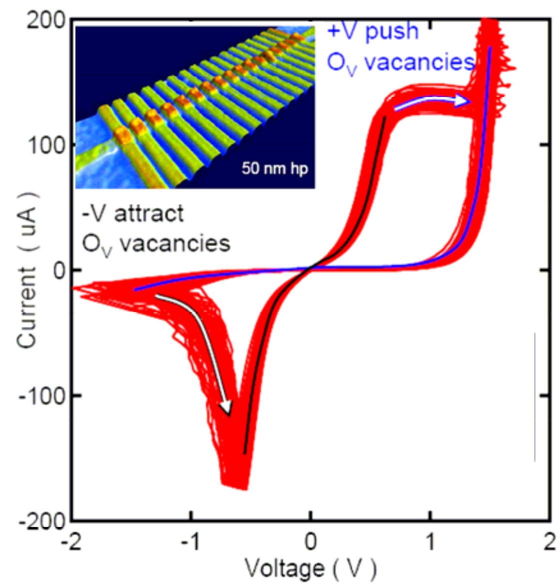
M=aq+b

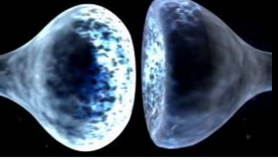
the HP memristor



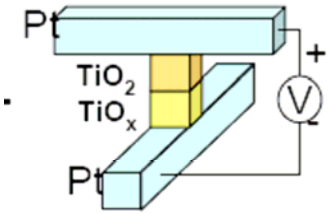
ions electromigration

Yang et al., Nature Nano (2008)



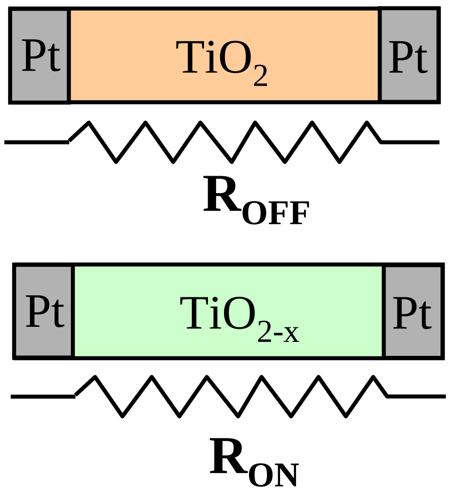


Hewlett-Packard Memristor

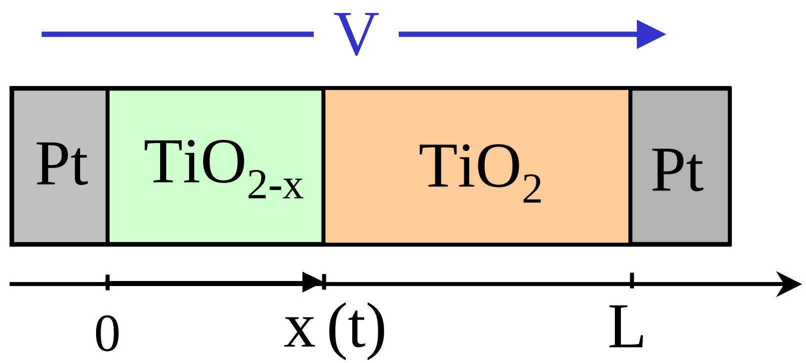


< 30x30 nm^2

$$\frac{R_{OFF}}{R_{ON}} > 1000$$



migration of oxygen vacancies



$$R = R_{ON}\frac{x}{L} + R_{OFF}\left(1 - \frac{x}{L}\right)$$

displacement proportional to the charge

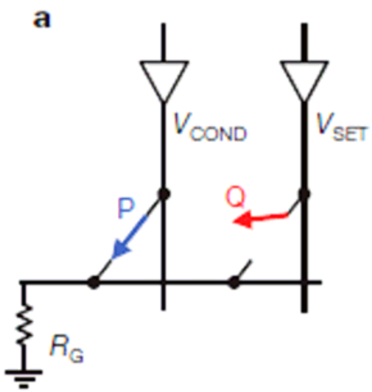
$$\boxed{x \propto q} \Rightarrow \boxed{M(q) \cong R_{OFF}\left[1 - \mu \frac{R_{ON}}{L^2} q\right]}$$

Strukov, Snider, Stewart & Williams, Nature 453 (2008)

Memristor applications

- **non-volatile digital memories**
(R_{OFF}/R_{ON}>1000)

- **logic functions** (no transistors)
  Kuekes et al., JAP 2005
  Borghetti et al., Nature 2010

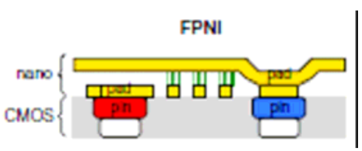


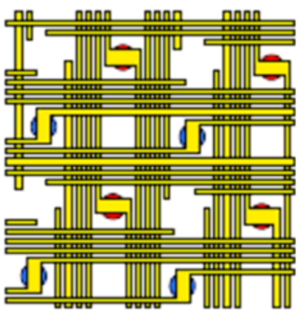
b

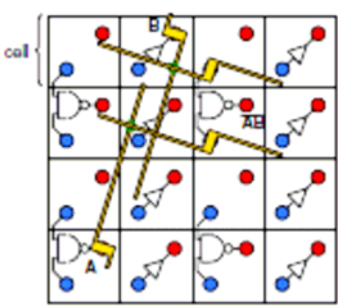
$q' \leftarrow p\mathrm{IMP}q$

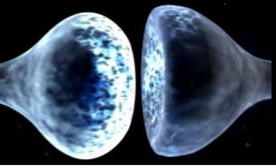
In p	In q	Out q'
0	0	1
0	1	1
1	0	0
1	1	1

- **Reconfigurable Architectures**
 (Field Programmable Gate Arrays)
 Snider et al., Nanotechnology 2007
 Field Programmable
 Nanowire Interconnect









Memristors : artificial synapses

biological synapse : synaptic plasticity

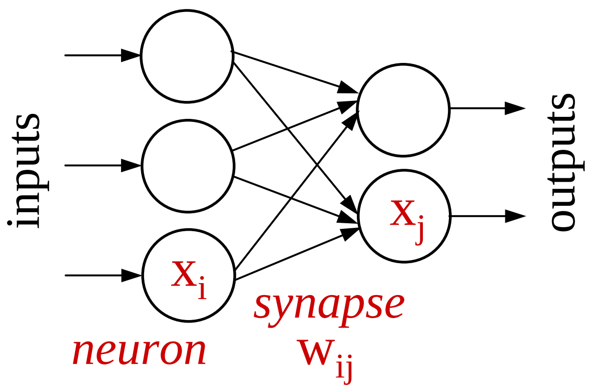
change in strength in response to either use or disuse of transmission

Memristors directly implement the synaptic plasticity

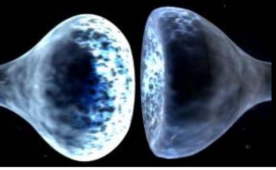
- v = M(q) i
- sub-µm size

key to the development of hardware Artificial Neural Networks

Bio-inspired computing architectures



- w_{ij} : synaptic weights
  - network memory
  - efficiency to transmit information
  - adjustable = **plasticity** = learning
- huge interconnectivity



Von Neumann vs. Neuromorphic computing

- **Human brain**

parallel architecture	analog
10^{11} neurons	10 Hz
10^{15} synapses	20 W

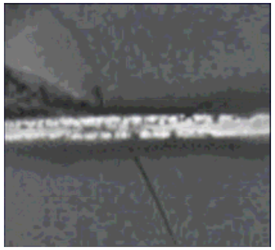
- **Simulations of mouse cortex on Blue Gene L**

Von-Neumann architecture	digital
8.10^{4} neurons	1 GHz
5.10^{10} synapses	40 kW
super-computers slower than mouse ($\times 10$)	

- **Advantages of parallel, analog architecture**

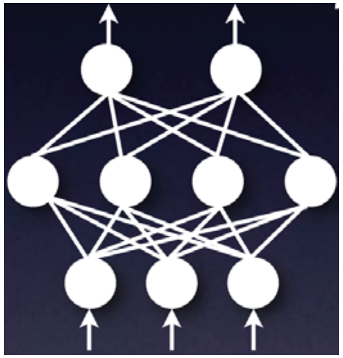
speed, low energy consumption, defect tolerance

Convergence of trends

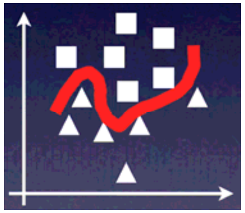


Constraints

Neurobiology

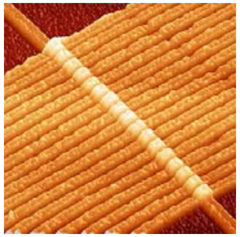


Hardware ANNs



Machine learning

Applications



Nanotechnology

O. Temam, The rebirth of Neural Networks, Proc. ISCA'2010

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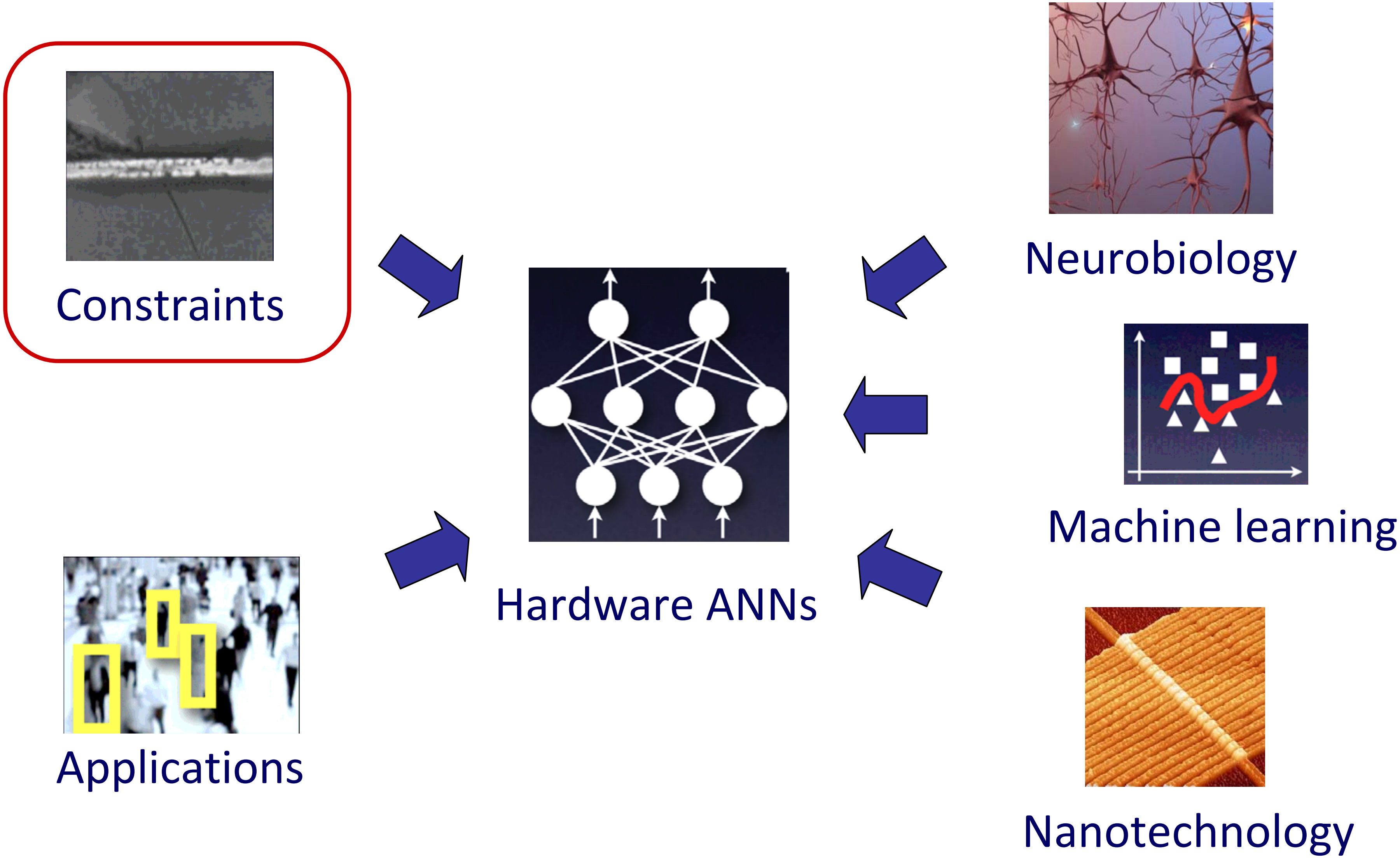

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Convergence of trends

- power limita- -tions : Multi-cores
- defects
- heterogeneous multi-cores

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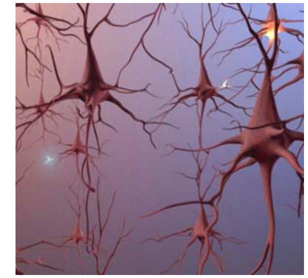

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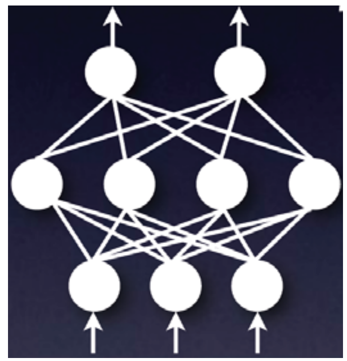

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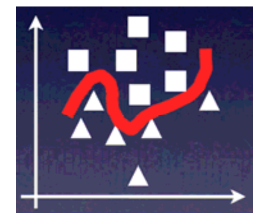

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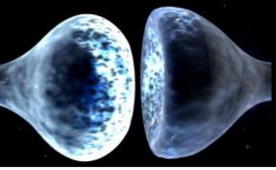

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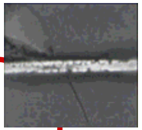

- power limitations : Multi-cores
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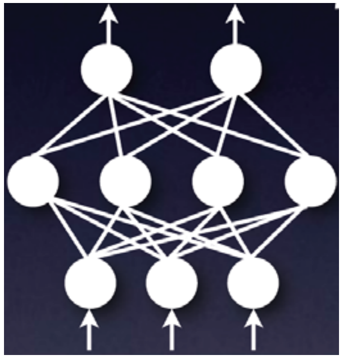

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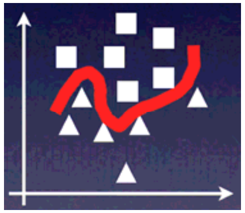

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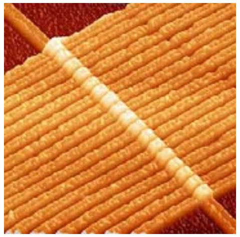

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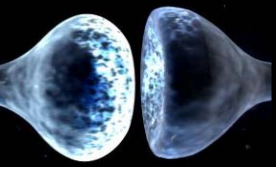

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Constraints

Intel 2005 :

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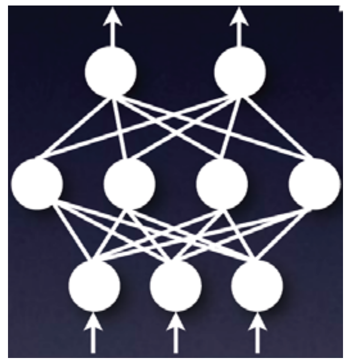

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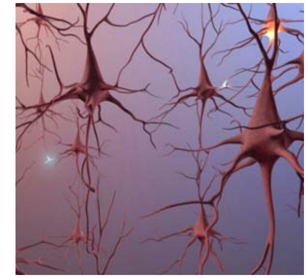

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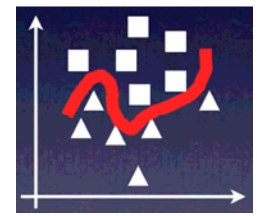

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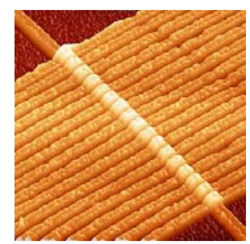

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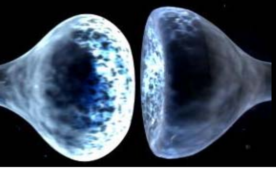

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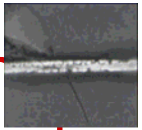

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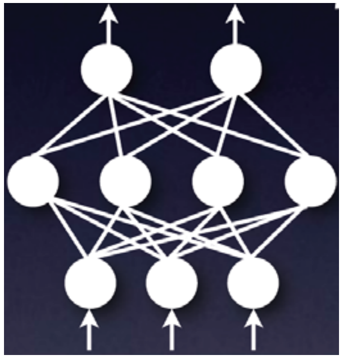

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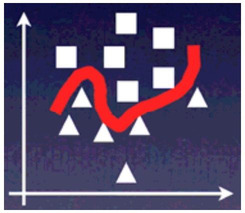

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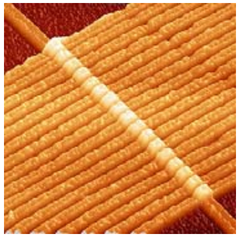

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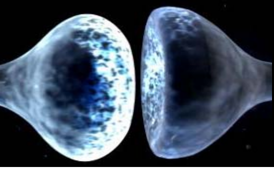

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- brain reverse enginering
- visual cortex ex : T. Poggio

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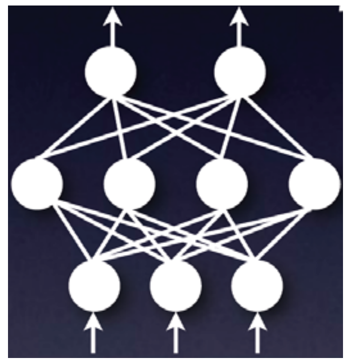

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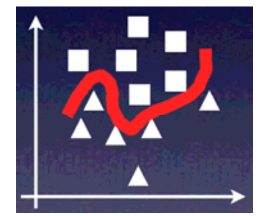

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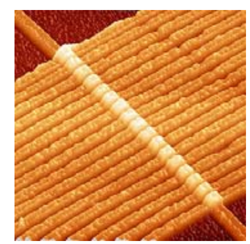

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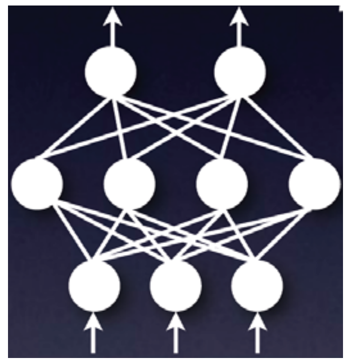

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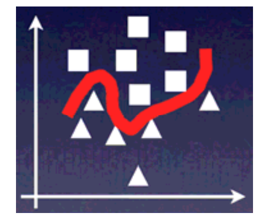

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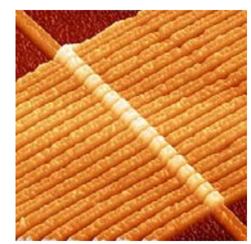

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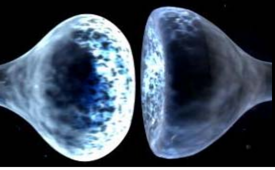

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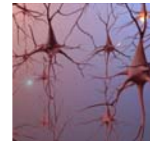

- brain reverse enginering
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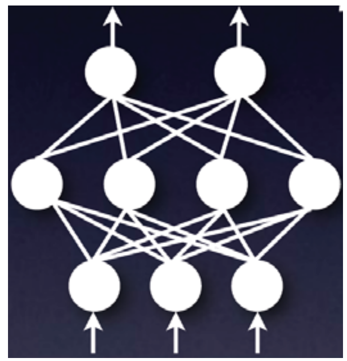
Neurobiology

- deep networks
- powerfull classifiers

Machine learning



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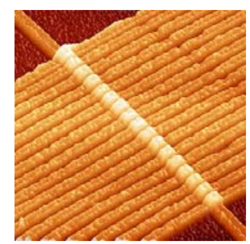

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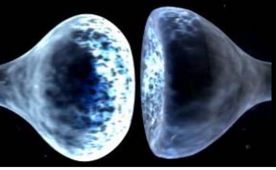

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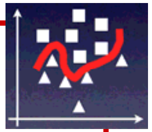

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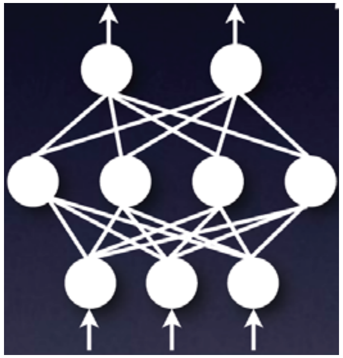

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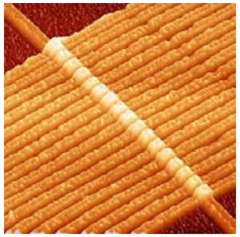

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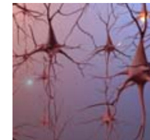

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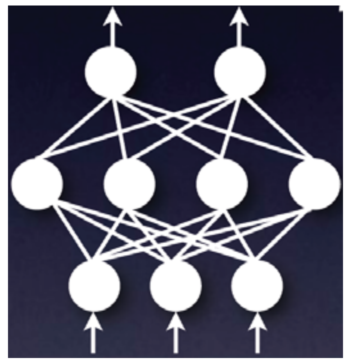

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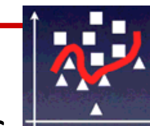

- deep networks
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Machine learning

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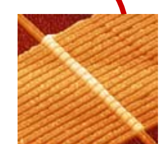
Applications

- 1 memristor = 1 synapse
- 3D stacking
- 10^4 synapses/neuron

Nanotechnology



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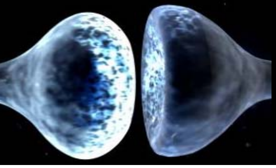
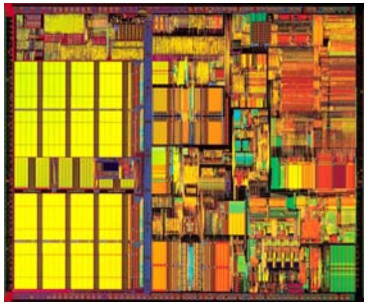


Memristors synapses : applications

• **Hardware ANNs accelerators (heterogenous multi-core, embedded applications)**

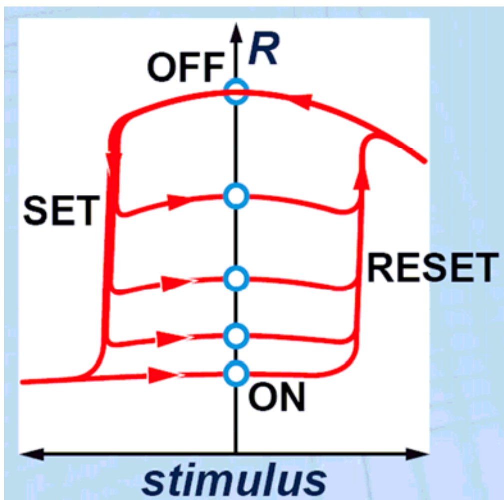


• **Large scale hardware simulations of the human brain ?**

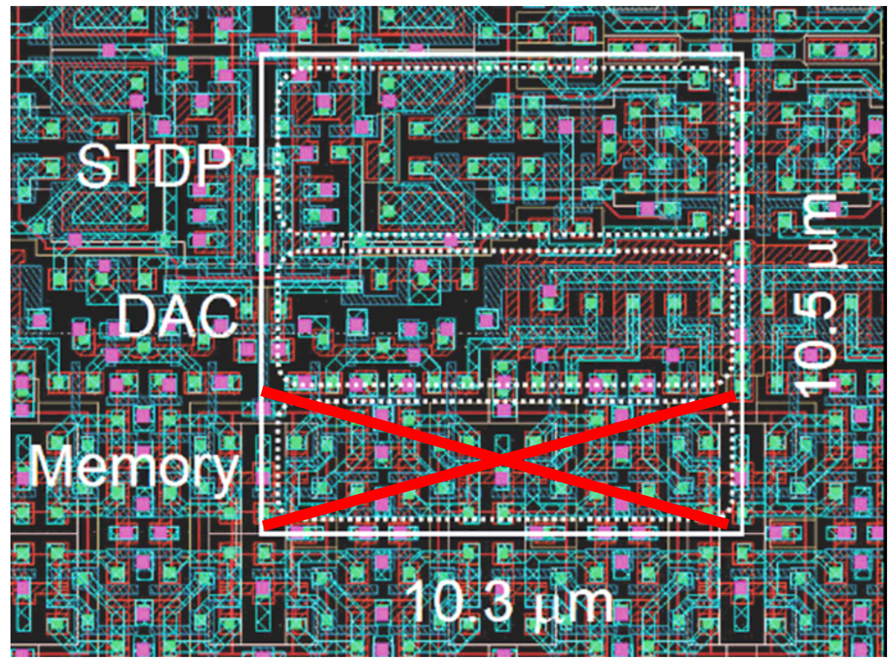
Memristors : artificial synapses

- **Memristors directly store the synaptic weights *(w = conductance)***

Non-volative multi-valued resistances



No need for space consuming SRAM banks



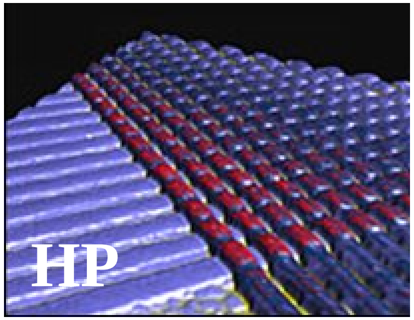
Schemmel *et al.*, IJCNN 2006

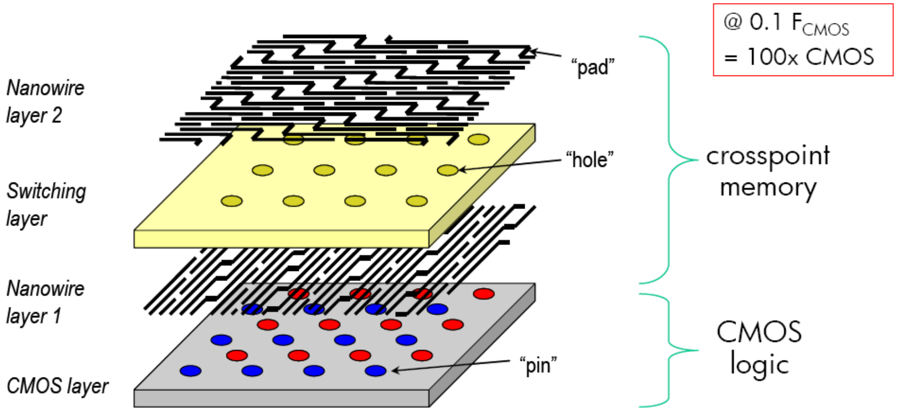
Memristors : artificial synapses

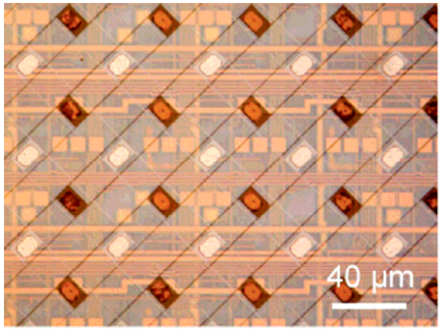
- **Memristors are small *(< 50 x 50 nm^2)***

interconnection issue : about 10^4 synapses per neuron in the brain

ex : CMOS "neurons" + **memristive "synapses"**





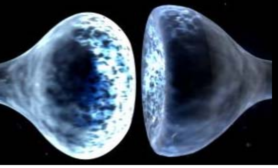


Xia *et al.*, Nanoletters (2010)

memristor crossbar arrays

No demonstration yet of operational mixed memristor/CMOS cognitive chip

to be solved : cross-talk, sneak paths, lithography



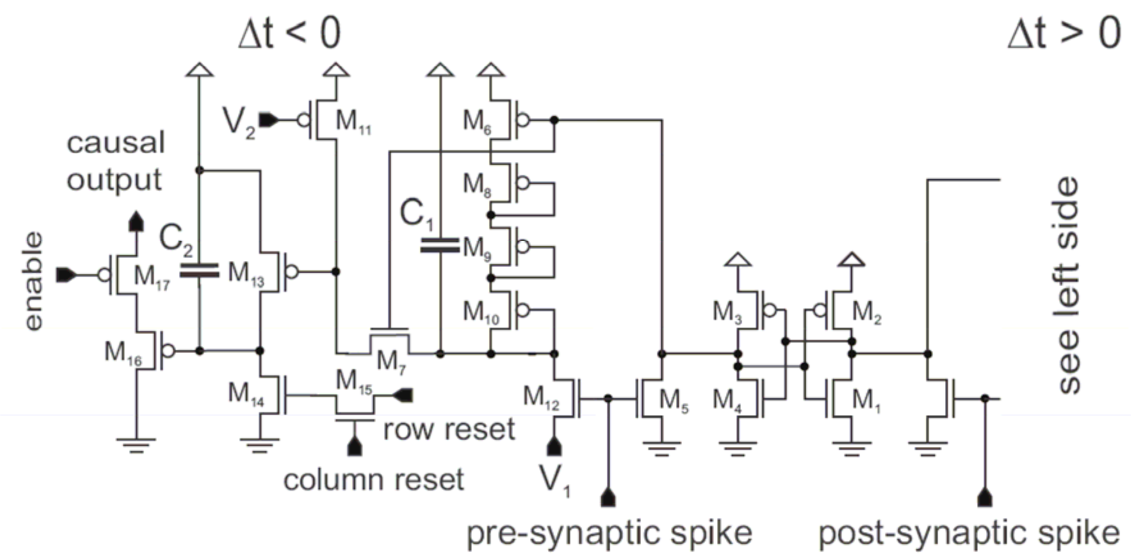
Memristors : artificial synapses

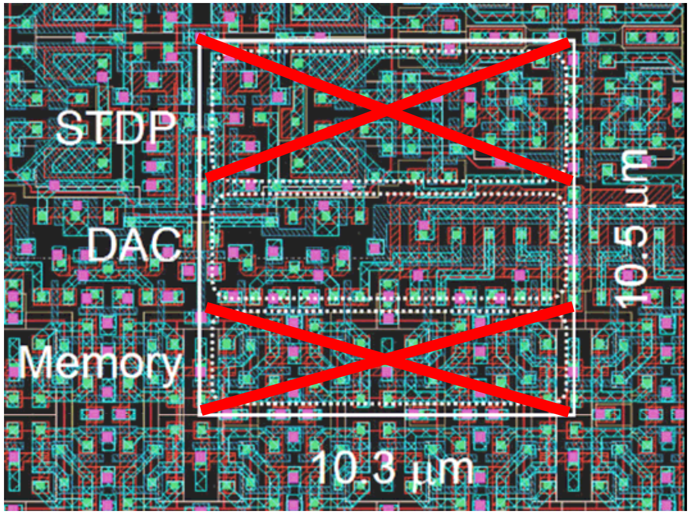
- **Memristors directly implement the synaptic plasticity**

change in strength in response to either use or disuse of transmission

- $v = M(q)\, i$

No need for space consuming complicated CMOS circuits





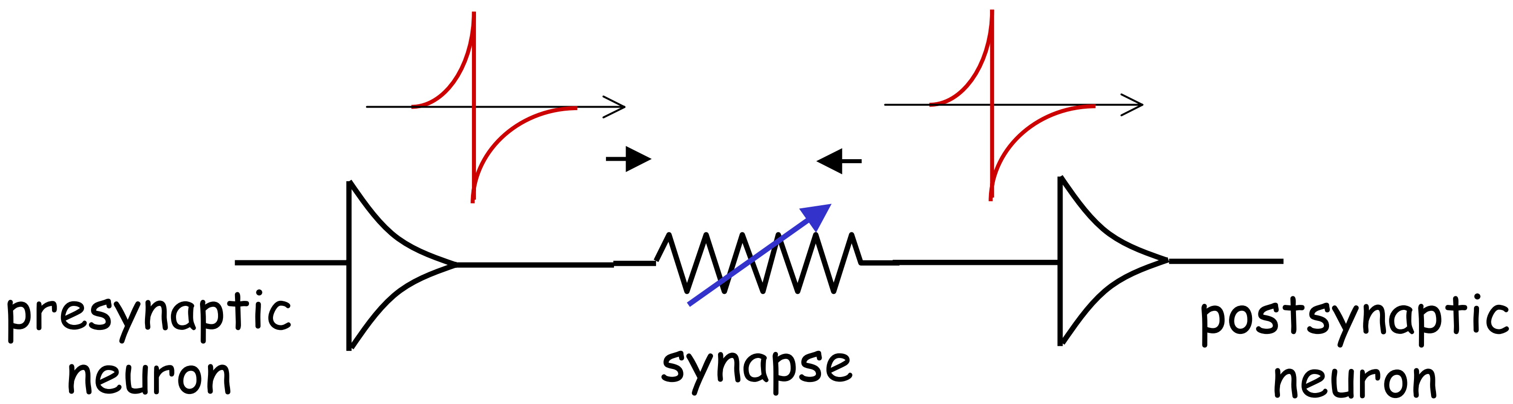
Schemmel *et al.*, IJCNN 2006

Hebbian learning

- **Learning rule :**

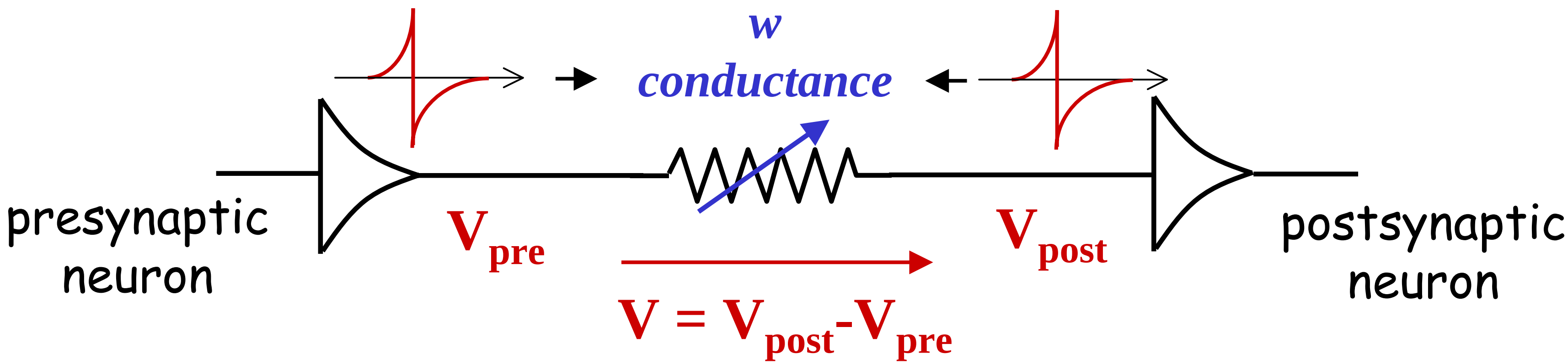
« Neurons that fire together wire together » Hebb, 1949

- **Spike timing dependent plasticity :**



- causality is important:
transmission enhanced if post-neuron fires after pre-neuron
- timing is important :
–ΔT small, large transmission changes

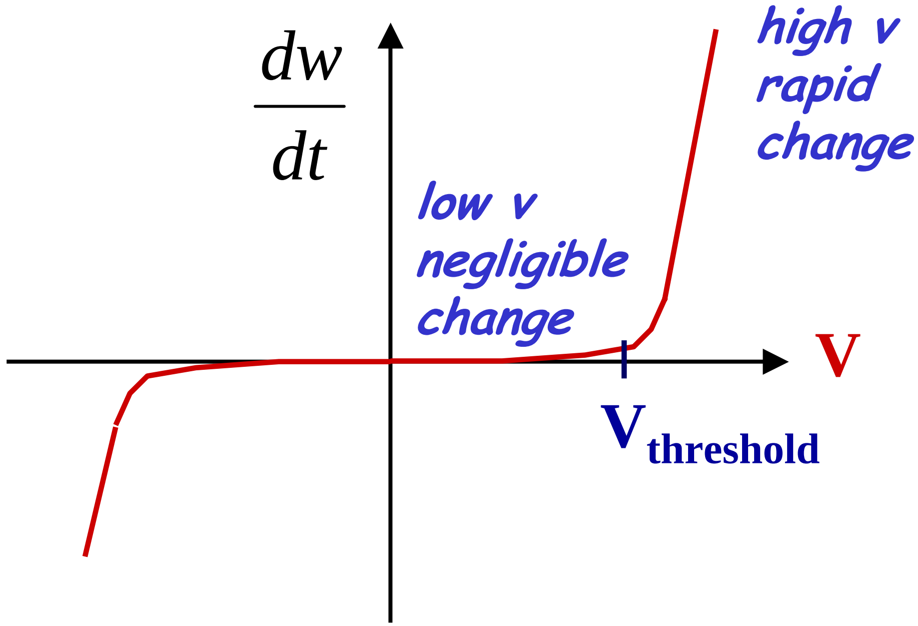
Spike timing dependent plasticity



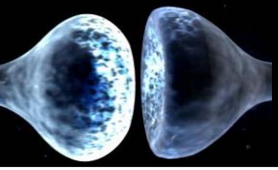
- **change of conductance vs. applied voltage :**

general shape for memristors

enables learning



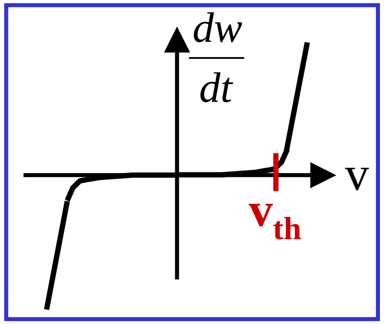
Snider *et al.*, Nanotechnology 2007

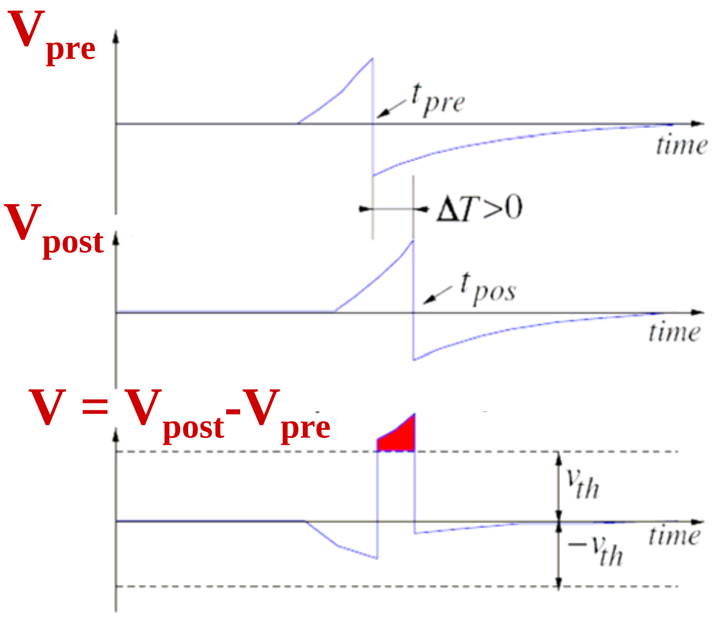


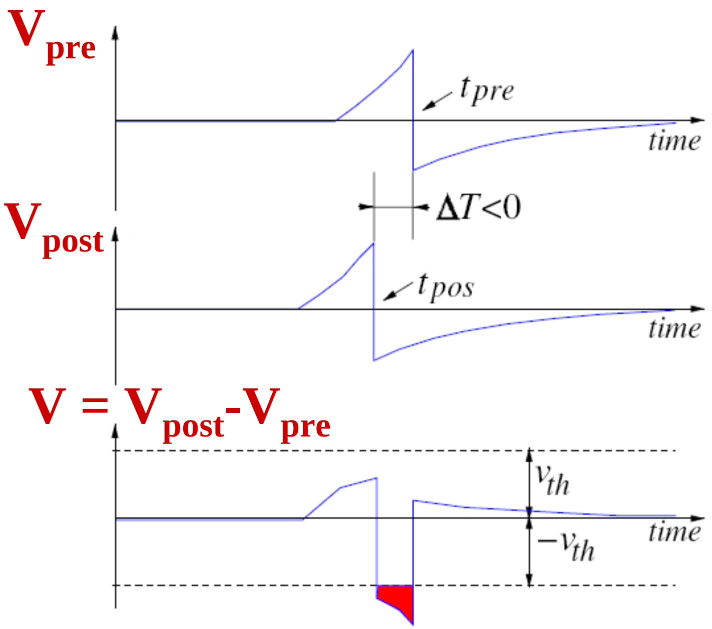
Spike timing dependent plasticity

Memristor change of conductance (synapse weight)

Linarres-Barranco *et al.*, frontiers in Neuroscience, 2011







conductance increase

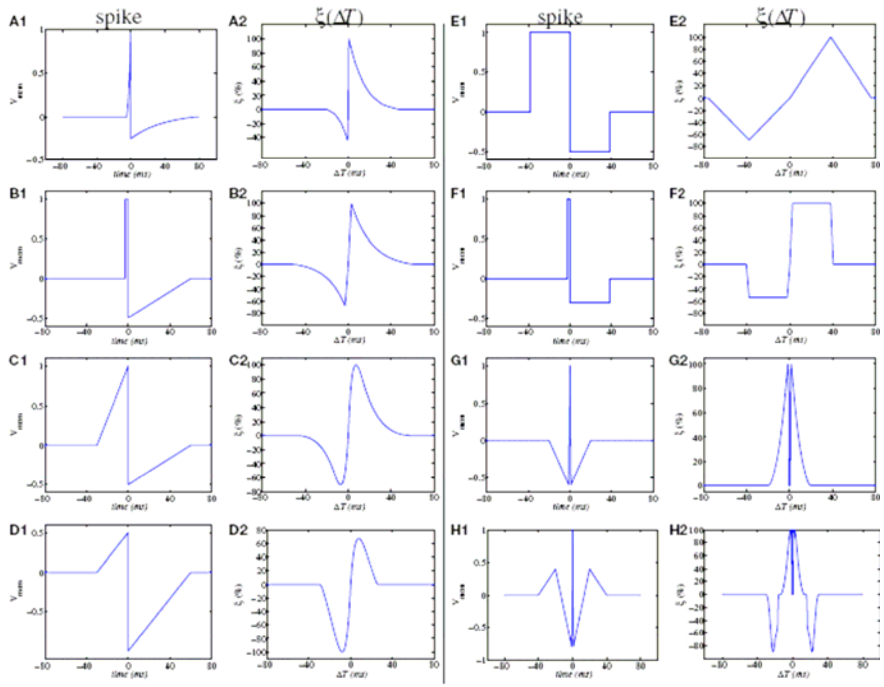
potentiation

conductance decrease

depression

STDP curve vs action potential shape

Linarres-Barranco *et al.*, frontiers in Neuroscience, 2011

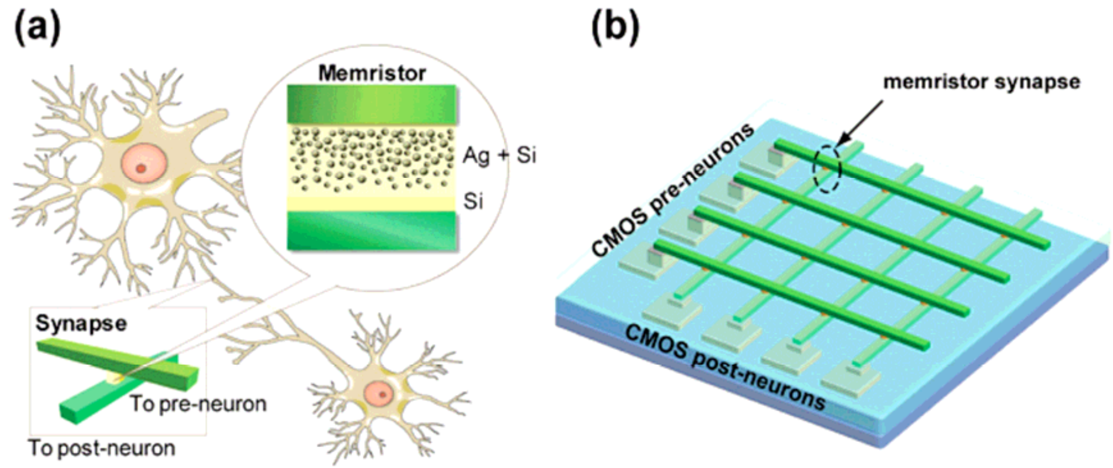


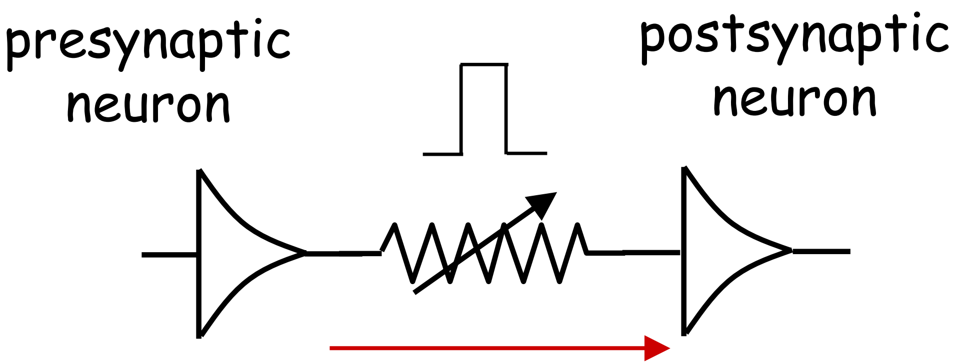
possibility to implement different kinds of STDP with a single device

STDP allows unsupervised learning (image recognition etc.)

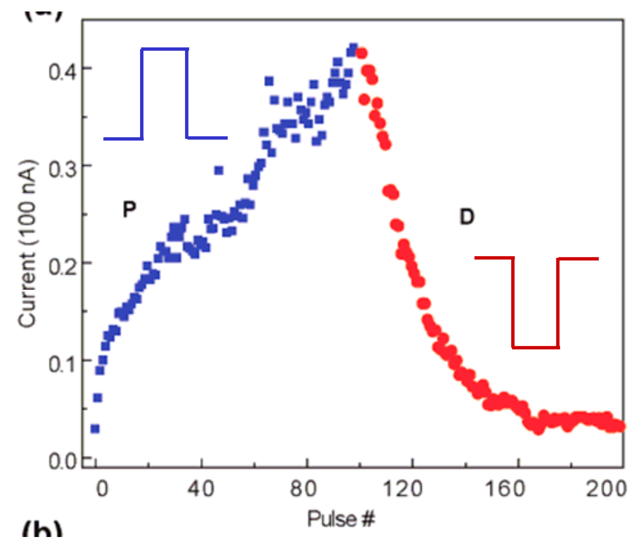
STDP : experimental implementation

Jo *et al.*, Nanoletters 2010



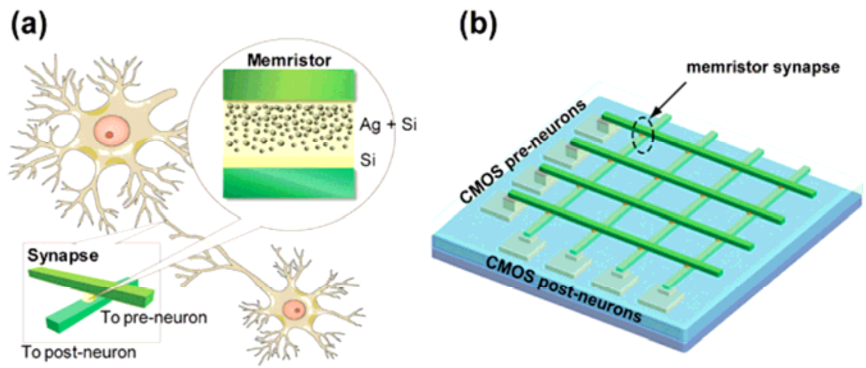


$$V = V_{post} - V_{pre}$$

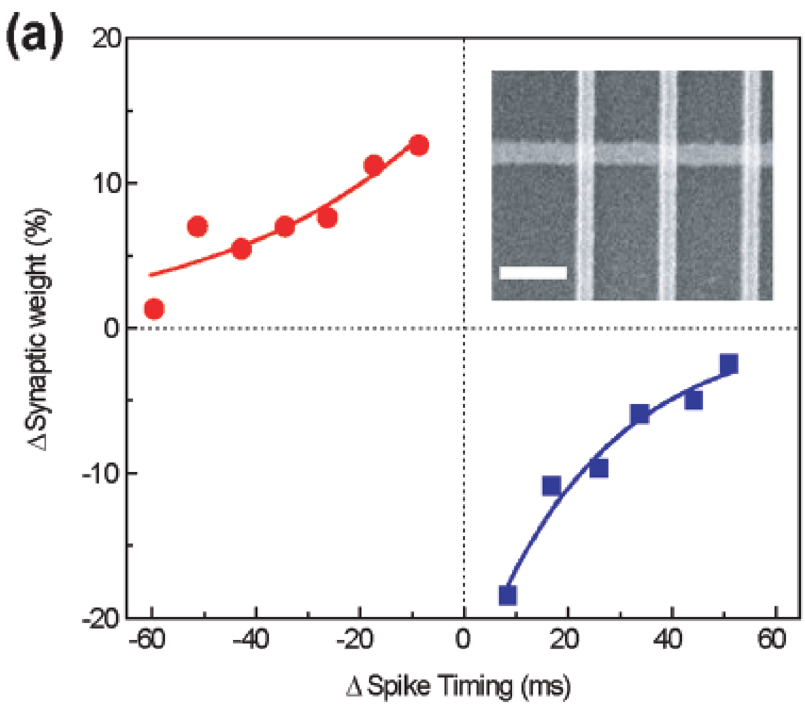


STDP : experimental implementation

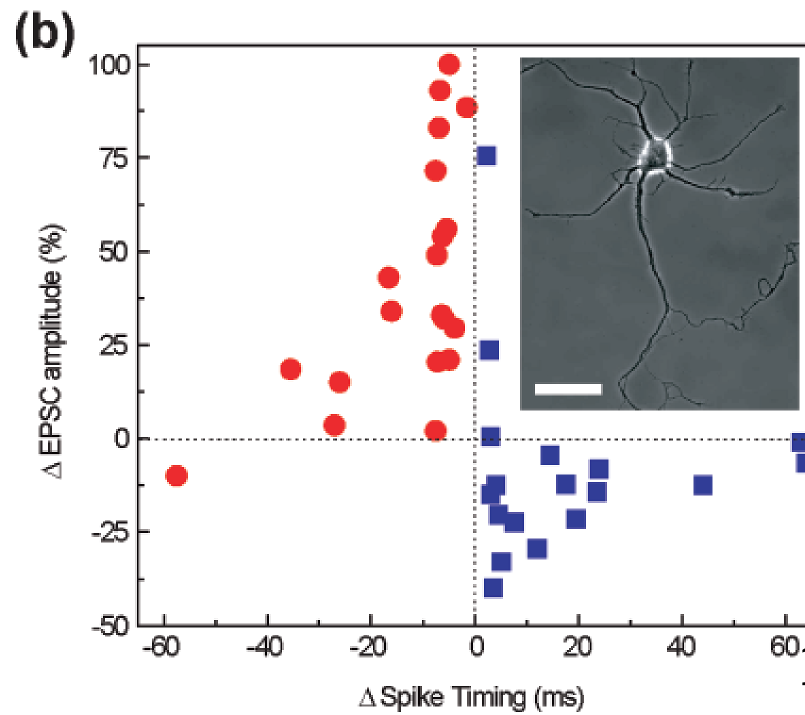
Jo *et al.*, Nanoletters 2010



Memristor STDP curve



Bi & Poo 1998

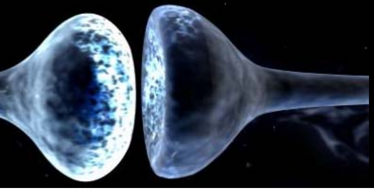


Which memristor ?

After (and even before) Hewlett-Packard TiO_2 memristor was proposed, many other very different memristor concepts were identified :

Erokhin et al., Surface and thin films (2007) PANI
A.A. Zakhidov et al., Organic elec. (2009) metal/mixed conductor/metal
F. Alibart et al., Advanced Func. Mater. (2009) Pentacene + gold particles
Ben Jamaa et al., IEEE Nano (2009) Poly-cristalline Si nanowires
Derycke et al., TNT (2009) Carbone nanotubes
Driscol et al., APL (2009) Phase change material
Gergel et al., IEEE EL (2009) flexible TiO2
Jo et al., Nanoletters (2009) Ag/Si
Wang et al., IEEE EL (2009) spintronics
Kim et al., Nanoletters (2009) nanoparticle assemblies
Jeong et al., Nanoletters (2010) graphene
Lee et al., Nature Materials (2011) Ta2O5
Ohno et al., Nature Materials (2011) atomic switches
Chanthbouala, Grollier et al., Nature Physics (2011) spintronics
….

Classification :
- ***Organic memristors***
- ***Most Resistive Switching memristors***



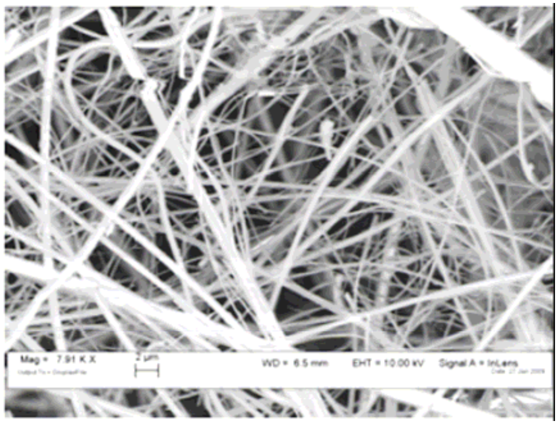
Organic memristors

- ***Organic memristors :*** NOMFET (polymer), CNT-FET, PANI….

- additional functionalities
ex : interaction with light

-bottom up approach
ex : self-organization

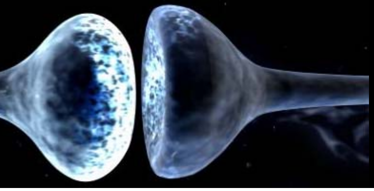
- high density



Erokhin *et al.*, NanoNet 2009

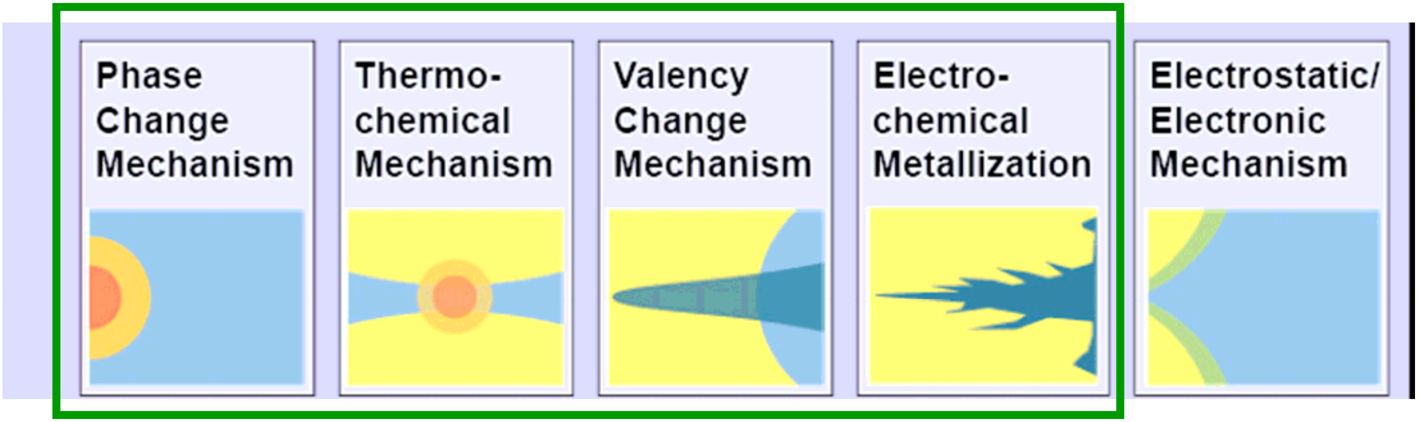
- Very promising
- time scale > 10 years

FP7 Bion & Nabab projects



Resistive switching memristors

“easy” implementation in crossbar arrays – top down approach



Waser *et al.*, Nature Materials 2007

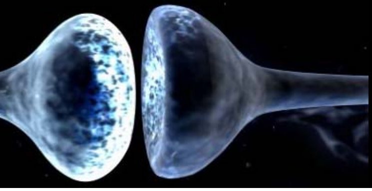
- defect-mediated : thermal effects, ionic motion

Ex : HP memristor based on electromigration : reliability / endurance issues

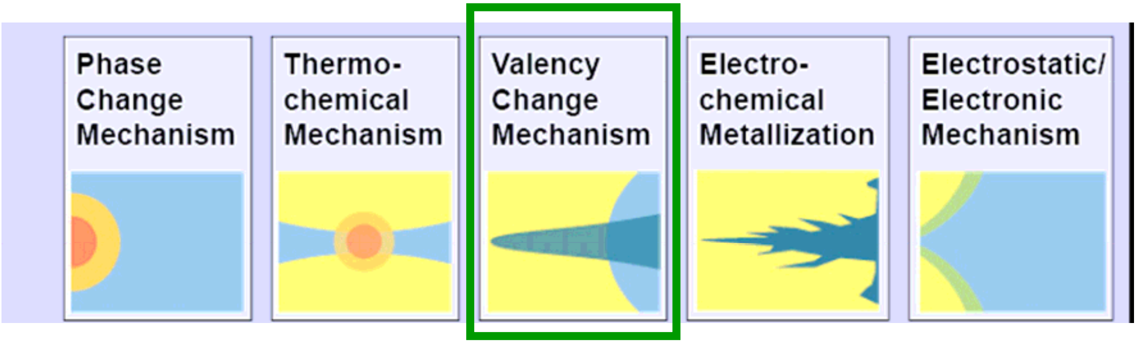
- large local heating   - need of a forming step   - physics not understood

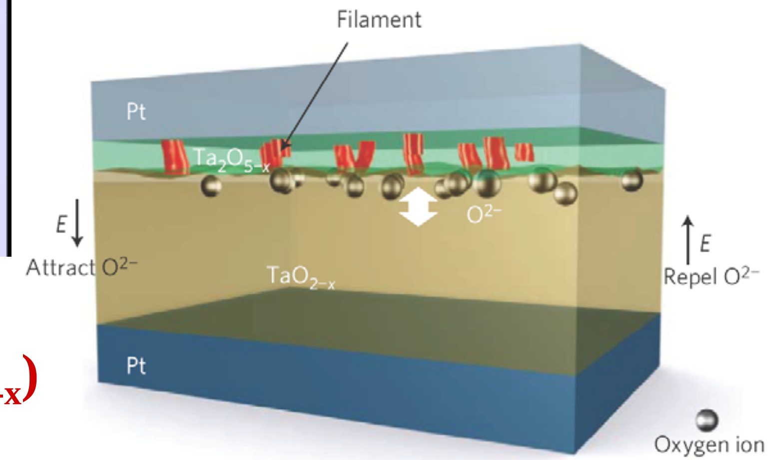
- the most mature existing technology

- Strukov et al., Nature 2008 (TiO2)
- Jo et al., Nanoletters 2010 (Ag/Si, no forming step)

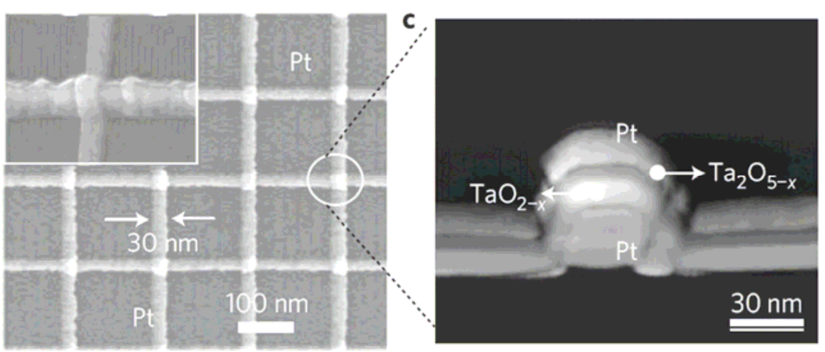


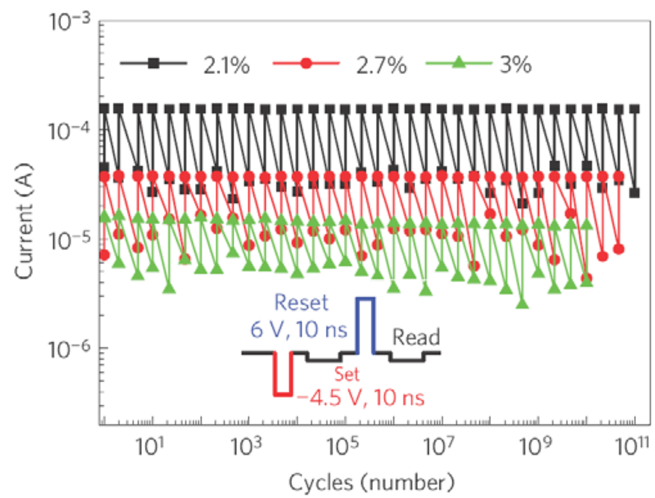
Resistive switching memristors





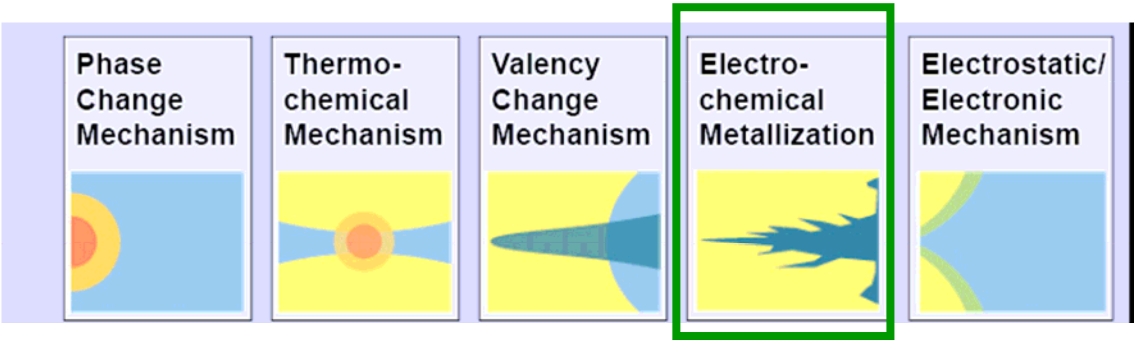
Lee et al., Nature Materials 2011 **(Ta_2O_{5-x}/Ta_{2-x})**

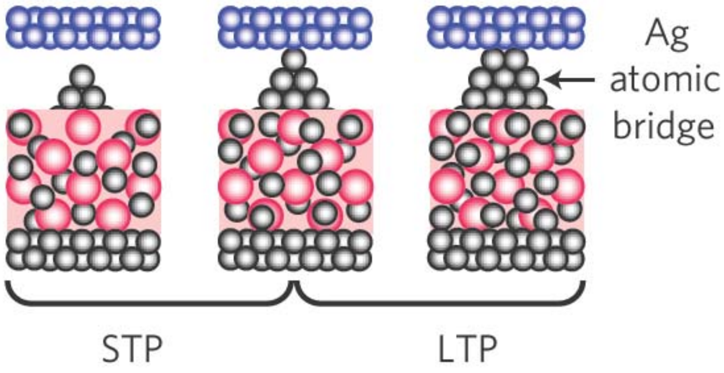




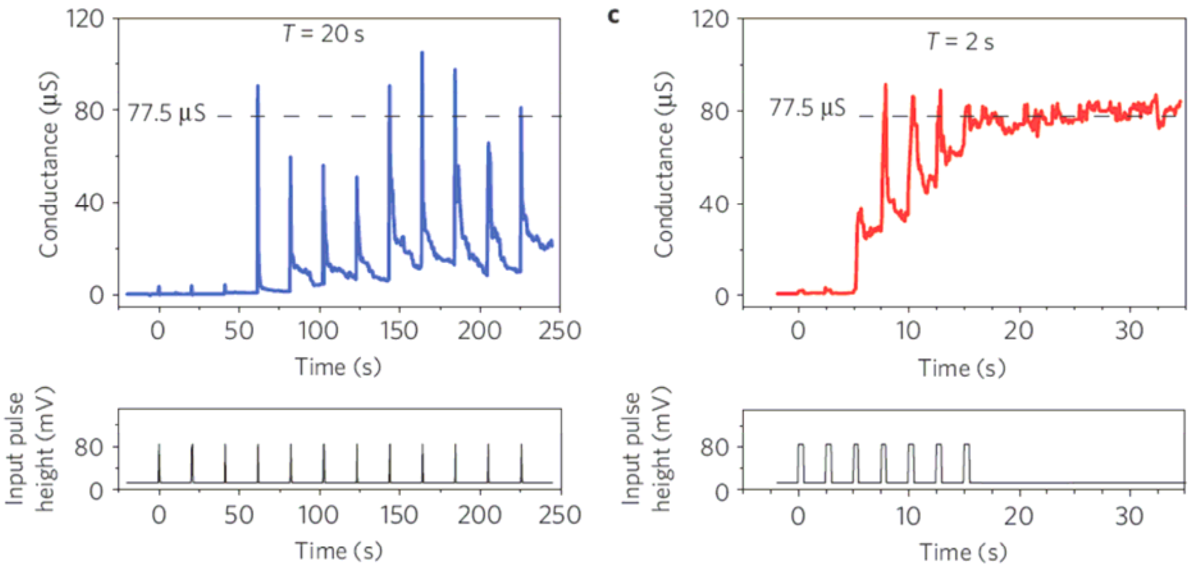
good cyclability > 10^{12}, fast (10ns) and reduced power consumption

Resistive switching memristors

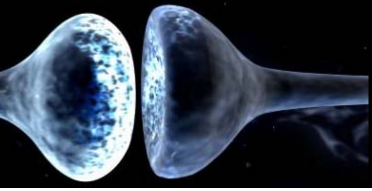




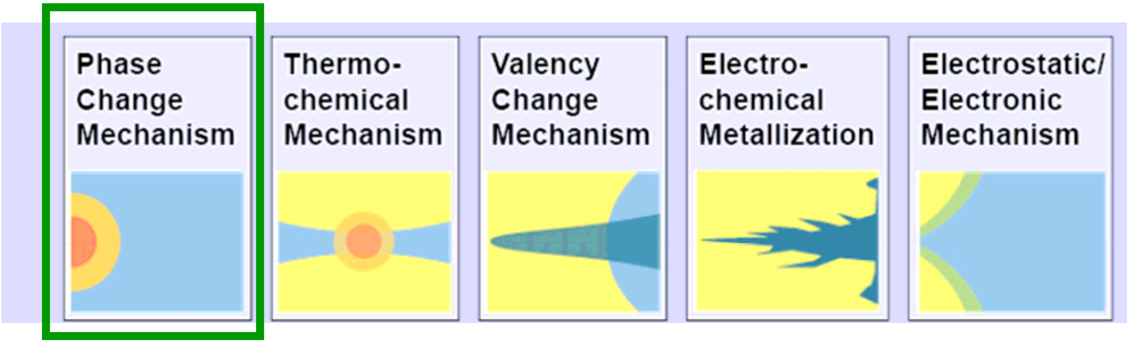
Ohno et al., Nature Materials 2011 (Ag$_2$S atomic switch)

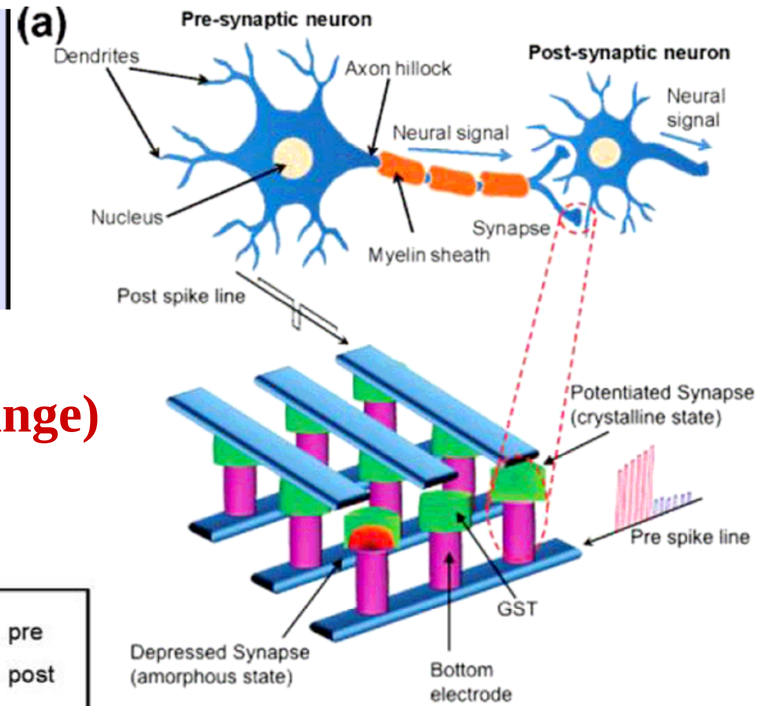


Short AND long term potentiation ! STDP ? Cyclability ?

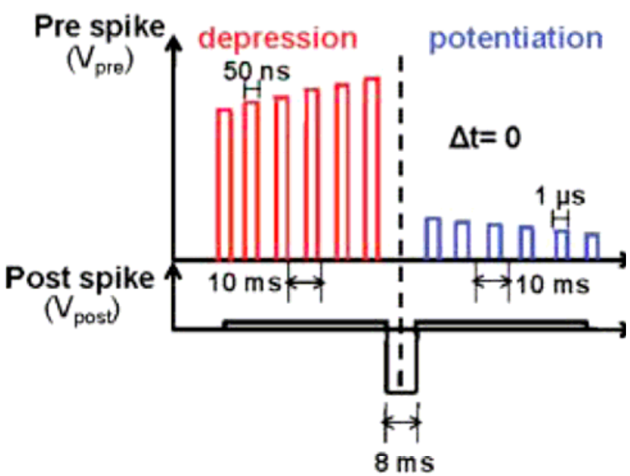


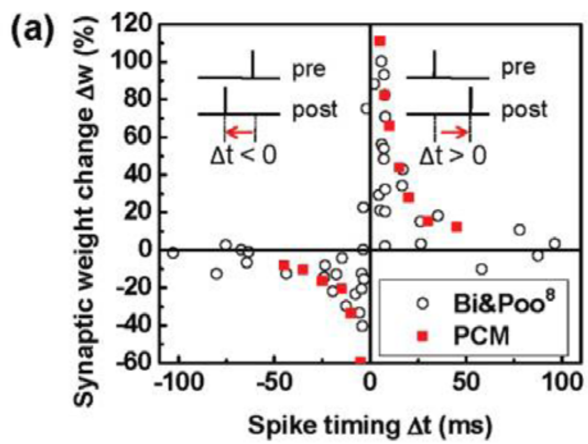
Resistive switching memristors



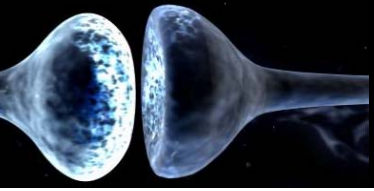


Kuzum et al., Nature Materials 2011 (Phase change)
see also : Wright et al., Advanced Materials 2011

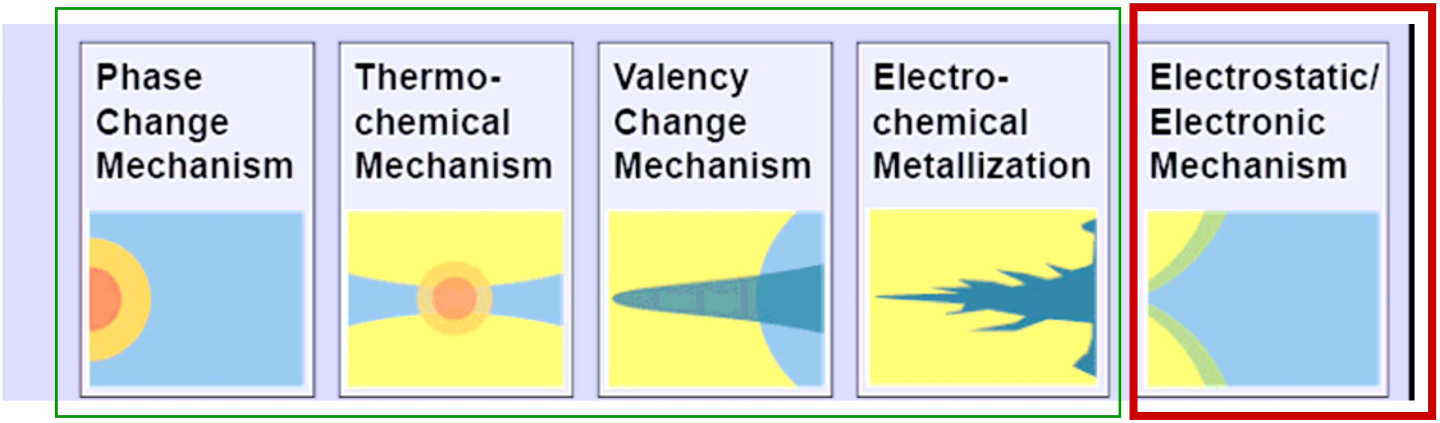




Phase change : unipolar switching. STDP = yes, complicated ?



Resistive switching memristors

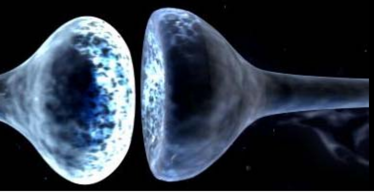


Waser *et al.*, Nature Materials 2007

- *defect-mediated : thermal effects, ionic motion*

- our work : **purely electronic resistive switching**

  1 example : "spintronic" memristor *WO 2010/ 142762 A1*



Spintronic memristor

A. Chanthbouala, J. Grollier, R. Matsumoto, V. Cros, A. Anane, A. V. Khvalkovskiy, A. Fert

Unité Mixte de Physique CNRS/Thales, France

K.A. Zvezdin

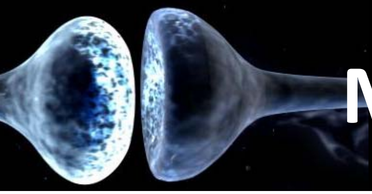
A.M. Prokhorov General Physics Institute of RAS, Russia
Istituto P.M. s.r.l., Italy

K. Nishimura, Y. Nagamine, H. Maehara, K. Tsunekawa

Process Development Center, Canon ANELVA Corporation, Japan

A. Fukushima, and S. Yuasa

National Institute of Advanced Industrial Science and Technology (AIST), Japan



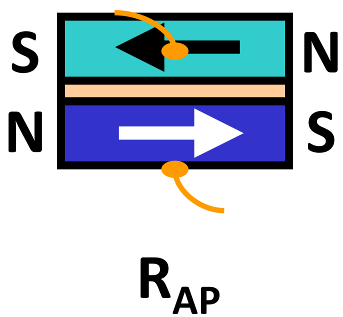
Magnetic Random Access Memory (MRAM)

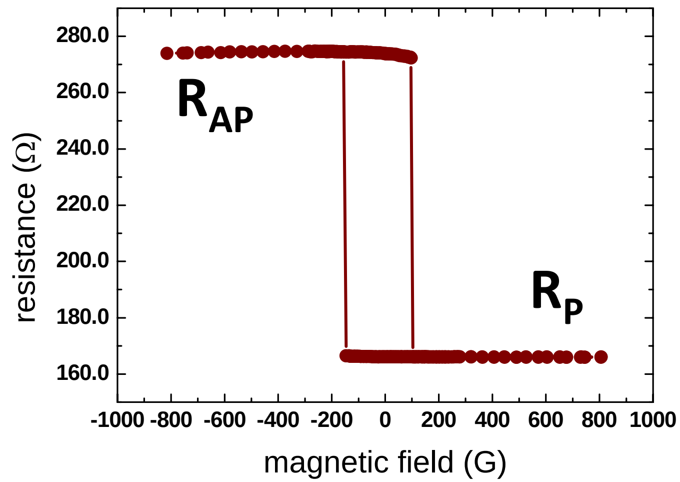
MRAM building block = Magnetic Tunnel Junction

Magnetic metal/Insulator/Magnetic metal

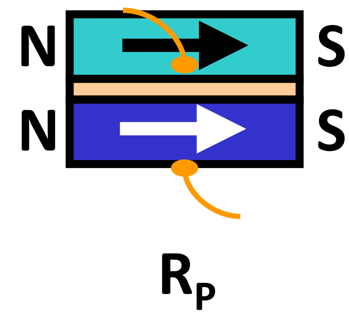
Tunnel MagnetoResistance (TMR)

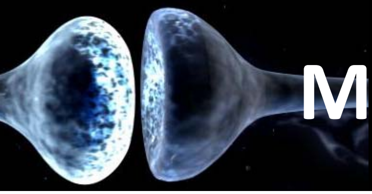
Anti-parallel state (AP)





Parallel state (P)





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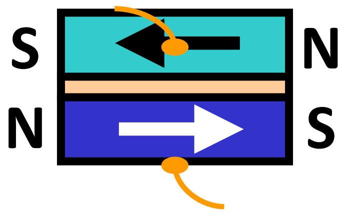
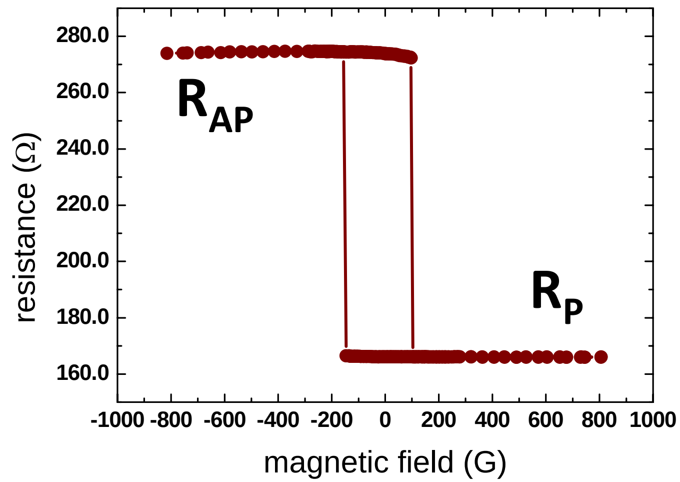
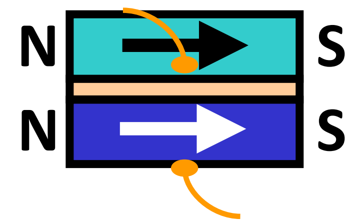


R_{AP}



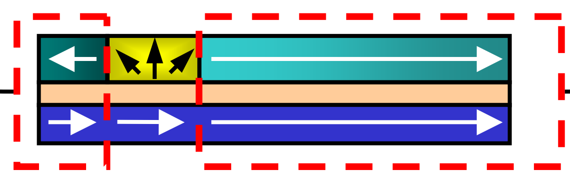
Parallel state (P)



R_P

Domain Wall

Domain $\mathbf{R_{AP}}$



Domain $\mathbf{R_P}$

- Resistance: proportion of parallel and anti-parallel domains

Magnetic Random Access Memory (MRAM)

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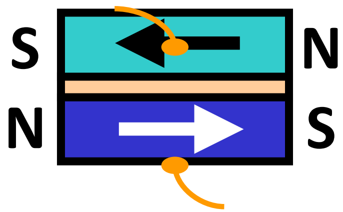
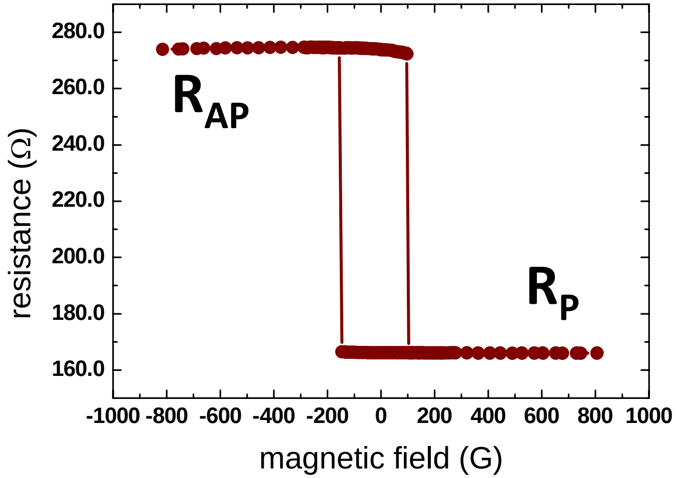
Magnetic metal/Insulator/Magnetic metal

Tunnel MagnetoResistance (TMR)

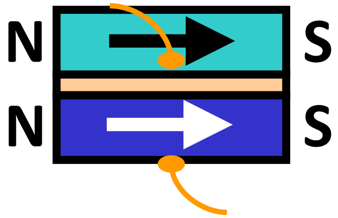
Anti-parallel state (AP)



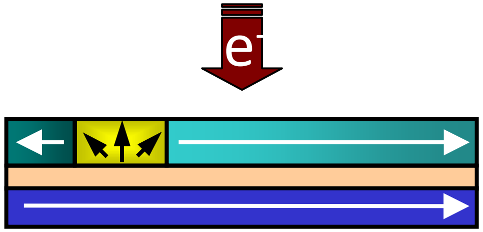
R_{AP}



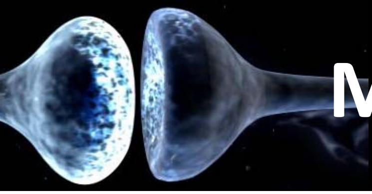
Parallel state (P)



R_P



- Resistance variation: **Spin Transfer Torque (STT)**



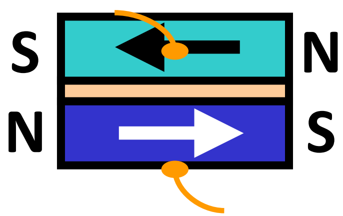
Magnetic Random Access Memory (MRAM)

MRAM building block = Magnetic Tunnel Junction

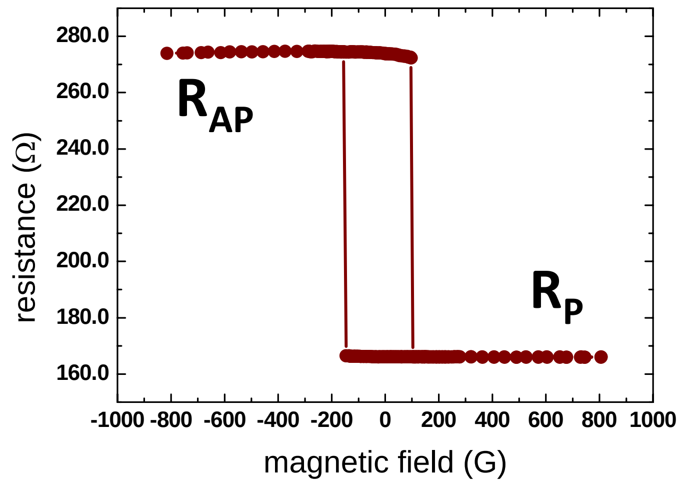
Magnetic metal/Insulator/Magnetic metal

Tunnel MagnetoResistance (TMR)

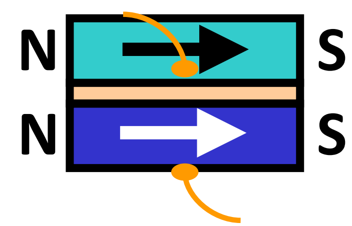
Anti-parallel state (AP)



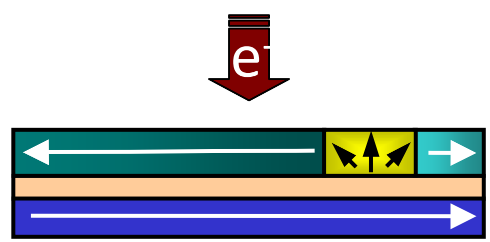
R_{AP}



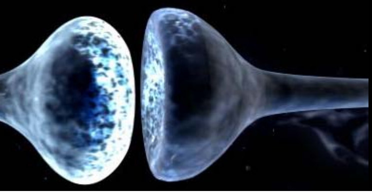
Parallel state (P)



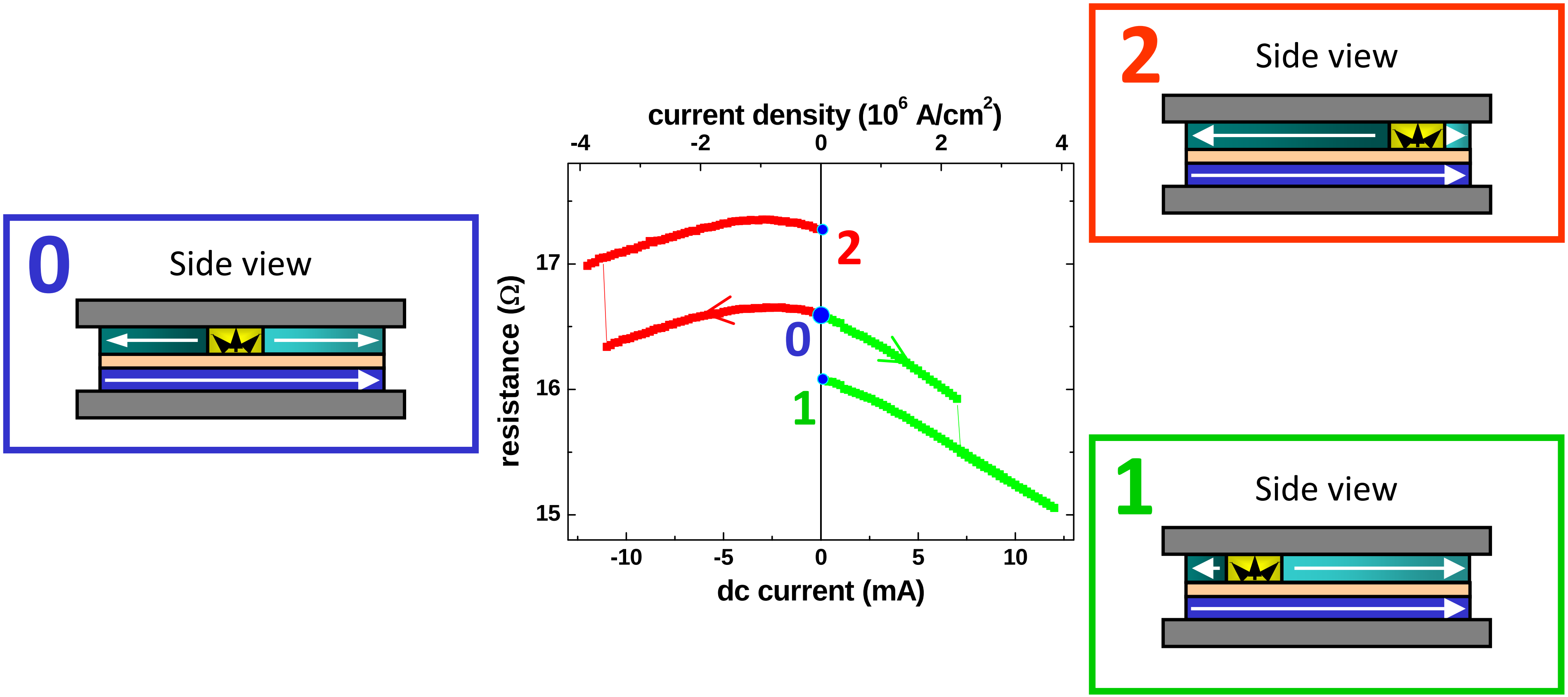
R_P



- Resistance variation: **Spin Transfer Torque (STT)**

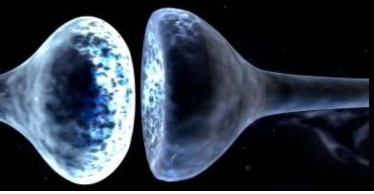


DW displacement by vertical DC current



- **Bidirectionnal DW motion**
- Current densities lower than previous DW motion experiments

A. Chanthbouala *et al.*, Nature Phys., 2011



Concept of the spintronic memristor

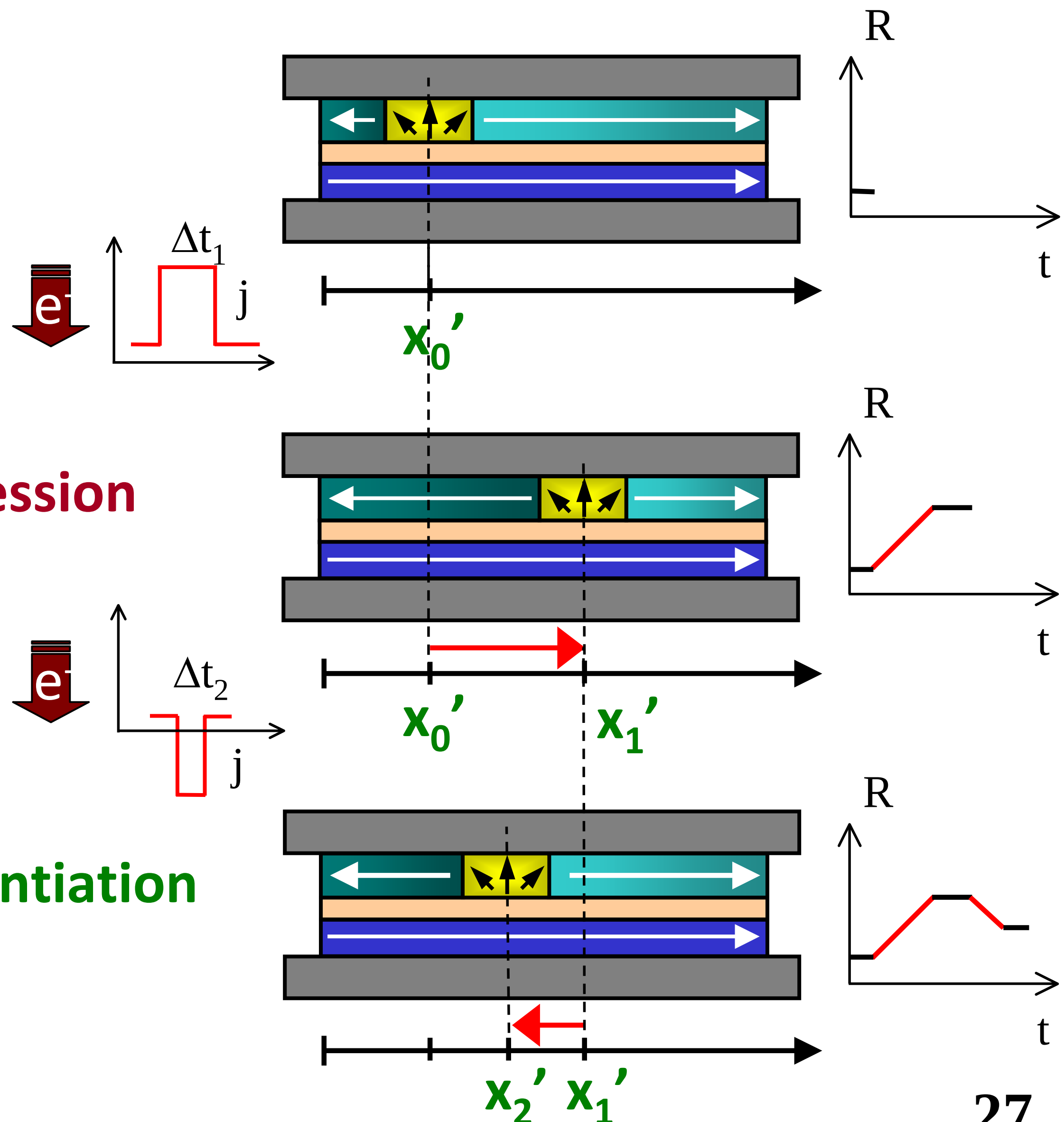
$$\Delta x \propto J\Delta t \propto q$$

- Resistance: DW position
- DW position: charge injected

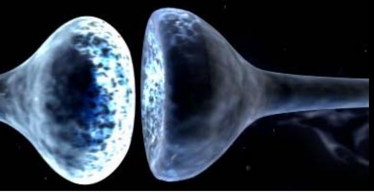
Positive current pulse: **Depression**

Negative current pulse: **Potentiation**

➢ **Synaptic weight**



Wang *et al.*, IEEE, 2009



Conclusion on the spintronic memristor

✓ Advantages

- Understanding of the underlying mechanisms: key to further improvements and **tuning of the synapse transfer function**

- **Fast**: sub-ns write process

- **Purely electronic effect**: high reliability and endurance

✗ Perspectives

- ON/OFF (R_{AP}/R_P) ratio now max = 6 ➤ **Theoretical limit 100**

- Connectivity: **perpendicularly magnetized materials**

➤ **Scalable below 50x100 nm**

International **T**echnology **R**oadmap for **S**emiconductors identified **Spin Transfer Torque-RAM** as one of the two most promising emerging memory devices: **Spintronic memristor will benefit from these developments**

Benchmarking memristors ?

Technology	memristors
Gain Signal/Noise ratio Non-linearity	
Speed Power consumption	
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	
Other specific properties	
Manufacturability (Fabrication processes needed, tolerances etc.)	
Timeline (When exploitable or when foreseen in production)	

Benchmarking memristors ?

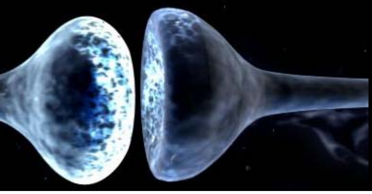
Technology	memristors
Gain Signal/Noise ratio Non-linearity	depends on the application
Speed Power consumption	
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	
Other specific properties	
Manufacturability (Fabrication processes needed, tolerances etc.)	
Timeline (When exploitable or when foreseen in production)	

Memristors as 2 states digital memories

- **ITRS table 2010**

Appendix 3: Performance parameters projected for the fully scaled emerging research memory technologies considered in this assessment compared with NAND Flash scaled to the 16nm technology generation

	NAND FLASH	FeFET	NEMS	STT-MRAM	Redox RRAM	PCM RRAM	Electronic Effects RRAM	Macromol RRAM	Molecular RRAM
Minimum F -Scaling	16nm	22nm	5-10nm	7-10nm	5-10nm	5-10nm	5-10nm	5-10nm	5-10nm
Cell Size	2.5F^2	8-4F^2	6-12F^2	20-40 F^2	8/5F^2	6F^2	8/5F^2	8/5F^2	5F^2
MultiLevel	3-bits/cell	NA	Yes	MLC 2bits/cell	Yes	4 bit/cell	Yes	NA	NA
Write/Erase Voltage	18-20V	0.6/-0.2V	1.5V	< 1.8V	<0.5V	<3V	<3V	1V	80mV
Read Voltage	0.1-0.5V	NA	3V	0.5V	<0.2V	<3V	0.7V	0.7V	0.3V
Write Erase Current	Low	NA	NA	<100μA	0.4μA	>100μA	NA	NA	NA
Write Erase Time	>10μs	20ns	0.9ns/0.3ns	<100ns	<5ns	<50ns 120ns	<20ns	<10ns	<40ns
Read Speed	15-50 □s	20ns	>1.5ns	10-20ns	<10ns	<60ns	<10ns	<10ns	<10ns
Retention Time	10yrs	~33ds	10yrs	10yrs	10yrs	10yrs	10yrs	10yrs	10yrs
Endurance Cycles	10^4-10^5	10^{12}	NA	2E12@10ns 2E6@10ms	10^{16}	10^{15}	10^{16}	10^{16}	10^{16}
Write Energy per Bit	>1fJ	2fJ	0.03fJ	<4pJ	1fJ	<2pJ	<100pJ	NA	0.2aJ
Ease of Integration	10 Masks	NA	NA	3-4 Masks BEOL	1fJ	2-3 Masks to BEOL	NA	NA	NA



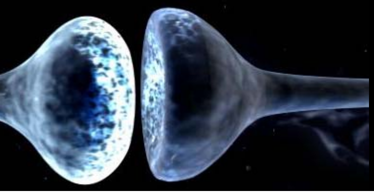
Memristors as artificial synapses

Criteria issue

Endurance / cyclability / low power consumption / OFF-ON ratio / small : yes

speed, retention time : ?

organic memristors ?



Memristors around the world

- **US** : 2009 DARPA “SyNAPSE” program

Systems of Neuromorphic Adaptive Plastic Scalable Electronics

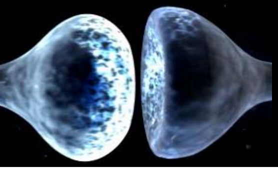
define a new path forward for creating
useful, intelligent machines

3 funded projects (*~ 5 M$ each for the first phase*)

- Hewlett-Packard (*memristors*) - HRL labs (*memristors*) - IBM (*?*)

- **Europe** :

FP7 Nabab, FP7 Bion (ended)
ERC NanoBrain & ERC Femmes projects, Chist-Era PNEUMA



Conclusion & perspectives

- State of the art memristor : exciting potential of memristor devices as artificial synapse

- spintronic memristor : resistance switching based on purely electronic effects

  ⇒ very promising : endurance, speed, power consumption

- Young topic : no demonstration yet of a cognitive chip based on memristors

- Dedicated architectures and programmation schemes to be developed

- Which type of memristor for which application ?

Acknowledgements

Funding :

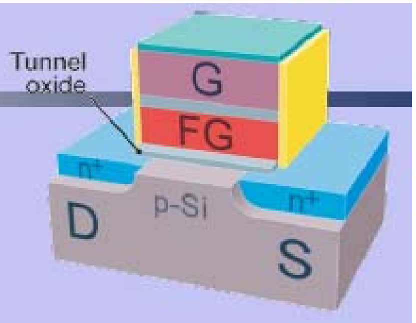
- **ERC Starting Grant 259068 Nanobrain**

- **ANR P2N MHANN « Memristive Hardware Artificial neural Networks Accelerators »**

- **PEPS project ACME « Memristive Accelerators »**

	Volatile		Non-volatile				
	DRAM	**SRAM**	**NAND Flash**	**Trapping charge**	**FERAM**	**MRAM**	**PCM**
Storage mechanism	Charge on capacitor	Interlocked state of logic gates	Charge on floating gate	Charge trapped in gate insulator	Ferroelectric polarization	Magnetization	Amorphous /cristalline phases
Cell elements	1T1C	6T	1T	1T	1T1C	1(2)T1C	1T1R
Feature size (nm)	50	65	90	50	180	130	65
Cell area	$6F^2$	$140F^2$	$5F^2$	$6F^2$	$22F^2$	$45F^2$	$16F^2$
W/E time	<10 ns	0.3 ns	0.1 ms	20 µs	10 ns	20 ns	50 ns
Retention time	64 ms	0	> 10 y	> 10 y	> 10 y	>10 y	>10 y
Write cycles	>1E16	>1E16	>1E5	>1E5	1.00E+14	>1E16	1.00E+09
Write voltage	2.5	2.5	15	8	0.9-3.3	1.5	3
Read voltage	1.8	1	2	1.6	0.9-3.3	1.5	3
Write energy	5 fJ	0.7 fJ	10 fJ	100 fJ	30 fJ	100 pJ	6 pJ

Requirements



... to compete with Flash

Endurance:	**> 10^7 cylces** (Flash 10^3 ... 10^7)
Resistance ratio:	**R_{OFF} / R_{ON} > 10**
Scalability:	**F < 22 nm and/or 3-D stacking**
Write voltage:	**approx. 1 ... 5 V** (Flash > 5 V)
Read voltage:	**0.1 ... 0.5 V**
Write speed:	**< 100 ns** (Flash > 10 µs)
Retention:	**> 10 yrs**

R. Waser, ISIF 2011