Nanowires for logic devices. From Si Towards III-Vs

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1. Scaling limitations of the MOSFET

- L is reduced: Reduced charge control by gate
- d_{ox} is decreased: Increase in gate leakage
- Shallow junctions: finite number of dopants: device variability
- V_T shift, increased inverse subthreshold slope (S_{min} = 60mV/dec)

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2. Power Challenge

Power per chip increases by scaling down

Alternative Architectures

➡ Optimum gate control by changing gate architecture. Roadmap:

Planar FET ➡ FinFET ➡ NW FET

Planar vs. NW FET

Improved scaling and better inverse sub-threshold slope

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3. Si NW FET

Using the top – down approach:

Sub – 10nm NWs reliably produced.

H_2 annealing and oxidation thinning leads to reduced LER, thus permitting for high performance GAA FET, which shows:

- Significantly improved gating behavior
- ~ 2.5 x L_{eff} benefit at constant short channel effects

Conclusion: **GAA FET is expected to be the ultimately scaled device**

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4. Need to reduce Power Consumption

$P_{dynamic} \sim V^3$

➡ Need to reduce V further

Steep Sub-threshold slope switch

Steep turn – on characteristics essential for low – power devices

Tunnel FET is the most promising small swing switch for V_{dd} scaling

➡ S<60mV/dec possible (principle of operation)

Disadvantage: I_{on} depends on tunneling probability

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5. Performance achieved with Si T-FET

S_{min} < 60mV/dec achieved in 2008 (SOI TFET, strained Ge – OI TFET)

S_{min} depends on voltage

Vertical Si NW TFET

Small diameter: Better electrostatics, more efficient dopant segregation

Benchmarking of published Si TFET performance

- Not all in one device
- Point slope does not help

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Further optimization of Tunnel FETs

- Material optimization

  III-V Heterostructure NWs

  Different TFET devices

- III-V planar homojunction TFET
- III-V planar heterojunction TFET
- InAs/Si NW heterostructure tunnel TFET

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Benchmarking

- Top-down GAA SiNW FET

  The ultimate – scaled FET

- T-FET: Best candidate for steep slope switch
- All-Si T-FET: limited by bandgap
- III-V heterostructure T-FET: Best option

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Questions – responses

- Good control of NW structural characteristics, size etc is possible
- III-V NWs on Si: Due to the small contact area, mismatch problem is overcome
- Growth of III-V NWs on Si easy, controllable

Main Challenges of vertical NW devices

- Contacting
- Device addressing
- Diameter variability

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