NANO-TEC

SEVENTH FRAMEWORK PROGRAMME

Discussion on Nanowires (Session 5)

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Questions related to Nanowires

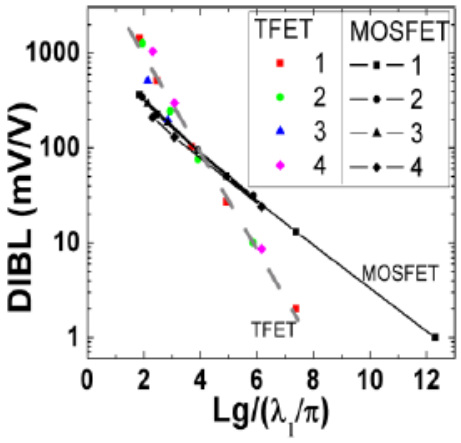
1. Which driving forces will govern the future of nano-wires?
   - Contacts and dopant engineering?

2. How do we address reproducibility issues of nano-wires characteristics from device to device, wafer to wafer and from batch to batch?
   - Is the top-down approach the most relevant one for future work ito reproducibility?

3. How to make novel nano-wire devices “attachable” to more conventional devices on silicon chips?

Questions related to Tunnel-FETs

1. T-FET's scalability: SS vs. Junction abruptness instead of SS vs. L_G
2. Below-60 mV/dec SS: how do designers cope with the small voltage window?



	Parameters			Natural Length $\Lambda=\lambda_1/\pi$
	T_S (nm)	T_{ox} (nm)	ε_{ox}	
1	10	6	9	8.128
2	10	9	9	10.231
3	20	9	9	14.051
4	10	6	18	6.491

Fig. 5 Scalability comparison of TFET vs MOSFET: MOSFET follows a universal scaling curve. TFET shows superior short channel effect when $L_g > 4x\ \lambda_1/\pi$. However, short channel effect degrades faster in TFET when $L_g < 4x\ \lambda_1/\pi$.

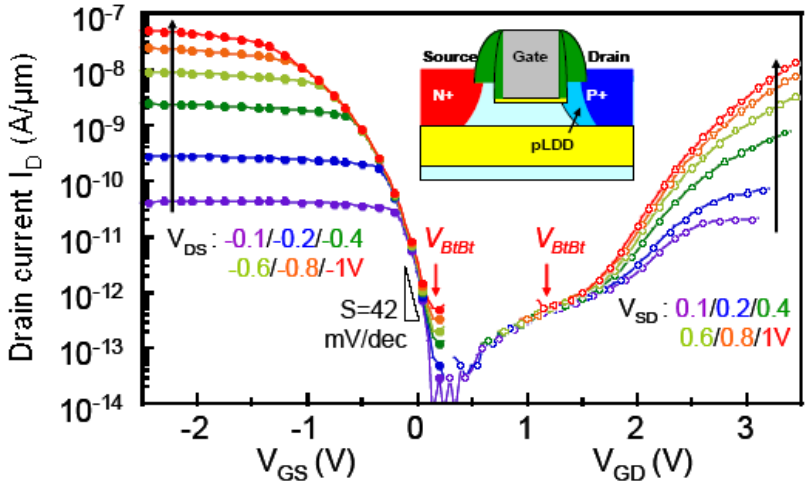


Fig. 6 : $I_D(V_G)$ characteristics of a L_G=100nm SOI TFET in p (left) and n (right) channel operation modes (t_{Si}=20nm; P30: pLDD, 30nm 2nd spacers). Local subthreshold slope at low as 42mV/dec is measured. We define V_{BtBt} as the voltage at which band to band tunneling occurs.

📖 L. Liu and S. Datta. *Investigation of the scalability of ultra thin body (UTB) double gate tunnel FET using physics based 2D analytical model*. In: Proceedings of DRC 2010. pp. 15-16.

📖 F. Mayer et al. *Impact of SOI, Si1-xGexOI and GeOI substrates on CMOS compatible Tunnel FET performance*. In: Proceedings of IEDM 2008. pp. 1-5.

5. Is T-FET meant to be application-dedicated? Multi-V_T scheme?
6. Experimental assessment of power consumption in elementary logic circuits
   - CV/I : high Miller capacitance + low I_{on}: does V_{dd} scaling come to the rescue?

Benchmarking exercise

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Technology	Nanowires
Gain, Signal/Noise ratio **Non-linearity**	Not available yet
Speed **Power consumption**	Tunnel FET: SS<thermodynamical limit at low V_D. Added value of T-FET as compared to impact ionization-mode FETs? SS vs. V_{DD} trade-off
Architecture/Integrability	Scalability of T-FETs?
Other specific properties	GAA nanowire: enhanced scalability (as compared to bulk Si single-gate FETs) with relaxed constrains on high-k gate dieletric thickness and silicon body thickness.
Manufacturability **(Fabrication processes needed, tolerances etc.)**	-Bottom-Up: (nanowire growth) not Si FF-compatible (Au), yield? 10nm min. diameter -Top-Down: CMOS-compatible, Abrupt junctions required for TFETs
Timeline	