Benchmarking Beyond CMOS Devices

Technology	Tunnel FETs
Gain **Signal/Noise ratio** **Non-linearity**	Similar functionality than MOSFET but promises lower voltage and lower power consumption, I_{on} may be smaller, Potentially better noise margin and high gain at extremely low current/voltage
Speed **Power consumption**	Depends on the I_{on} that can be achieved, probably not faster, maybe a little bit smaller Lower power consumption
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	Similar architecture, some circuit changes needed, may have density penality but there is room for new clever circuit designs.
Other specific properties	
Manufacturability **(Fabrication processes needed, tolerances etc.)**	SiGe TFET CMOS compatible, Integration of III-V heterojunction TFETs need more work but should be possible, junction quality, interface states, self-alignment critical, variability may be more critical due to exponential dependence of tunneling, V_T variation, doping tails and stochastic behavior of doping, high-k gate stack…
Timeline **(When exploitable or when foreseen in production)**	On the roadmap after GAA and conventional III-V → 5-10 years

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Technology	Junctionless Nanowire Field Effect Transistor (JNT)
Gain, Signal/Noise ratio **Non-linearity**	Not investigated yet (single-device characterization)
Speed **Power consumption**	CV/I: lower Miller capacitance than inversion mode FETs, SS~60mV/dec at V_{dd}=1V, I_{on} similar to IM FETs (contact resistance is the main issue!)
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	Same as FinFETs/GAA NW: high density required SOI is the substrate of choice (thermal dissipation issues?) Bulk Si OK
Other specific properties	
Manufacturability **(Fabrication processes needed, tolerances etc.)**	Fully CMOS compatible, no need for ultra- shallow junction engineering. Need for SOI thickness and LER control
Timeline **(When exploitable or when foreseen in production)**	Outperforms bulk Si GAA IM FETs at gate lengths < 25nm (in terms of SCE control), σ_{VT} being addressed,

NANO-TEC

What is missing?

- Theoretical understanding of the underlying physics, material science, etc.
  - Growth and morphology, surface roughness
  - Physical properties of nanowires (electronic, optical, thermal, mechanical e.g. strain, Interfaces, interface states, Surface chemistry etc)
  - Understanding the relationship between structure, function, properties
  - Further understanding of device operation and mechanism
- Fabrication
  - top-down versus bottom-up
  - Catalyzed, non-catalyzed growth
  - How can we address vertical wires, is there a benefit in density?
- Suitability of benchmarking criteria for nanowires, TFETs, etc.
- What breakthroughs need to be accomplished?
  - Contacts
  - Inversion
  - …
- Other open issues
  - Non-destructive testing,
  - Metrology e.g. doping concentration, D_{it}, abruptness of doping, uniformity, size,
  - variability

What is missing?

- Modeling and Simulation
  - Compact modeling needed to optimize and predict circuit performance
  - Better models needed to capture the physics of material and devices
  - Understand dynamic behavior of devices