Benchmarking Spintronics

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Outline

- What are the main drivers for Spintronics?
  - History
  - Present
- MRAM
  - Toggle MRAM
  - Spin Transfer Torque MRAM (STT-MRAM)
  - Thermally Assisted Switching MRAM (TAS-MRAM)
  - Thermally Assisted STT-MRAM (TAS+STT-MRAM)
  - Thermagnonic STT-MRAM
- Spin Torque Oscillators
- Spin Torque Microwave Detectors

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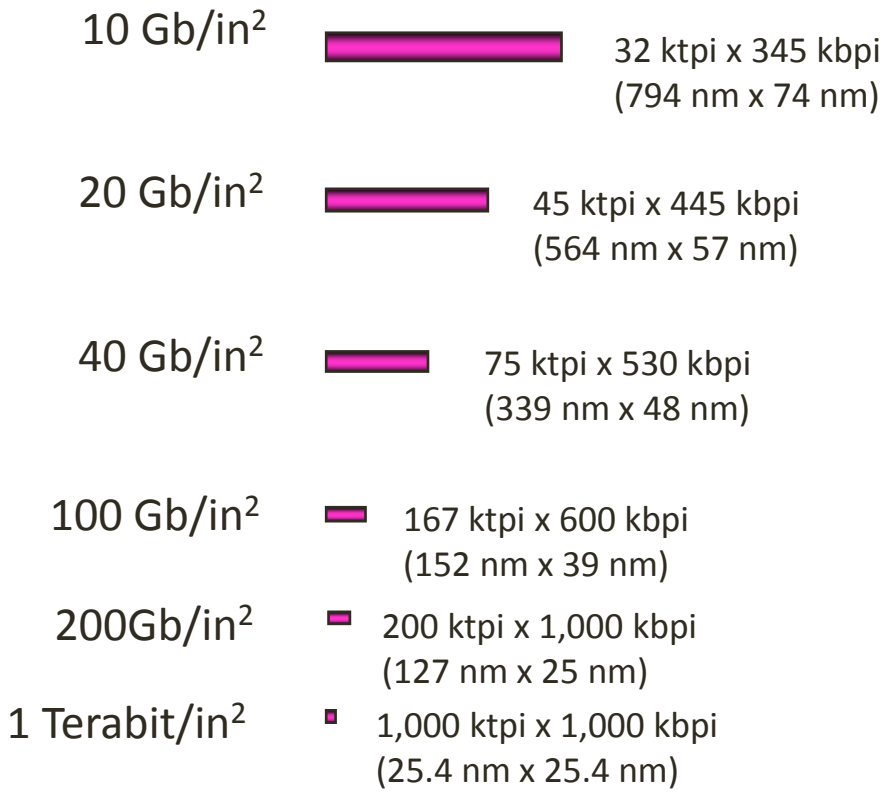
Historic Drivers for Spintronics

- Historic strong ”pull” from HDD Industry
  - Read heads – the main driver
    - Anisotropic Magnetoresistance
    - Made much more sensitive by GMR/TMR
  - Write heads – still an electromagnet
    - Concept of Microwave Assisted Magnetic Recording
    - Heat Assisted Magnetic Recording – flirting with nanoplasmonics
  - Media – benefits from spintronic read head development
    - Synthetic Antiferromagnet media – RKKY coupling

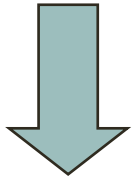
Bit size and Reader technologies

Areal Density vs. Magnetic Bit Sizes

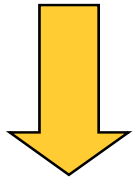


Experimental MR Effect

AMR (~2%)



GMR (~20 %)



TMR (20-230%)

CPP-GMR (up to 50%)

High MR ratio translates to High Signal– to–Noise ratio

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- HDD companies + others starting MRAM research in 1995
  - Conventional field switched MRAM
  - DARPA driven

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- MRAM pull – Half-Select Problem, Read Signal
  - Toggle MRAM solves Half-Select Problem (2001)
  - Toggle Patent out in 2004 – The end of conventional MRAM
  - MgO Tunneling Barrier out in 2004 – Almost the end of AlOx
  - 4 Mb Toggle MRAM goes commerical in 2006 – lukewarm response.
  - Toggle MRAM does not scale very well

Historic Drivers for Spintronics

- Parallel development: Academic ”Push” for Spintronics
  - Spin Transfer Torque (STT) – John Slonczewski, Luc Berger (1996)
  - Spin Torque Oscillator – John Slonczewski (1999)
  - STT driven domain walls
  - Spin Injection
  - Spin Hall Effect
  - Spin Pumping
  - Inverse Spin Hall Effect
  - Spin Seebeck Effect
  - Spin Injection using Spin Pumping
  - Spin Peltier Element
  - Thermally Driven STT, Thermo-magnonic STT
  - ”Spin Caloritronics”, ”Magnonics”

Present Drivers for Spintronics

- Limit power consumption

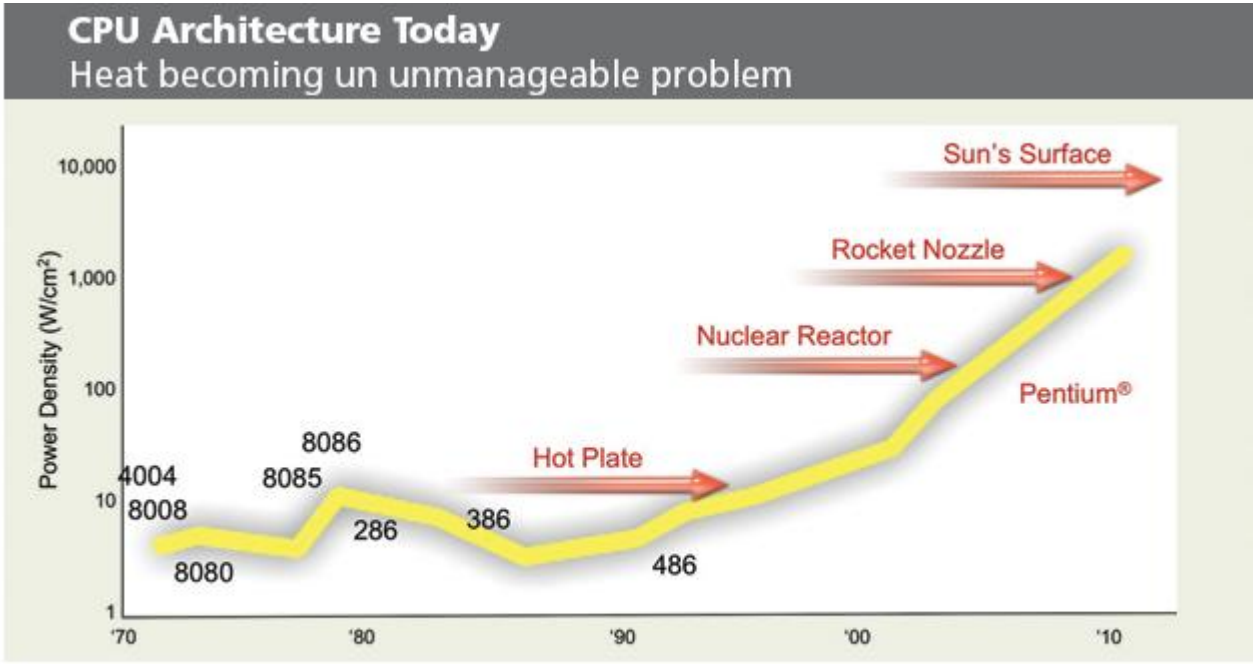
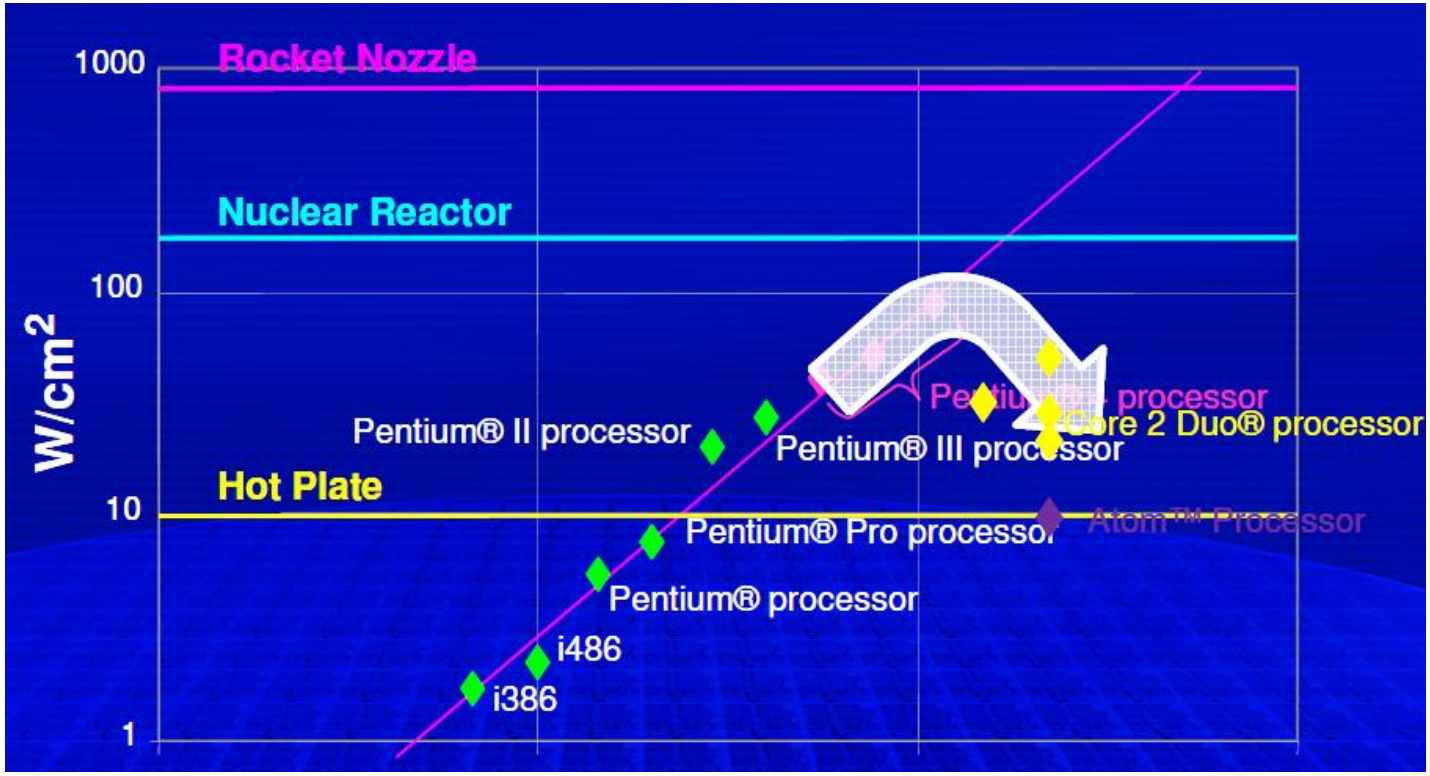


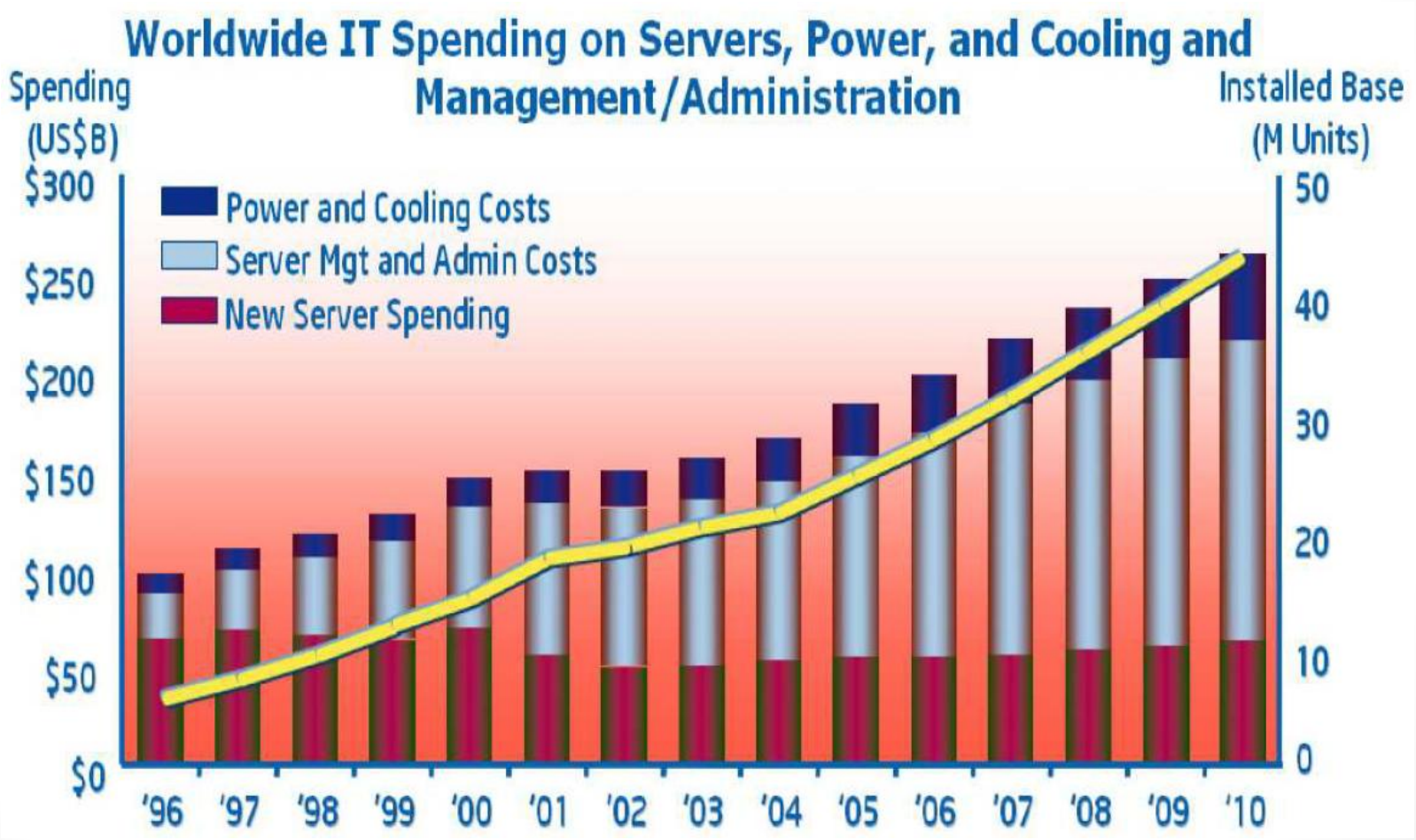
Figure 1. In CPU architecture today, heat is becoming an unmanageable problem. (Courtesy of Pat Gelsinger, Intel Developer Forum, Spring 2004)

Present Drivers for Spintronics

- Limit power consumption
- CPU solution = many cores
- Memory becoming the next problem



Power & Cooling Costs Still Increase



Present Drivers for Spintronics

Device Type	HDD	DRAM	NAND Flash	FRAM	MRAM	STTRAM	PCRAM	NRAM
Maturity	Product	Product	Product	Product	Product	Prototype	Product	Prototype
Present Density	400Gb/in^2 [7]	8Gb/chip [9]	64Gb/chip [10]	128Mb/chip	32Mb/chip	2Mb/chip	512Mb/chip	NA
Cell Size (SLC)	(2/3)F^2	6F^2	4F^2	6F^2	20F^2	4F^2	5F^2	5F^2
MLC Capability	No	No	4bits/cell	No	2bits/cell	4bits/cell	4bits/cell	No
Program Energy/bit	NA	2pJ	10nJ	2pJ	120pJ	0.02pJ	100pJ	10pJ [11]
Access Time (W/R)	9.5/8.5ms [8]	10/10ns	200/25us	50/75ns	12/12ns	10/10ns	100/20ns	10/10ns [11]
Endurance/Retention	NA	10^{16}/64ms	10^5/10yr	10^{15}/10yr	10^{16}/10yr	10^{16}/10yr	10^5/10yr	10^{16}/10yr

Device Type	RRAM	CBRAM	SEM	Polymer	Molecular	Racetrack	Holographic	Probe
Maturity	Research	Prototype	Prototype	Research	Research	Research	Product	Prototype
Present Density	64Kb/chip	2Mb/chip	128Mb/chip	128b/chip	160Kb/chip	NA	515Gb/in^2	1Tb/in^2
Cell Size	6F^2	6F^2	4F^2	6F^2	6F^2	N/A	N/A	N/A
MLC Capability	2bits/cell	2bits/cell	No	2bits/cell	No	12bits/cell	N/A	N/A
Program Energy/bit	2pJ	2pJ	13pJ	NA	NA	2pJ	N/A	100pJ [12]
Access Time (W/R)	10/20ns	50/50ns	100/20ns	30/30ns	20/20ns	10/10ns	3.1/5.4ms	10/10us
Endurance/Retention	10^6/10yr	10^6/Months	10^9/days	10^4/Months	10^5/Months	10^{16}/10yr	10^5/50yr	10^5/NA

Mark H. Kryder and Chang Soo Kim, IEEE Trans. Magn. **45**, 3406 (2009)

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Toggle MRAM

Technology	Toggle MRAM – Commercially Available
Gain **Signal/Noise ratio** **Non-linearity**	N/A N/A N/A
Speed **Power consumption**	40 MHz Zero stand-by power, ~120 pJ per switching event
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	CMOS compatible, embeddable, modular
Other specific properties	Radiation hard, High Reliability, Temperature range
Manufacturability **(Fabrication processes needed, tolerances etc.)**	CMOS compatible
Timeline **(When exploitable or when foreseen in production)**	Commercialized

STT-MRAM

Technology	Spin Transfer Torque MRAM (STT-MRAM)
Gain **Signal/Noise ratio** **Non-linearity**	N/A N/A N/A
Speed **Power consumption**	40 MHz Zero stand-by power, ~0.02 - 2 pJ per switching event
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	CMOS compatible, embeddable, modular
Other specific properties	Radiation hard
Manufacturability **(Fabrication processes needed, tolerances etc.)**	CMOS compatible
Timeline **(When exploitable or when foreseen in production)**	1-3 years

TAS-MRAM

Technology	Thermally Assisted Switching MRAM (TAS-MRAM)
Gain **Signal/Noise ratio** **Non-linearity**	N/A N/A N/A
Speed **Power consumption**	40 MHz Zero stand-by power
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	CMOS compatible, embeddable, modular
Other specific properties	Radiation hard
Manufacturability **(Fabrication processes needed, tolerances etc.)**	CMOS compatible Reliability?
Timeline **(When exploitable or when foreseen in production)**	1-3 years?

TAS+STT-MRAM

Technology	Thermally Assisted STT-MRAM (TAS+STT-MRAM)
Gain **Signal/Noise ratio** **Non-linearity**	N/A N/A N/A
Speed **Power consumption**	40 MHz Zero stand-by power, 2-3 pJ per switching event
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	CMOS compatible, embeddable, modular
Other specific properties	Radiation hard
Manufacturability **(Fabrication processes needed, tolerances etc.)**	CMOS compatible Reliability?
Timeline **(When exploitable or when foreseen in production)**	1-3 years?

Thermagnonic STT-MRAM

Technology	Thermagnonic STT-MRAM
Gain **Signal/Noise ratio** **Non-linearity**	N/A N/A N/A
Speed **Power consumption**	40 MHz Zero stand-by power, <1 pJ per switching event
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	
Other specific properties	Radiation hard
Manufacturability **(Fabrication processes needed, tolerances etc.)**	CMOS compatible? Functionality demonstrated?
Timeline **(When exploitable or when foreseen in production)**	3-5 years

Spin Torque Oscillators (STO)

Technology	Spin Torque Oscillators (STO)
Gain **Signal/Noise ratio** **Non-linearity**	N/A Low to moderate signal, high phase noise Mostly linear
Speed **Power consumption**	0.1 - 50 GHz demonstrated, >100 GHz expected Low to moderate depending on technology
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	CMOS compatible, embeddable, modular
Other specific properties	Ultra wide band, Ultra high modulation rates, Nano size
Manufacturability **(Fabrication processes needed, tolerances etc.)**	RF CMOS compatible GMR based STOs show good wafer uniformity
Timeline **(When exploitable or when foreseen in production)**	3-5 years

Spin Torque Microwave Detectors

Technology	Spin Torque Microwave Detectors
Gain **Signal/Noise ratio** **Non-linearity**	N/A High signal, noise reasonably good Mostly linear
Speed **Power consumption**	Very fast, >1 GHz expected Low
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	CMOS compatible, embeddable, modular
Other specific properties	Ultra wide band, Nano size, Good spectral resolution
Manufacturability **(Fabrication processes needed, tolerances etc.)**	RF CMOS compatible
Timeline **(When exploitable or when foreseen in production)**	3-5 years