MEMS
design ← → technology

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DIMES

(**D**elft **I**nstitute **M**icrosystems & nano**E**lectronic**s**)

Delft University of Technology

NANO-TEC

Athens, 13-14 Oct 2011

dimes

TU Delft

MEMS:

Micro-**E**lectro-**M**echanical-**S**ystems

Microsystems employ **miniaturization** to achieve high complexity in a small space

Generally fabricated using modified integrated circuit (IC) fabrication techniques and materials ➔ Si-based

NANO-TEC

imes

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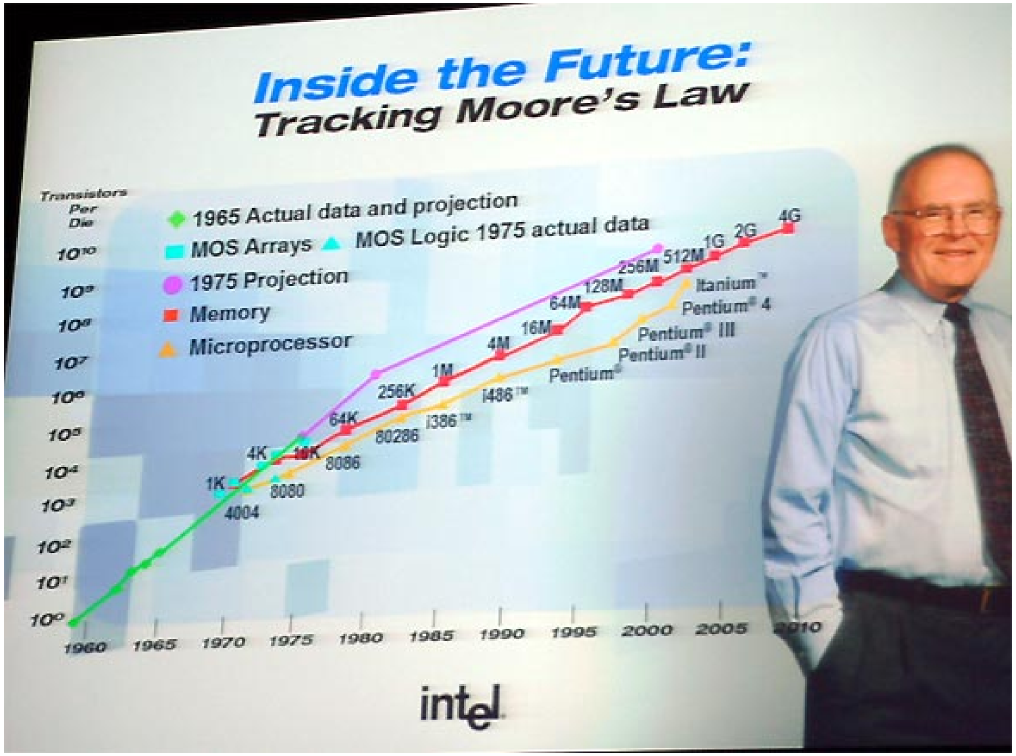
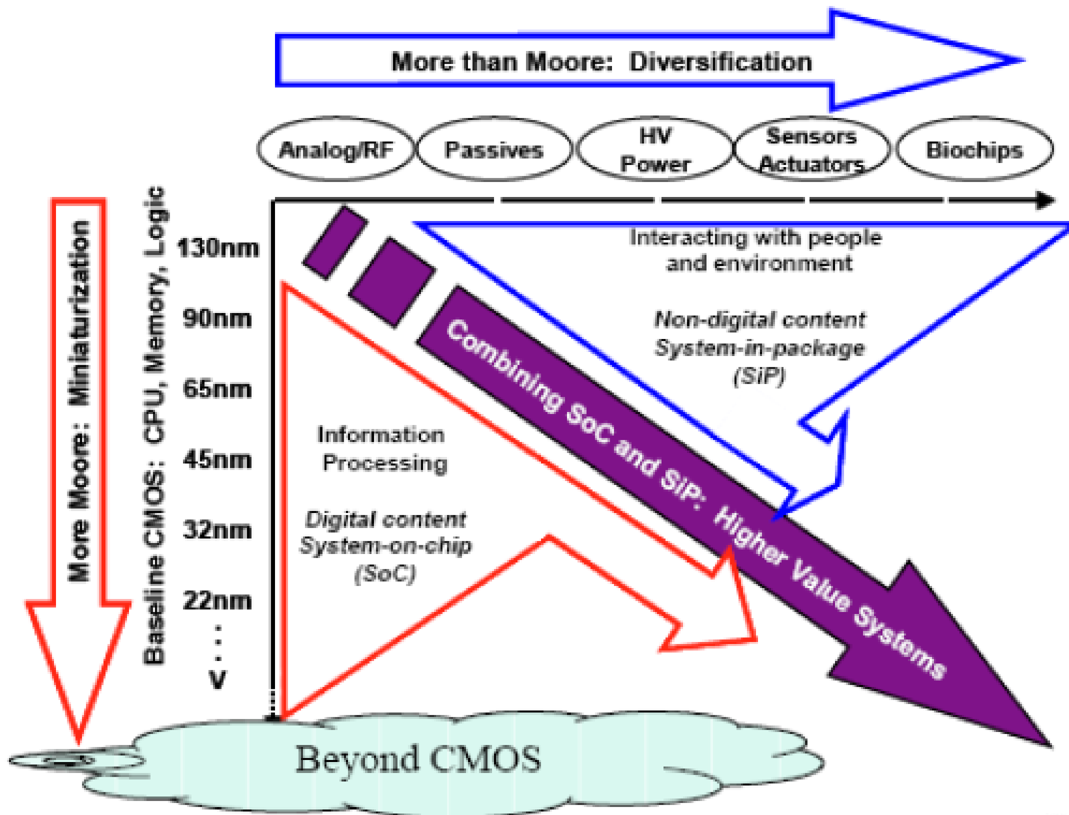
Microelectronics → Moore's Law

Miniaturization: More transistors per chip area



MEMS → More than Moore

Miniaturization: More functions per chip area



Generic/Application related Requirements for MEMS

- *High sensitivity/High resolution*
- *Low noise*
- *Stable/robust*
- *Fast response*
- *Small*
- *Low cost*
- *Low power*
- *Non contaminant/non invasive*
- *Non contaminable*
- *Compatible with meso and nanoelectronics*

“Ingredients” for MEMS development

- *Physics, Material science,Chemistry*
- *Technological Processes: IC* $^{++}$ and more
- (Biology)
- Dedicated CAD
- “Dedicated” packaging

MEMS ←→ IC

Many Similarities as well as Differences

- Technology
- Design
- Testing/Reliability
- Applications

  » How much “standardization” possible/desirable/feasible?

MEMS ⟷ IC

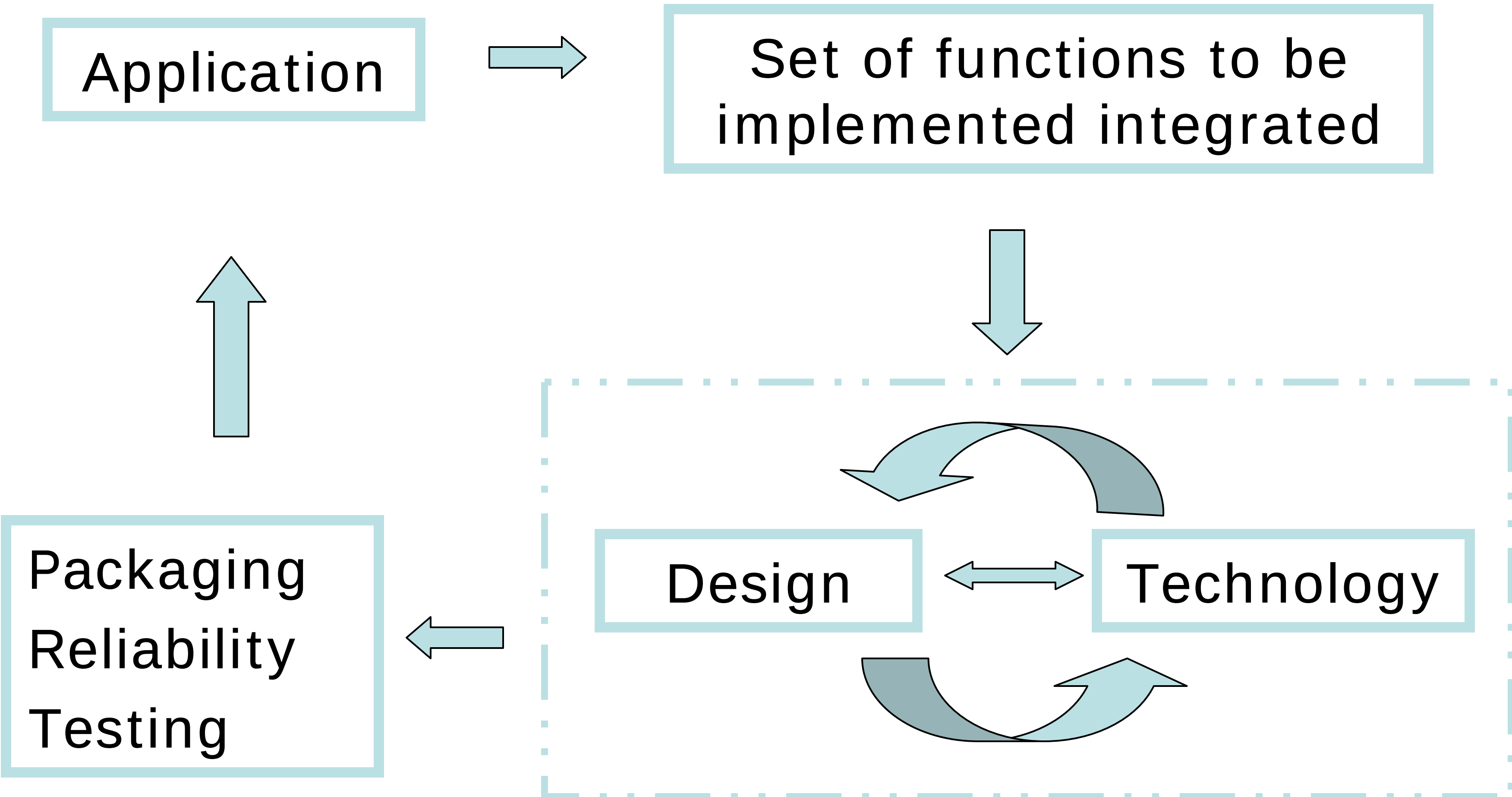
MEMS

- No unit cell
- No single "front end" technology, 3D
- Multidimensional Interaction space
- Very Multidisciplinary
- Generally low volume
- Application specific → design & technology

IC

- Unit cell: transistor
- CMOS, 2D
- Electrical Connections
- Physics & Engineering
- Generally large volume
- Application specific → design

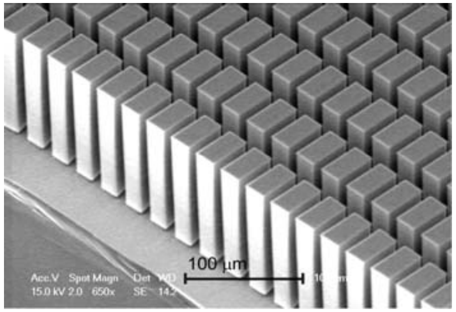
MEMS



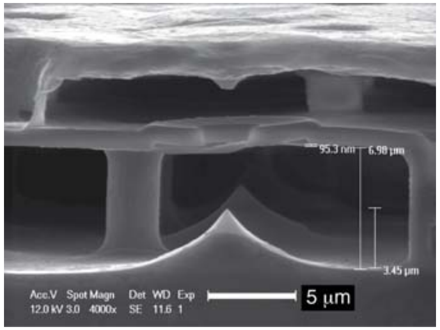
Application
Set of functions to be implemented integrated
Design
Technology
Packaging
Reliability
Testing

Technologies

- (Bi)CMOS
- Bulk Micromachining
- Surface Micromachining
- High-aspect ratio machining
- Wafer-to-wafer bonding
- Thin-film encapsulation
- ……



HAR fin-channel structure for microevaporator



SMM double cavity

3D micro/nano structuring

3D structures needed

to integrate specific functions

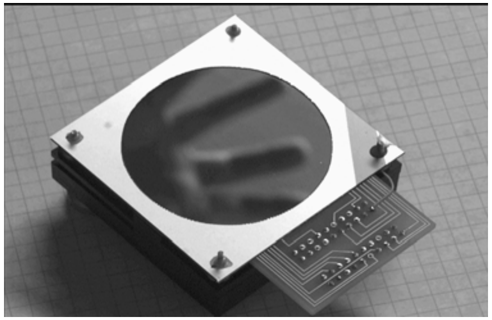
to enhance performance

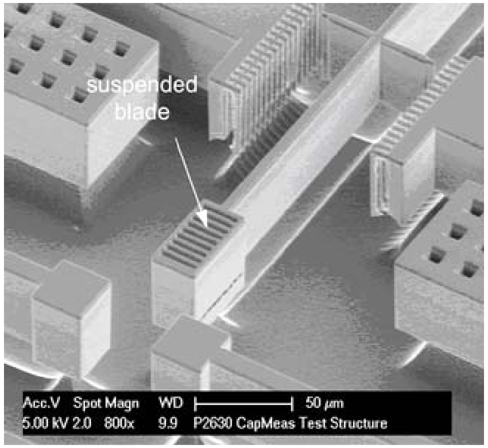
to miniaturize complete system

"Main" Technology:

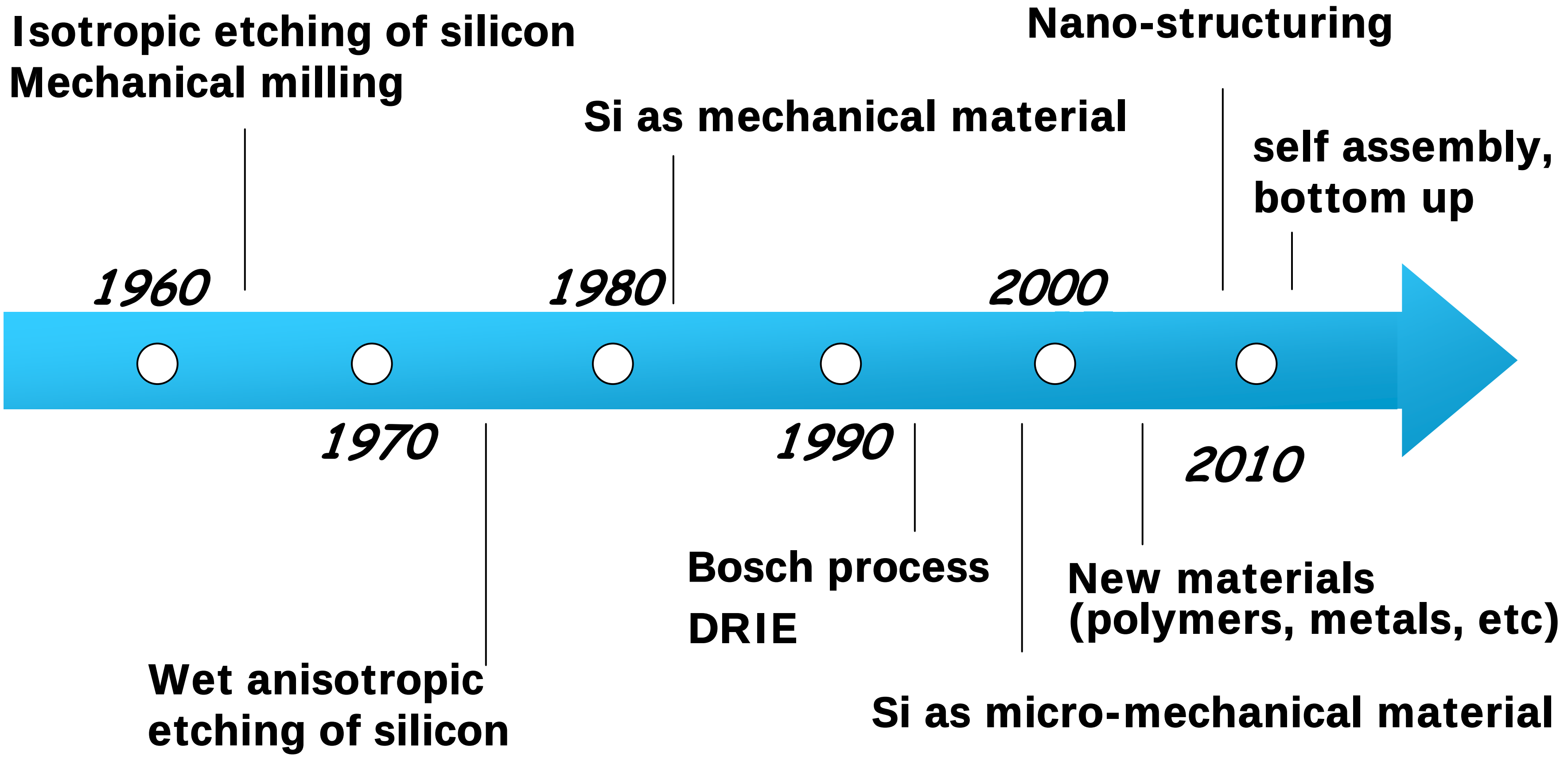
Bulk Micromachining

Surface Micromachining



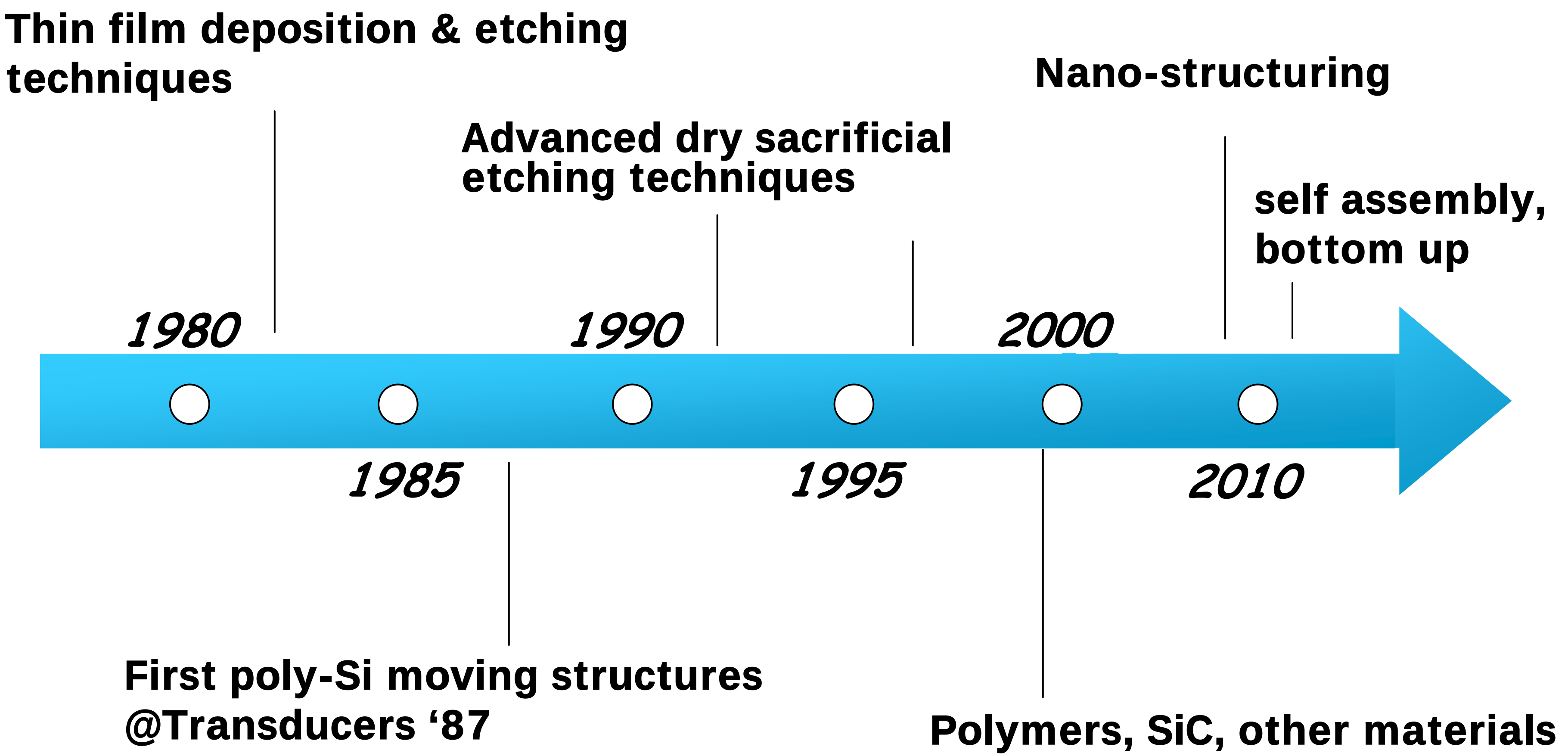


Silicon Bulk Micromachining
...>40 years of development.....



Silicon Surface Micromachining

...>25 years of development.....



Technology Trends

- **Top down & Bottom up**

  BMM & SMM →"merge"

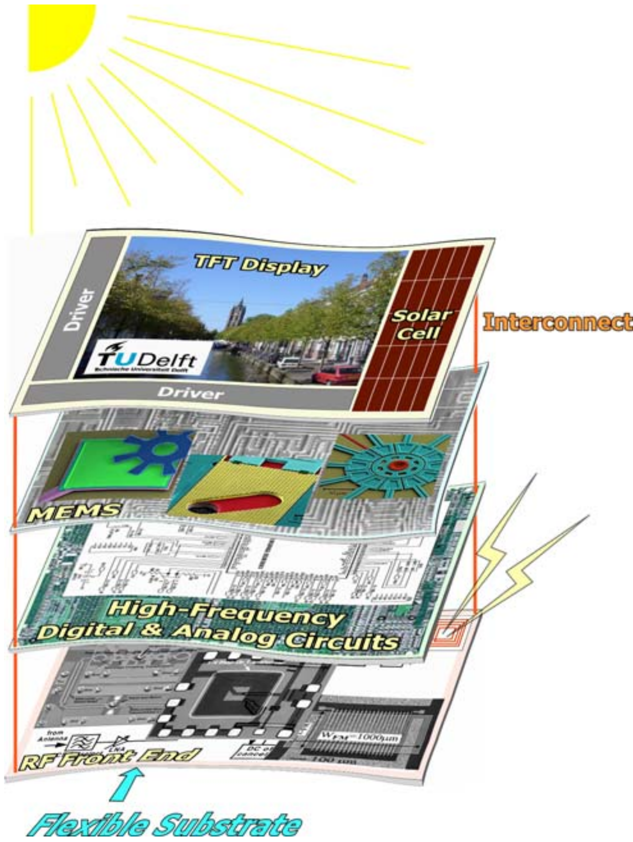
- **Functional multi-layers**

  hetereogenous intgration

- **System approach**
- **Harsh environment**

  SiC, Diamond, Graphene

- **Biocompatible**
- **"Flexible"**

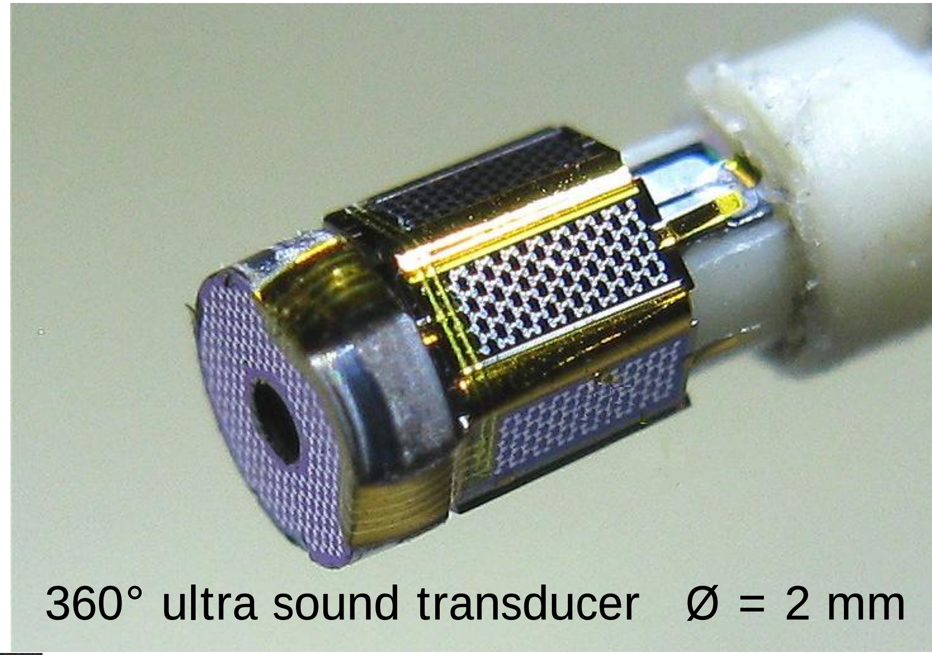


An example: "Living Chips"

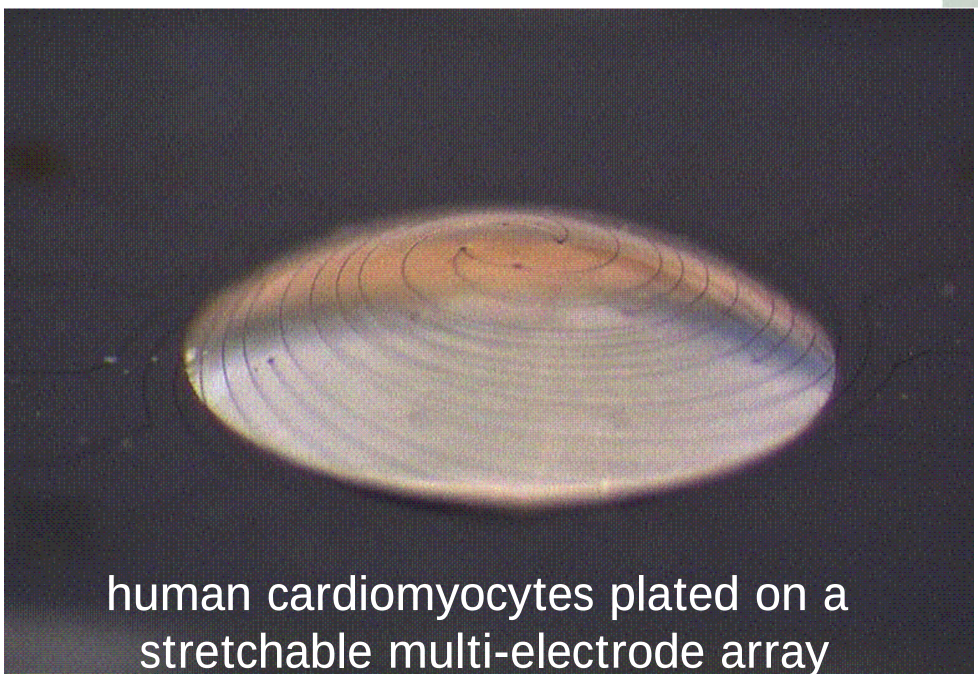
Chips for the Living

bring electronics and sensors
to the tip of catheters and guidewires

cooperations:
Philips Medical Systems, St Jude Medical,
BmechE (3mE), Cardiovascular Biomechanics (TU/e)



360° ultra sound transducer Ø = 2 mm



human cardiomyocytes plated on a stretchable multi-electrode array

Life on a Chip

integration of living cells on chips
as a functional layer

cooperations:
prof. C. Mummery (LUMC), Pluriomics (spin-off),
Philips Research

prof. Ronald Dekker
TUD & Philips

Design

Design of Device/Component

(package/system considerations)

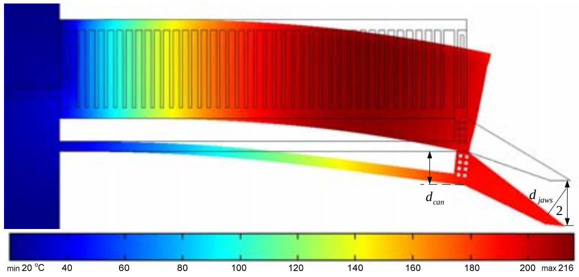
Modeling/Simulation:

specific features, several tools available

New device/new process

New device/existing process

Existing device/new process



Design Rules

"Design rules" for basic MEMS components
[mechanical structures and/or building blocks]

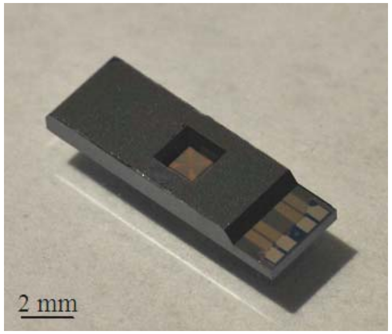
Membranes
Cantilevers
Beams
Comb Drives
Piezoresistors, Electrodes, …

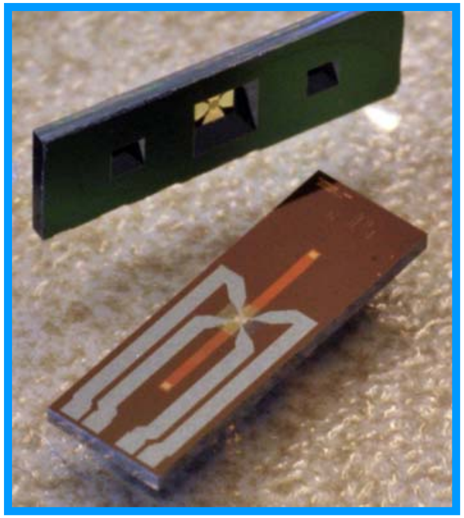
Possible/necessary?

Strong link to technology & application

System Integration

- Monolithic vs Hybrid
- Wafer level
- Packaging level



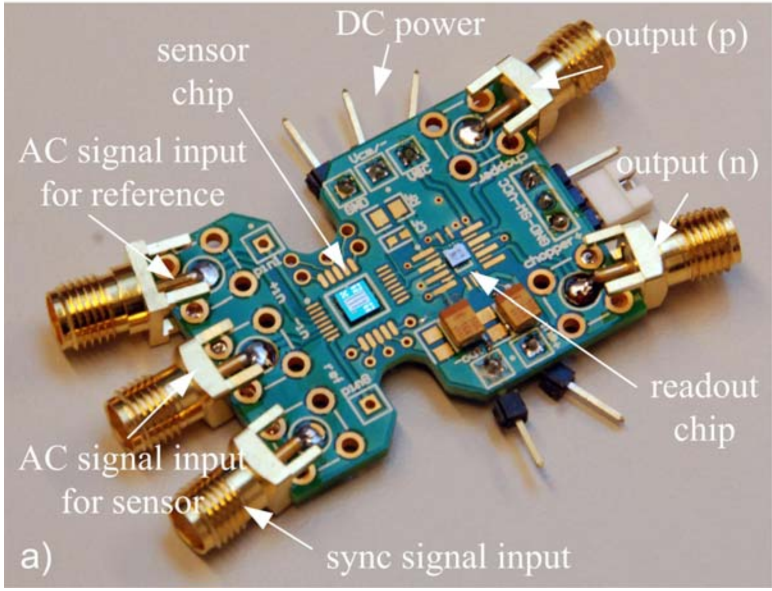


System integration:

➔ controls performance,

➔ >70% costs,

➔ >90% size and reliability

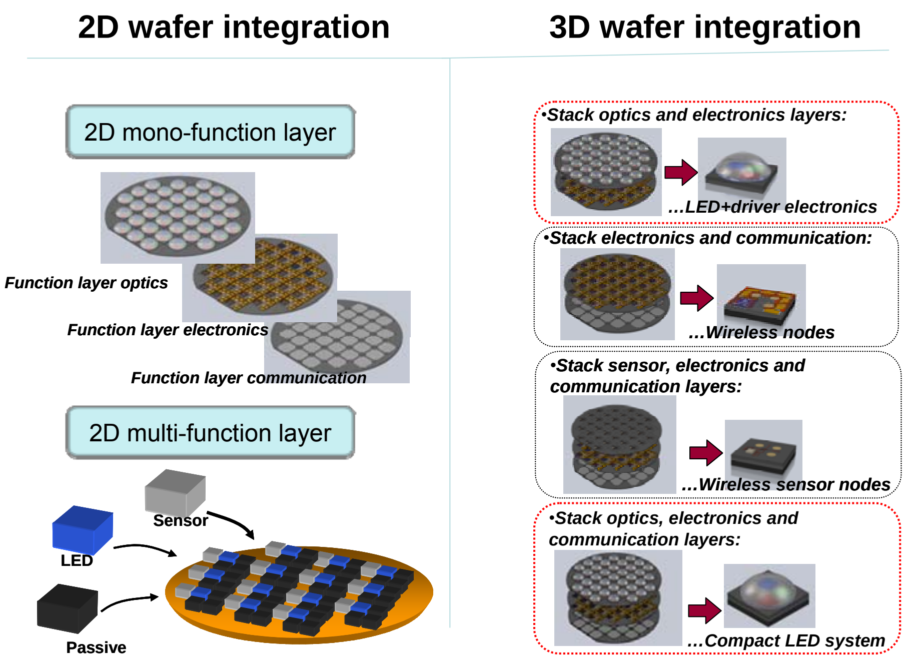


Wafer Level Integration

Wafer level, 3D, multi-function, smart and cost effective heterogeneous integration processes and technologies

Research subjects

- Polymer interposer technologies
- Hybrid interposer stacking for multi-function wafers
- 3D processes
- Design for X (reliability, yield, testability, cost, etc.)



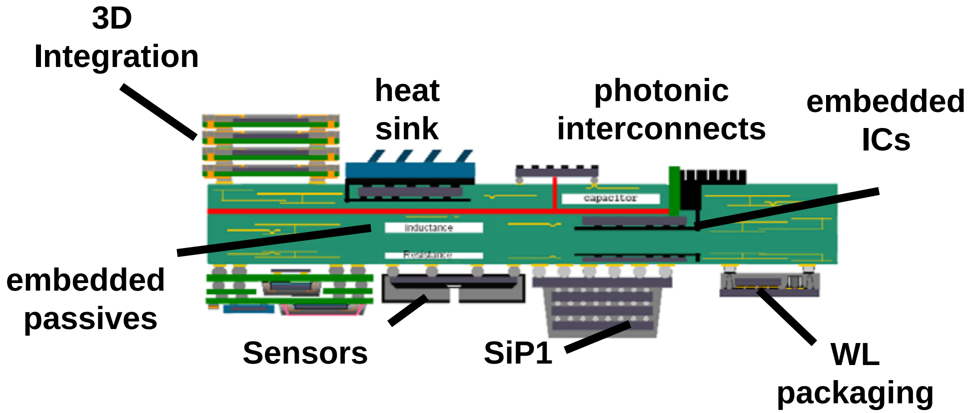
G.Q.Zhang, TUD & Philips

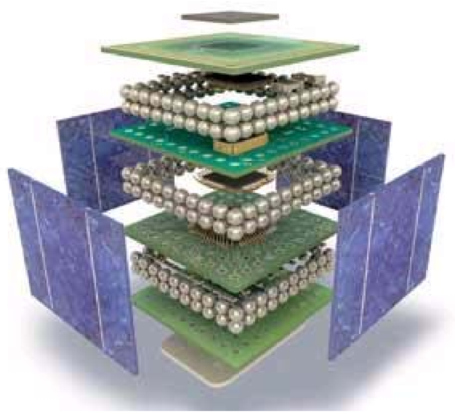
Package Level Integration (SiP)

Package level, 3D, multi-function, smart and cost effective heterogeneous integration processes and technologies

Research subjects

- Package architecture
- Integration processes for multi-functional modules & devices
- 3D and novel interconnect
- Design for X (reliability, yield, testability, green, etc.)
- Cost model





G.Q.Zhang, TUD & Philips

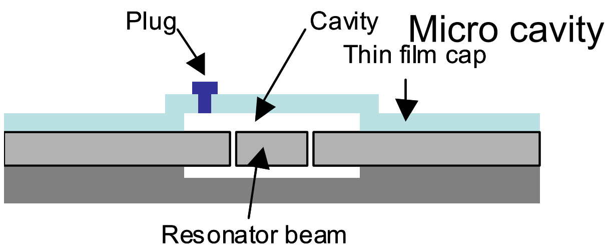
An example

- Thin film encapsulation for MEMS
  - Design for reliability
  - Mechanical design and modeling
  - IC compatible fabrication process
  - “pre-packaging” at wafer level

Design for Reliability of MEMS Packages

Motivations

- **During MEMS design assembly and packaging influences on micro cavities should be considered as they can threat the product or influence the performance.**



Objectives

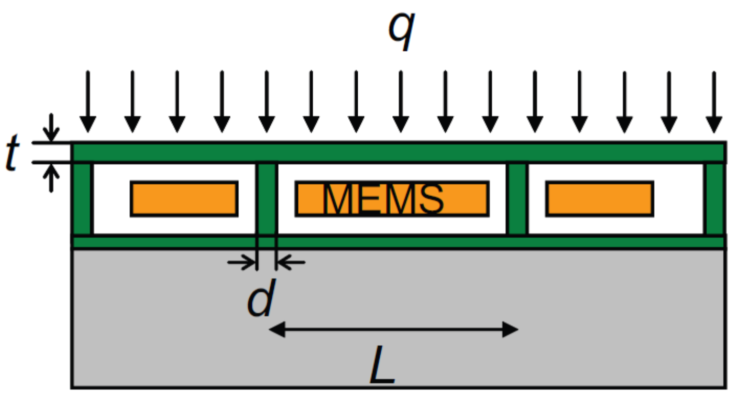
- **Develop predictive models to estimate weak spots in the design**
- **Find common failure modes of micro cavities**
  - **during manufacturing**
  - **during lifetime**

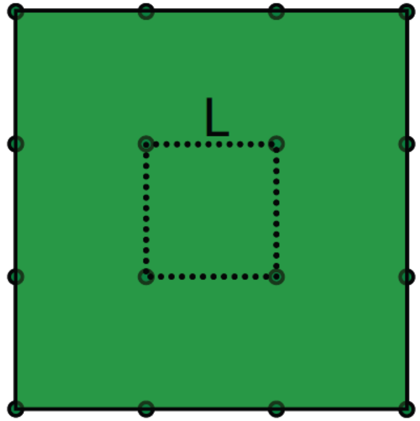
Approach

- **Combined experimental – modeling approach**
  - **Experimental determination of failure mode**
  - **Modeling of failure**
  - **Proposal of geometry / process adjustments**

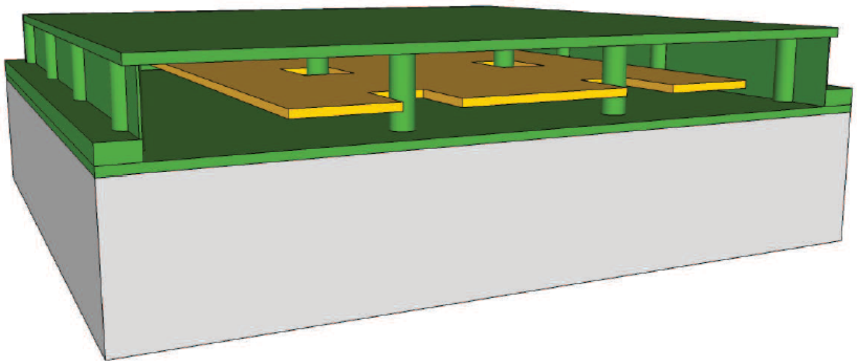
J.Zaal et al., TUDelft

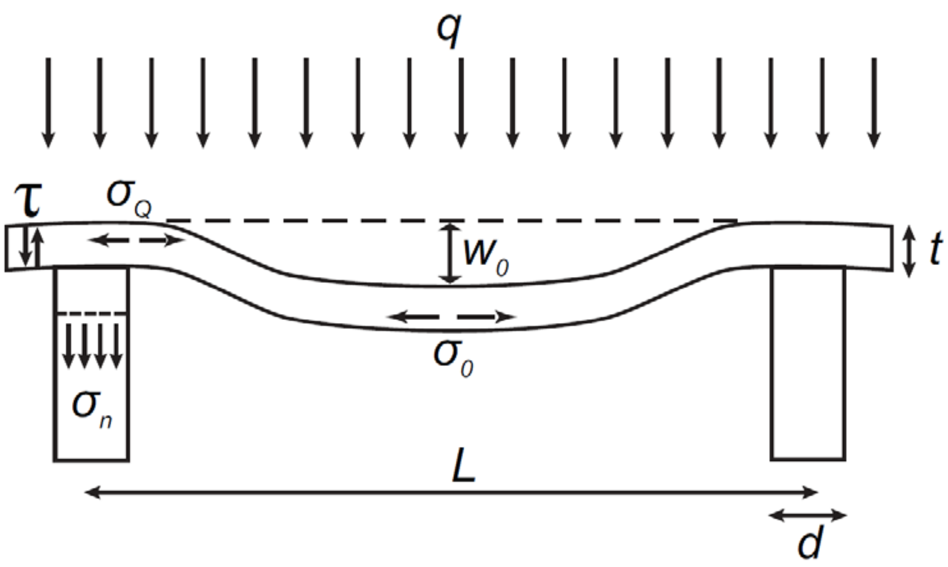
Mechanical Design of Thin Film Encapsulation





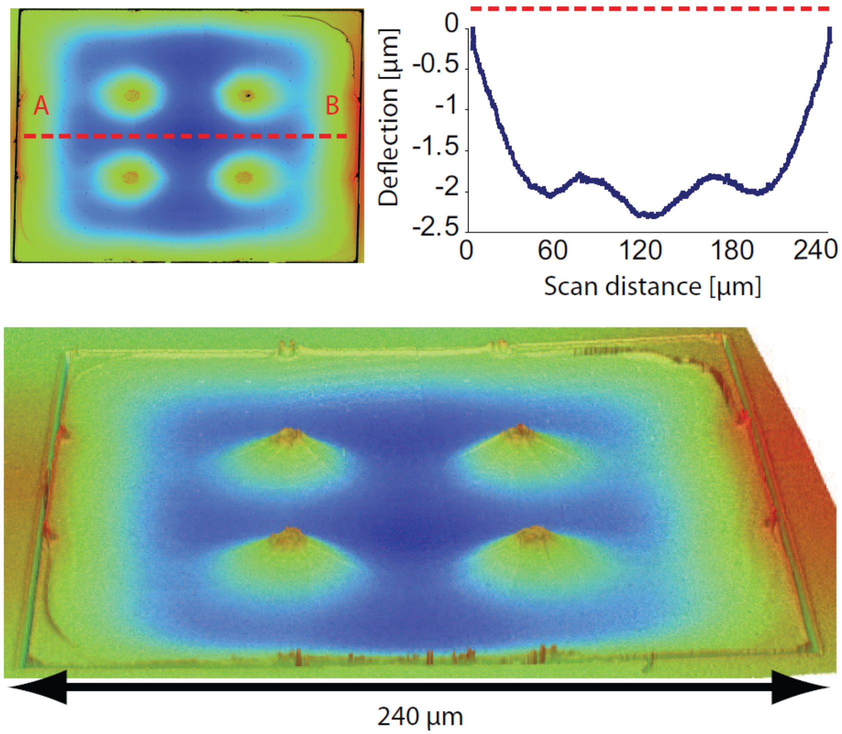
Thin-film package geometry consisting of a square plate with supporting columns



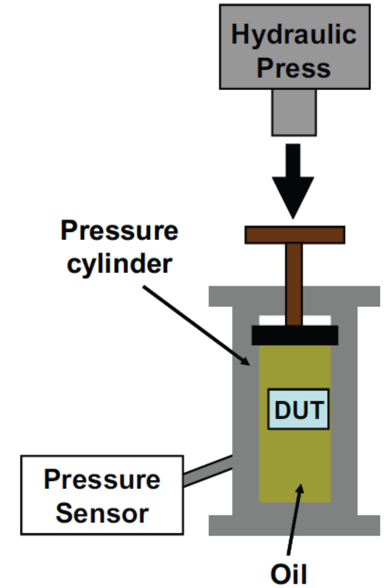


Stress components and the deflection of the capping layer taken into account in the mechanical model.

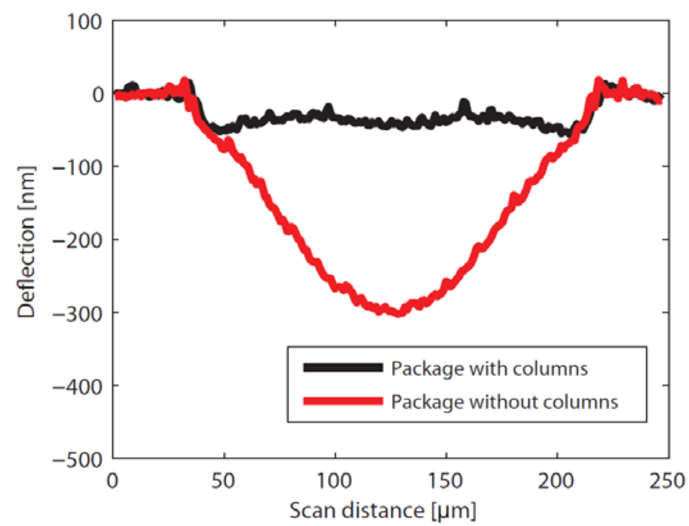
F.Santagata et al., TUDelft



3D imaging of the packages by optical profilometry after loading. The cap deflects and is stuck to the bottom of the package.

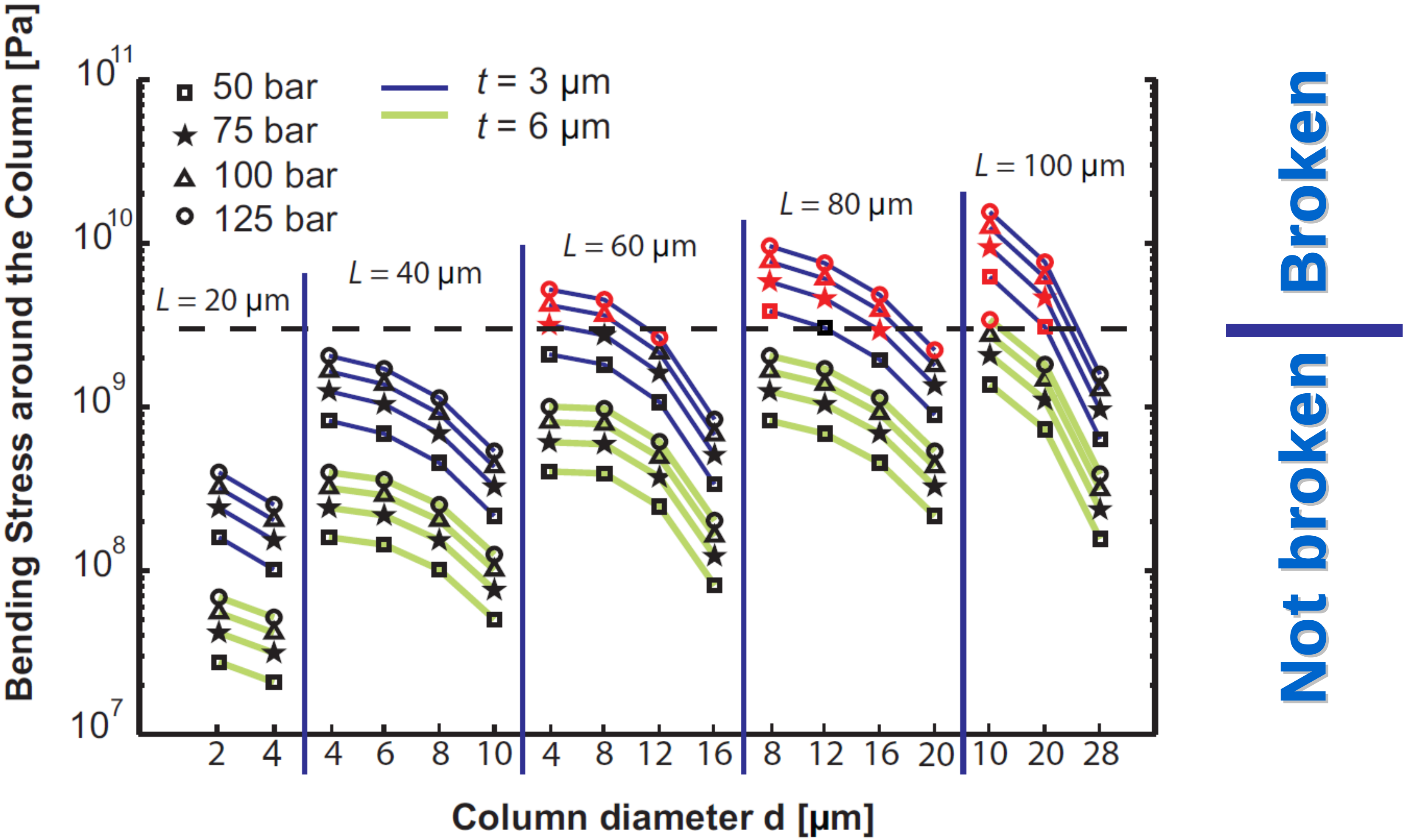


Sketch of the setup for the pressure test



Deflection under 1 bar. Comparison between two square packages (180 µm side length) with and without columns (4 µm diameter). The deflection of the package with no columns is too large for many applications.

Hydrostatic pressure test



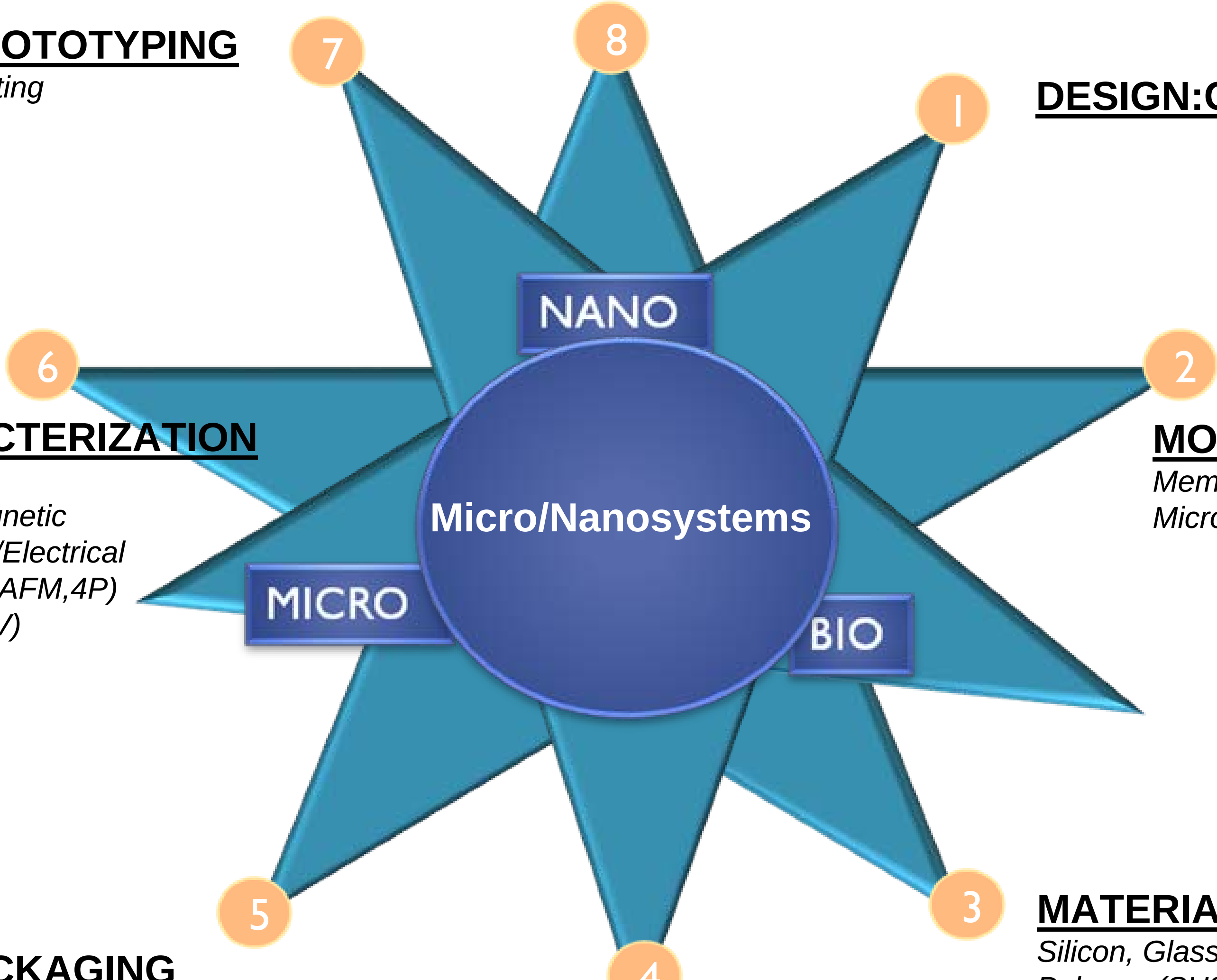
The red markers represent the broken packages.

From idea to Product

MEMS

PROTOTYPING
Testing

DESIGN:CAD



CHARACTERIZATION
Electrical
Optical/Magnetic
Mechanical/Electrical
SPM (STM,AFM,4P)
Fluidics (PIV)
SIMS,SEM

MODELLING
Mems
Micro/nano fluidics

MATERIALS
Silicon, Glass
Polymer (SU8)
Nanostructured Materials
Nanotubes, wires

PACKAGING
Wafer level
Heterogeneous integration
3D
Nano-assembly
Selfassembly

FABRICATION
CMOS
Bulk Micormachining
Surface Micromachining
Nanoimprint/E-beam
Advanced Deposition etch

Adapted from D'Amico et al, 2011

Challenges

- Miniaturization: size matters
- Integration: manage complexity
- New technologies: acceptance
- Autonomous: long life
- New applications: more functionality

Challenges

- Miniaturization:
  - Technology advances
  - Design tools
  - Simulation programs

Challenges

- Integration: manage complexity
  - Monolithic vs heterogeneous
  - Performance vs cost vs volume

➔“user” wants a system!

Challenges

- New technologies
  - Needed to integrate new functionalities
  - Reliability
  - “multiple” applicability

Challenges

- Design ⇔ Technology
  - Path to “generic” process(es)/standardization
  - Possibility and impossibility of a library
- Integration & Reliability
- Sub-domains:
  - Automotive
  - Bio/medical
  - CE and Mobile

Concluding Remarks

- **MEMS** development has come through fundamental research with an eye for the application.
- **Micro and nano technologies** advances offer many opportunities for improved performance and reduced costs in a wide range of industries.
- Emphasis is on improved functionality and reducing the size of the **system** rather than reduced size of individual components.
- **Scaling** of components should only be done where functional benefits can be obtained.
- Many applications require a **multi-disciplinary** approach
- **Health**, **Environment** and **Energy**: main application area