Design For Beyond CMOS

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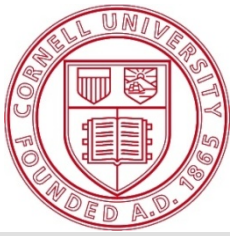
The design process can not be considered effective and successful if
it needs PhD level experts,
or doesn't work robustly,
doesn't produce working products within spec's in first spin,
and is not open for new research breakthroughs that may be useful in technology applications.



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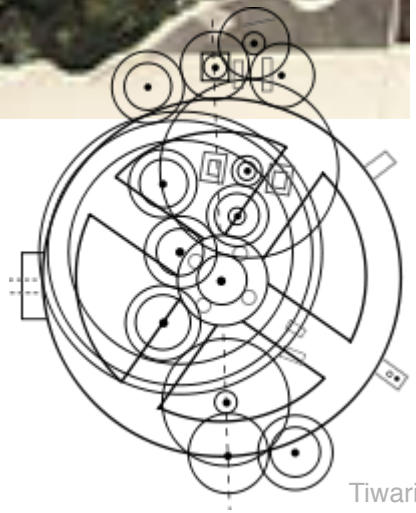
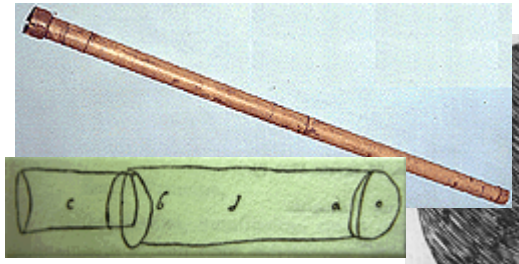
Design is Central to Good Engineering

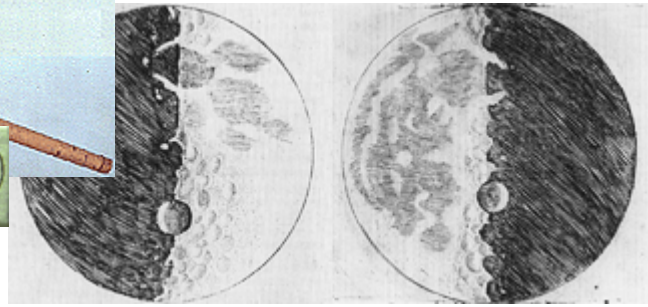
Analog Computing circa 200 BC:
Antikythera mechanism



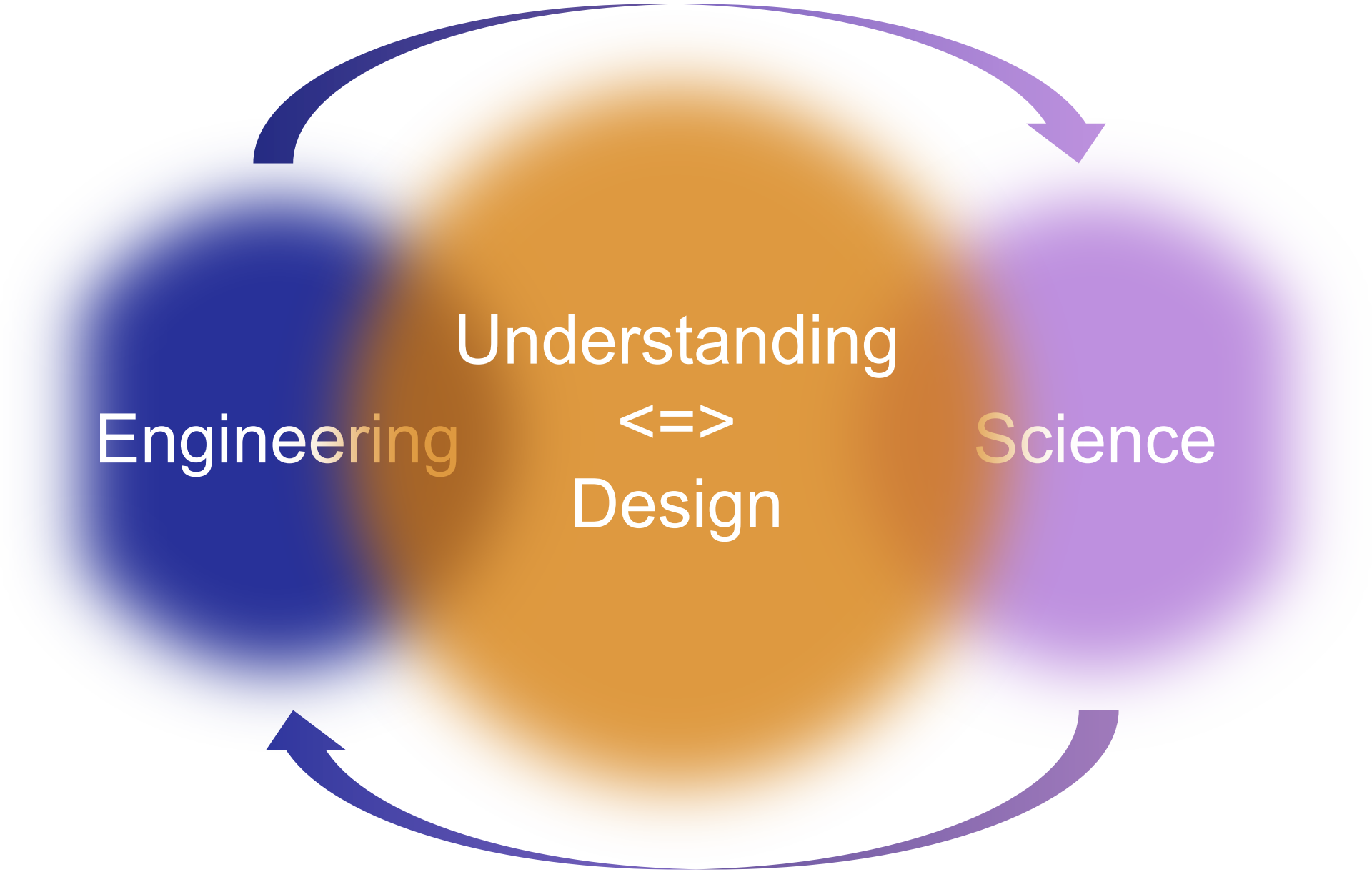
The Modern Era:
Copernicus, …

Galileo





phases of moon



Good Engineering => Good Tools => New Science => New Engineering => New Tools =>

So, what do we do today?

Digital World

High performance microprocessors:

Trillion transistors
hundreds of tools (layout, timing, process, models, noise, power, DRC, LVS, Yield, verification, …)
hundreds of people
2-3 years
hundreds of milllion$'s

Embedded :

Sub-trillion transistors
hundreds of tools (layout, timing, models, noise, power, DRC, LVS, Yield, verification, …)
IP,
10's of people
1-2 years
10's of million$'s

We usually get it right first time around

Analog/Mixed-Signal/RF World

Million transistors
Even more tools
Small-signal, parasitics, tlines, large signal, cross-talk, …

With enough resources, we can design for digital with trillion transistors,

but,

can't design with million transistors.

The objective of design *is* that non-specialists, with sufficient training, e.g., BS/MS, can design without knowing details of technology and everything else, so that designs can function in first pass with reliability and robustness.

This allows many designers (x100 or more) to take advantage of the costly technology infrastructure towards societal benefit. The technology costs are thus amortized.

The design approaches should also balance efficiencies and effectiveness.

And be open to new science breakthroughts

Problems with Current Microelectronics Infrastructure

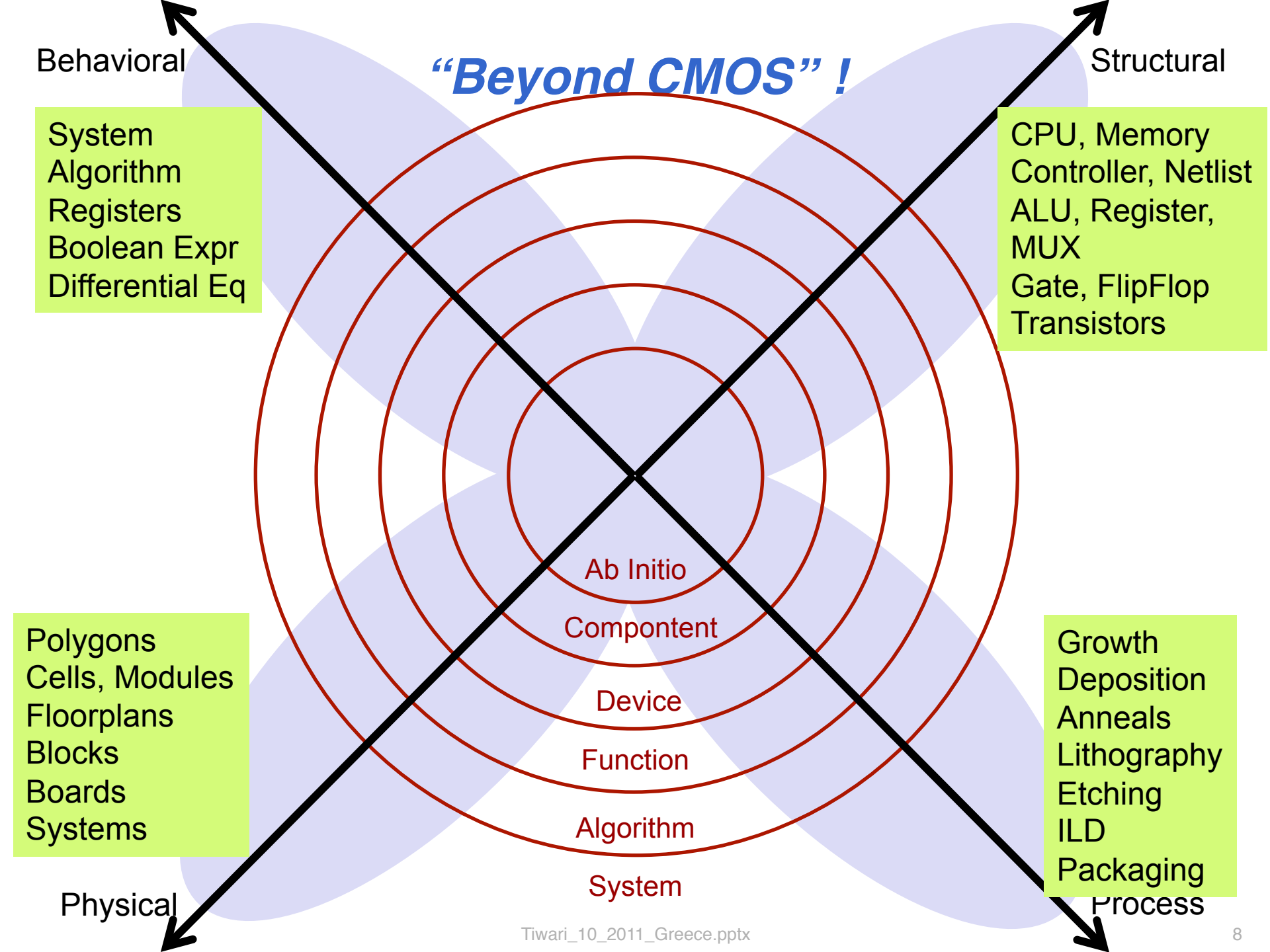
- Designed for digital quasi-static
  - Process models – layout – 2D device – compact model for quasistatic with layout, snm, thermal, noise, statistics, ..
  - Corners for all variations
  - Designed for worst cases
  - Inefficient
- Stochasticity is intrinsic at nanoscale; it is not just a threshold variation
- Quasistatic approaches brake for high frequency
  - In-plane effects– lateral diffusions, capacitances, … parasitics
  - Small-signal effects. …
- New technologies are very difficult to incorporate.
- Every change, e.g., 3D, is a kluged tool to be repeatedly used with base.

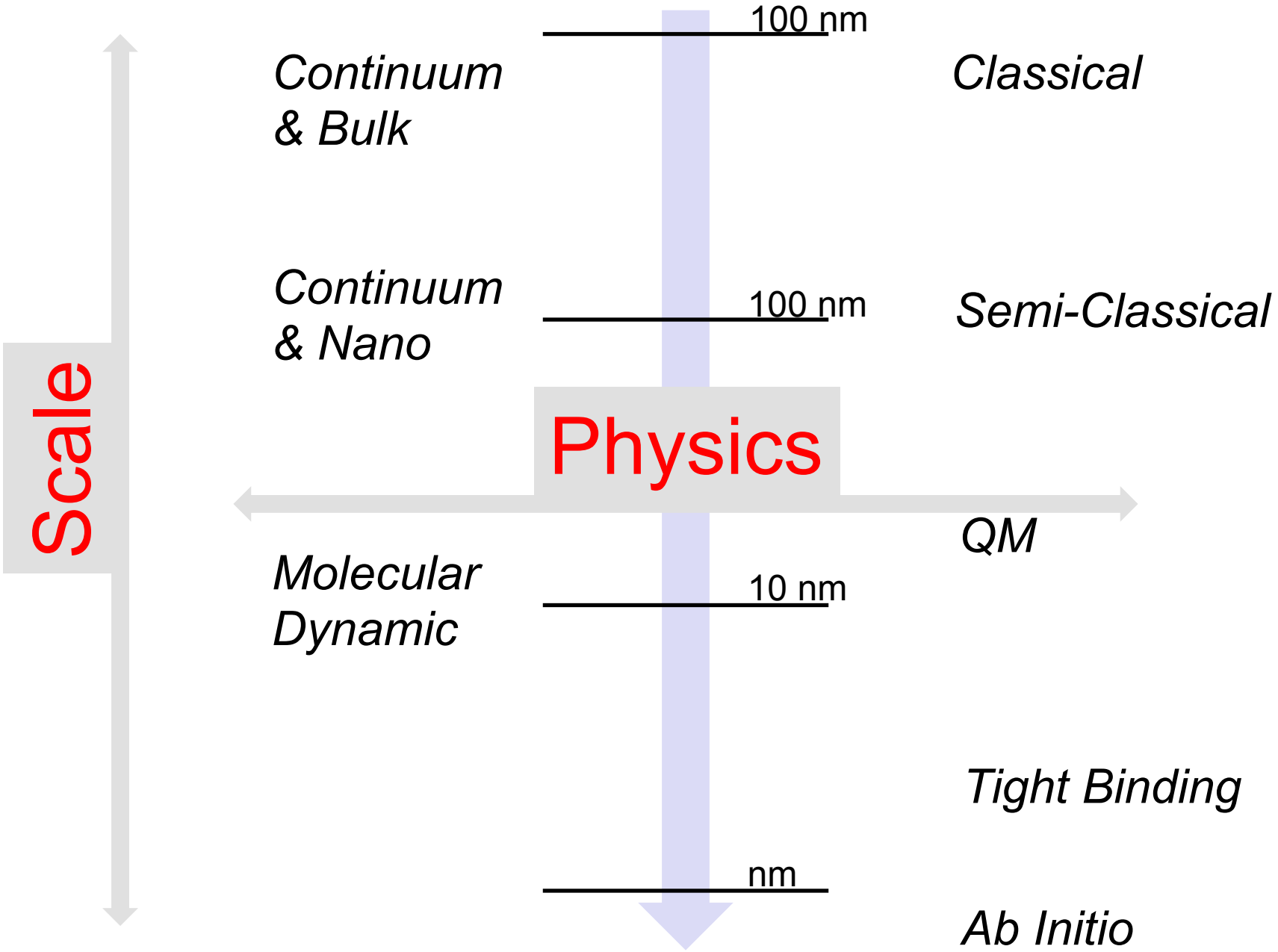
And, the problems beyond?

- Signals are not just I, Q and V in t.
- New signal modalities and their transformations.
- Corners at nanoscale? Stochasticity is intrinsic.
- Heterogeneous integration.
- 2D – 3D
- Abstractions across scales

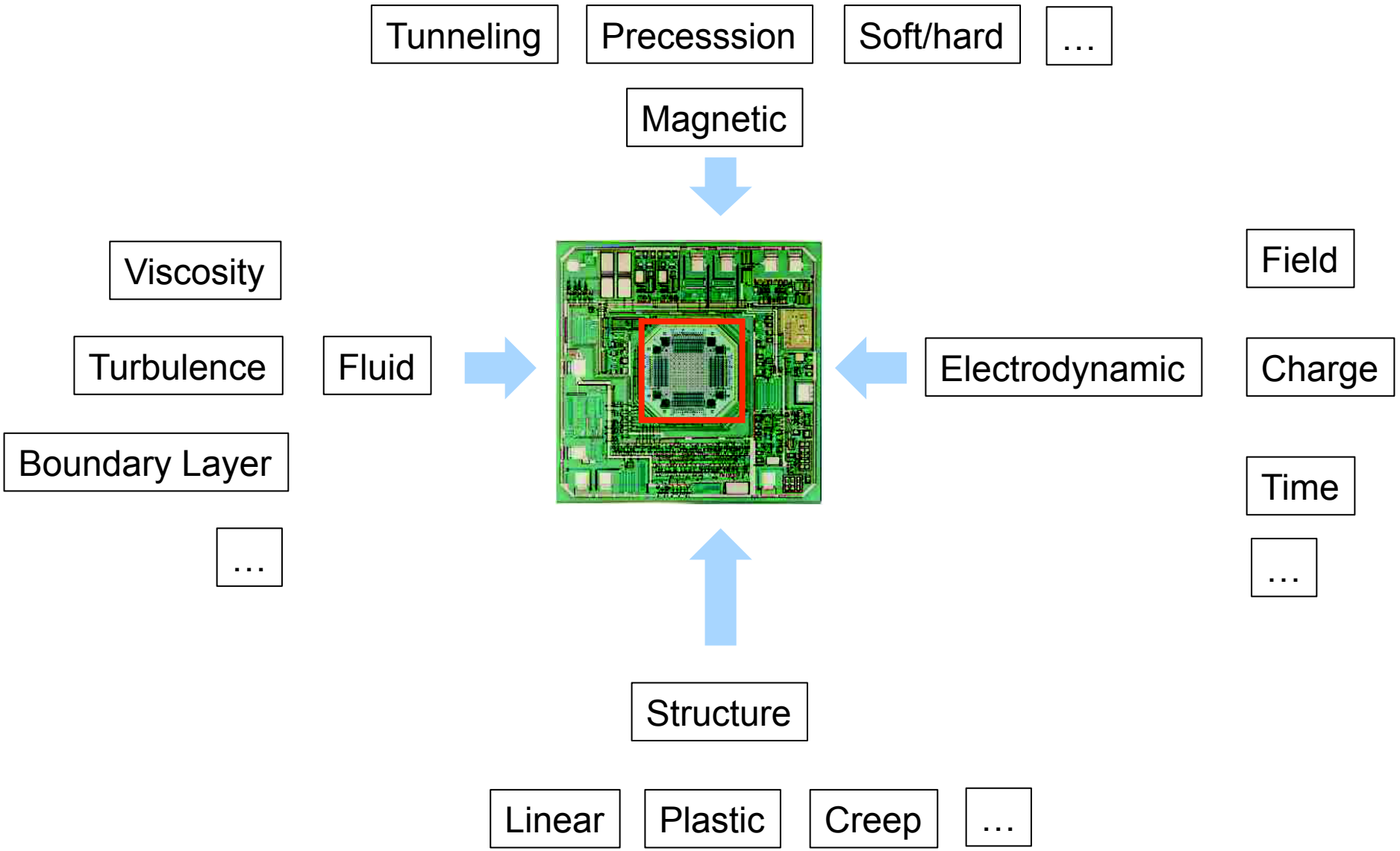
Consequences

- We don't really know how to judge what works and what doesn't work?
- What is robust and what is not?
- What energy and power in changing signals?
- What are process technology interactions and effects?
- Thermal, Temporal,

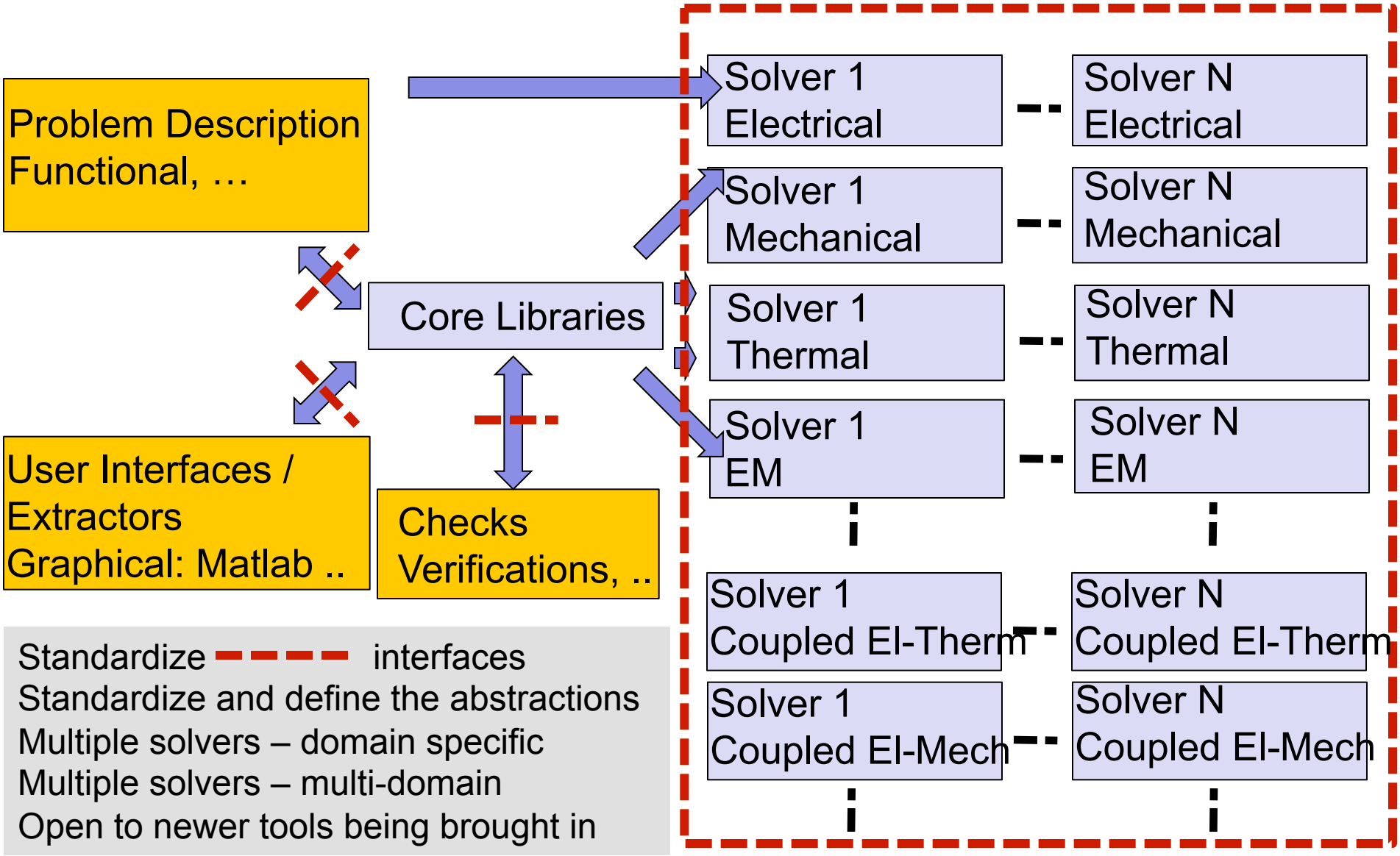

Behavioral
Structural
"Beyond CMOS" !
System
Algorithm
Registers
Boolean Expr
Differential Eq
CPU, Memory
Controller, Netlist
ALU, Register,
MUX
Gate, FlipFlop
Transistors
Ab Initio
Compontent
Device
Function
Algorithm
System
Polygons
Cells, Modules
Floorplans
Blocks
Boards
Systems
Growth
Deposition
Anneals
Lithography
Etching
ILD
Packaging
Physical
Process


Scale
100 nm
Continuum & Bulk
Classical
Continuum & Nano
100 nm
Semi-Classical
Physics
QM
Molecular Dynamic
10 nm
Tight Binding
nm
Ab Initio

An Example: Fluid-Magnetic-Electric-Mechanical



Build A New Open Infrastructure



Standardize ---- interfaces
Standardize and define the abstractions
Multiple solvers – domain specific
Multiple solvers – multi-domain
Open to newer tools being brought in