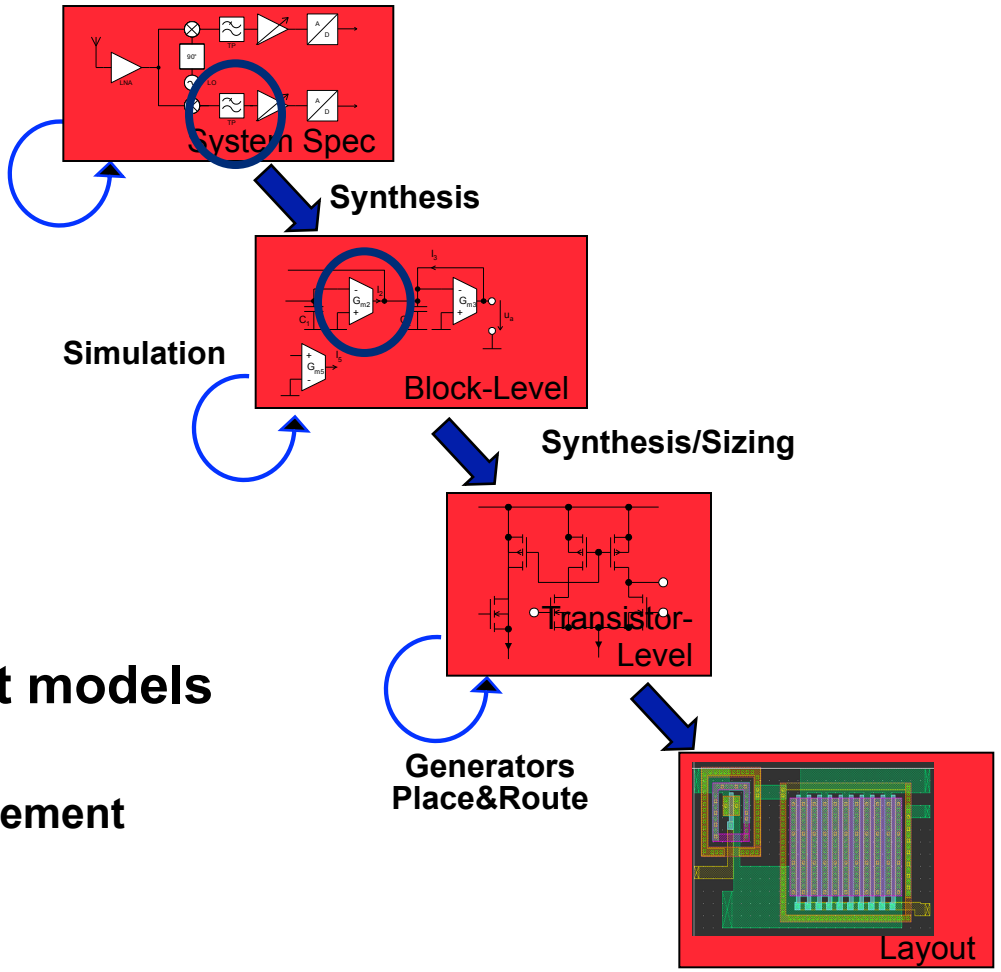
Panel Design

Lars Hedrich, University of Frankfurt, Germany

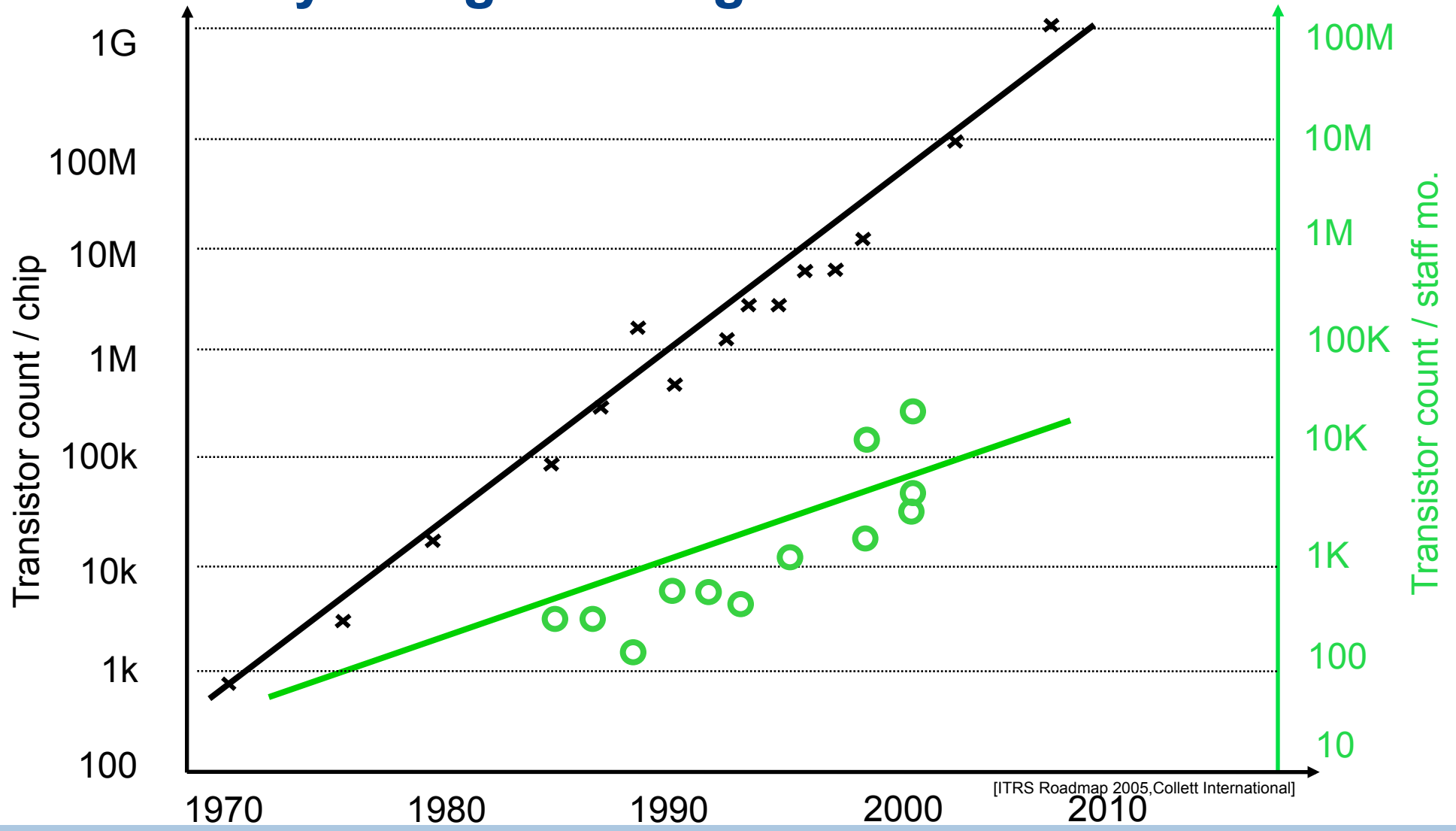
NanoTec Workshop 2011

Design-Flow of Mixed-Signal Chips / Systems

- **Highly sophisticated, mostly automated methodology**
- **Meet in the middle:**
  - **Rely on (digital) libraries**
- **Industry tend to stick to compact models**
  - **Stochastic**
  - **Quantum effects even harder to implement**



Productivity in Digital Design



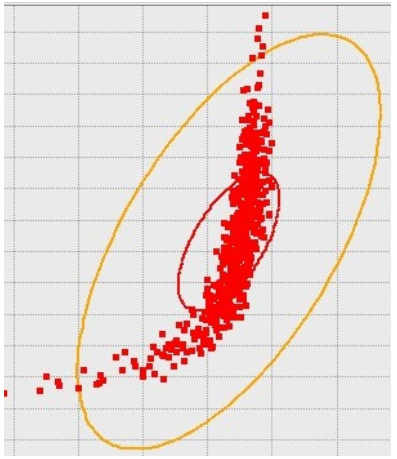
Productivity Issues

- Synthesis is the working horse
  - Relies on Boolean functionality and libs
  - Some (University) research on reversible logic
  - …

If digital libraries could be provided =>
System design could be straight forward
and cheap

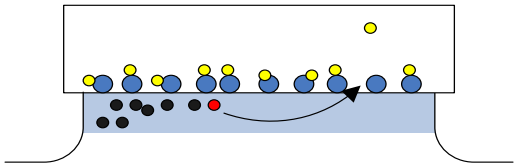
- However Place & Route could be hard
  - Parasitic capacitances, buried gates
  - Opportunities: 3D-Integration (just evolving)
- To compete with CMOS: Productivity should scale like in former times

Reliability Issues



- Design and EDA community try to accept unreliability issues
  - SEV, probabilistic failures
  - Degrading or increasing local yield distributions

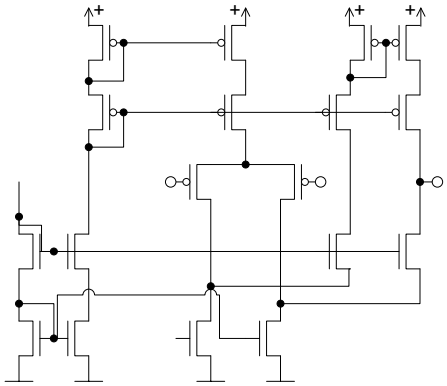
  => Could initiate “computing on uncertain hardware”
- Incorporate reliability issues took > 5 years



Unreliability technologies and low yield could be handled on many levels of abstraction

Design Issues

- Analog parts harder to design
  - Better transistor properties needed than digital
    - Matching
    - Gain
    - FT
- Design process relies on continuous simulations
  - Fundamental change needs total new simulation techniques



Design Issues

- Analog parts
  - Better tra
    - Match
    - Gain
    - FT
- Design proc
  - Fundame

Summary

- **Digital library cells needed for mass high complexity products**
- **Niche performance could drive a technology**
- **New paradigms (quantum, synapse) needed totally new designers and EDA**