BENCHMARKING BEYOND CMOS DEVICES

D. VERKEST

imec

BENCHMARKING BEYOND CMOS DEVICES

imec

CMOS SCALING:THE BAD

Switching heat/cm^2 ~ $(V_{DD}/\lambda)^3$ → ↓

V_{DD} ↑

Leakage Power ~ $\exp(-mV_T/kT)$ → V_T

Clock $F_{cl} \sim I_{on}/V_{DD} \sim \mu (V_{DD} - V_T)^{0.5}/\lambda$ → Clash

Device variability $\sigma V_T \sim 1/\lambda$ → σF_{cl}

Interconnect RC delay

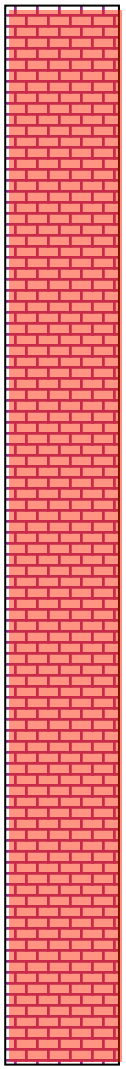
CMOS SCALING: THE GOOD

- "Zero" static power: symmetric n and p FET
- Simple (planar) layout strategy (litho compatible)
- Symmetric I/V → bidirectional switch
- Gain: signal restoration, noise margin, RF and analog
- W/L sizing → Fanout 1 ... 10^6
- Connectable by 10+ wiring layers
- Low manufacturing cost: < 1 n$/transistor
- Design technology and IP libraries
- Versatile: logic, storage, interconnect, I/O, analog, ...

→ **complete System**-on-Chip

BENCHMARKING BEYOND CMOS DEVICES

Beyond CMOS device inventor



The CMOS designer

Source: W. Joyner, IBM

BENCHMARKING BEYOND CMOS DEVICES

Beyond CMOS device inventor

=

Hey, here's a *great* new device …

- It's really cool! It looks useful!
- We actually made one!
  It worked!

The CMOS designer

Source: W. Joyner, IBM

BENCHMARKING BEYOND CMOS DEVICES

Beyond CMOS device inventor

Hey, here's a *great* new device …

- It's really cool! It looks useful!
- We actually made one! It worked!

The CMOS designer

… but I can't do ***design*** with them

- I don't understand them.
- You can't characterize them, model them, simulate them, make them in volume, . . .

Source: W. Joyner, IBM

BENCHMARKING BEYOND CMOS DEVICES

Beyond CMOS device inventor

Hey, here's a *great* new device …

- It's really cool! It looks useful!
- We actually made one! It worked!

SYSTEMABILITY

The CMOS designer

… but I can't do ***design*** with them

- I don't understand them.
- You can't characterize them, model them, simulate them, make them in volume, . . .

Source: W. Joyner, IBM

SYSTEMABILITY

The ability to economically design and manufacture reliable systems from the interaction of devices fabricated in a given technology.

SYSTEM = COMPUTATION, STORAGE, INTERCONNECT, I/O, (ANALOG)

Every contender

- Must add value to one or more of the 4 system functions and be compatible with the others
- All-in throughput/Watt and/or transactions/Joule must beat CMOS at time of manufacturing at equivalent or lower cost
- System level manufacturability, reliability, testability must beat ultimate CMOS solutions
- Room temperature operation is mandatory
- Device variability must be mitigated and modeled and cost efficient error resilient design solutions must be available
- Design methods and tools must be in place supporting design from device to system. Design tool development time is 3x technology development time.

BENCHMARKING BEYOND CMOS DEVICES

Beyond CMOS device inventor

Hey, here's a *great* new device …

- It's really cool! It looks useful!
- We actually made one! It worked!

PDK

Pathfinding

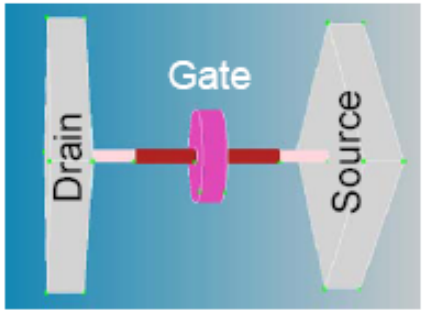
The CMOS designer

… but I can't do ***design*** with them

- I don't understand them.
- You can't characterize them, model them, simulate them, make them in volume, . . .

Source: W. Joyner, IBM

IMEC INSITE PATHFINDING INITIATIVE
LINKING PROCESSES, DEVICES, CIRCUITS, SYSTEMS



Architecture + models (TCAD)

Simplified circuit models

SlewAxis = [12.5 125 250 625 1250] ps

TDELAY (ns) =
[0.006254 0.015746 0.031686 0.068524 0.164907
0.019463 0.032747 0.050290 0.089016 0.185832
0.028944 0.046620 0.067449 0.107620 0.207008
0.045504 0.069108 0.096166 0.138539 0.246567
0.068189 0.122788 0.182575 0.229775 0.355785] ;

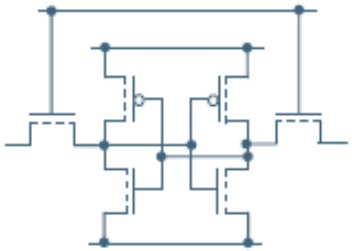
TTRANS (ns) =
[0.011796 0.037772 0.081873 0.184887 0.451113
0.021729 0.045590 0.087022 0.189108 0.463147
0.031871 0.057616 0.098460 0.198298 0.470681
0.047384 0.079744 0.122761 0.208534 0.484796
0.087580 0.131710 0.187385 0.291257 0.545090] ;

LoadAxis = [1 50 100 200 500] pF

Digital speed

Layout Strategy!!!

Place/route incl. interconnect



SNM
WM
I_{read}
I_{cell}
I_{BL}

MC

Yield (V_{dd})

Statistics: $\sigma_{\Delta Vt}$, $\sigma_{\Delta\beta}$

BENCHMARKING BEYOND CMOS DEVICES

imec

BENCHMARKING BEYOND CMOS DEVICES

imec

BEYOND DEVICES

BEYOND

BESIDE

In the spirit of

Thomas J. Watson

BE IN

"I think there is a world market for maybe five computers."

BE NOT

BEYOND DEVICES

BEYOND

BESIDE

- Molecular electronics (plastic/organic)

BE IN

BE NOT

BEYOND DEVICES

BEYOND

BESIDE

- Molecular electronics (plastic/organic)
- MEMS (complementary/on-top-off)

BE IN

BE NOT

BEYOND DEVICES

BEYOND
- Quantum Computing

BESIDE
- Molecular electronics (plastic/organic)
- MEMS (complementary/on-top-off)

BE IN

BE NOT

BEYOND DEVICES

BEYOND
- Quantum Computing

BESIDE
- Molecular electronics (plastic/organic)
- MEMS (complementary/on-top-off)

BE IN
- Spintronics

BE NOT

BEYOND DEVICES

BEYOND
- Quantum Computing

BESIDE
- Molecular electronics (plastic/organic)
- MEMS (complementary/on-top-off)

BE IN
- Spintronics
- Nanowires

BE NOT

BEYOND DEVICES

BEYOND
- Quantum Computing

BESIDE
- Molecular electronics (plastic/organic)
- MEMS (complementary/on-top-off)

BE IN
- Spintronics
- Nanowires
- Memristors

BE NOT

BEYOND DEVICES

BEYOND
- Quantum Computing

BESIDE
- Molecular electronics (plastic/organic)
- MEMS (complementary/on-top-off)
- Graphene

BE IN
- Spintronics
- Nanowires
- Memristors
- Graphene

BE NOT