Neuromorphic Computing

- Memristors -

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UNIVERSITÉ PARIS SUD

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erc Nanobrain

Outline

1- memristor devices : introduction

2- memristors as digital memory

3- memristors for logic applications

4- memristors for neuromorphic computing

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1- memristor devices : introduction

2- memristors as digital memory

3- memristors for logic applications

4- memristors for neuromorphic computing

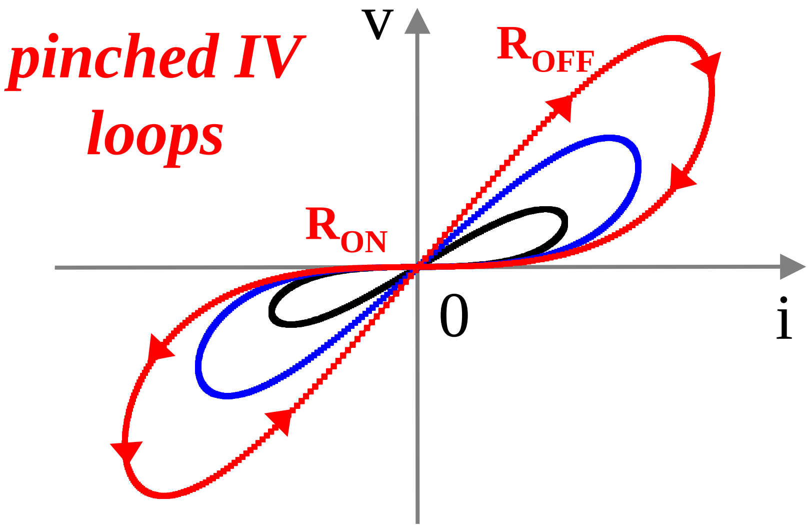
Memristor

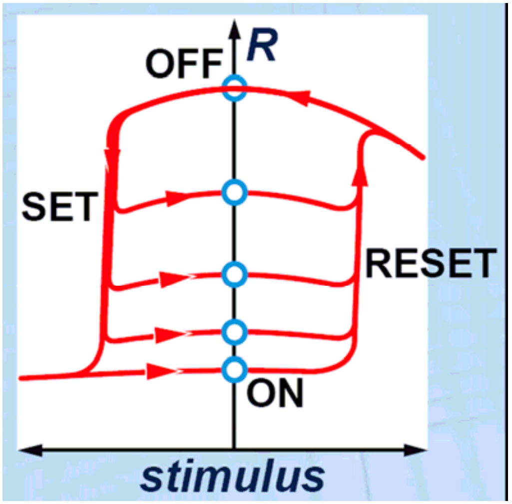
L. O. Chua, "memristor – the missing circuit element" IEEE Trans. Circuit Theory (1971)

$$\boxed{v = M(q)\ i}$$

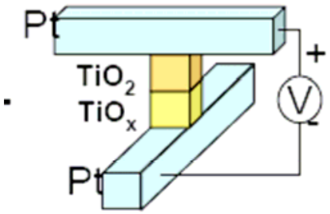
M(q) = R(q) continuously tunable between R_{ON} and R_{OFF}

M=aq+b



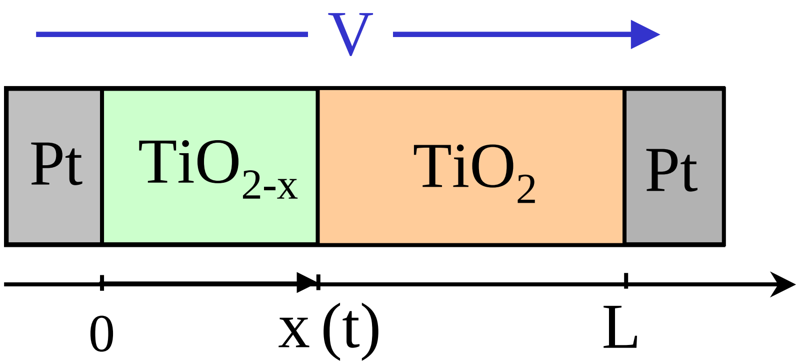


Hewlett-Packard Memristor

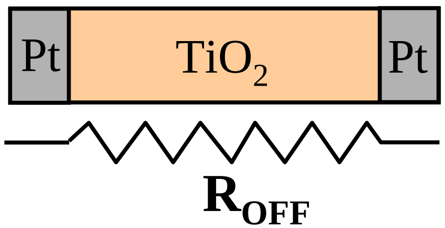


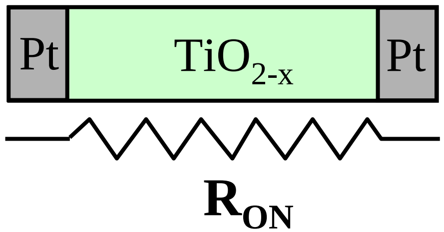
< 30x30 nm^2

migration of oxygen vacancies



$$\frac{R_{OFF}}{R_{ON}} > 1000$$





$$R = R_{ON}\frac{x}{L} + R_{OFF}\left(1 - \frac{x}{L}\right)$$

displacement proportional to the charge

$$\boxed{x \propto q}$$

$$\boxed{M(q) \cong R_{OFF}\left[1 - \mu\frac{R_{ON}}{L^2}q\right]}$$

Strukov, Snider, Stewart & Williams, Nature 453 (2008)

Hewlett-Packard Memristor

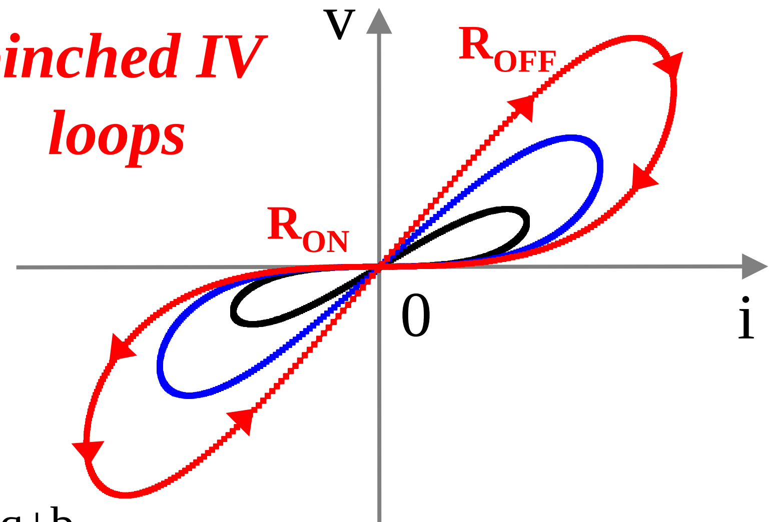
L. O. Chua, "memristor – the missing circuit element" IEEE Trans. Circuit Theory (1971)

$$\boxed{v = M(q)\, i}$$

M is a resistance that "remembers" how much current was injected, and how long

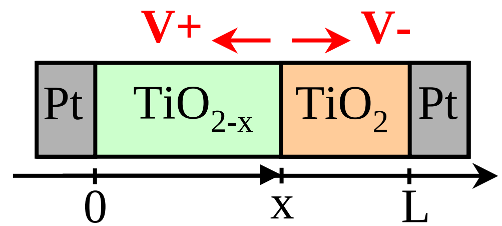
continuously tunable between R_{ON} and R_{OFF}

pinched IV loops



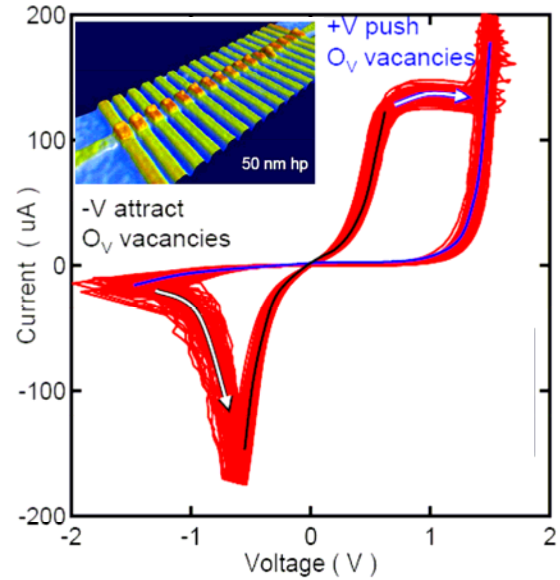
M=aq+b

the HP memristor



ions electromigration

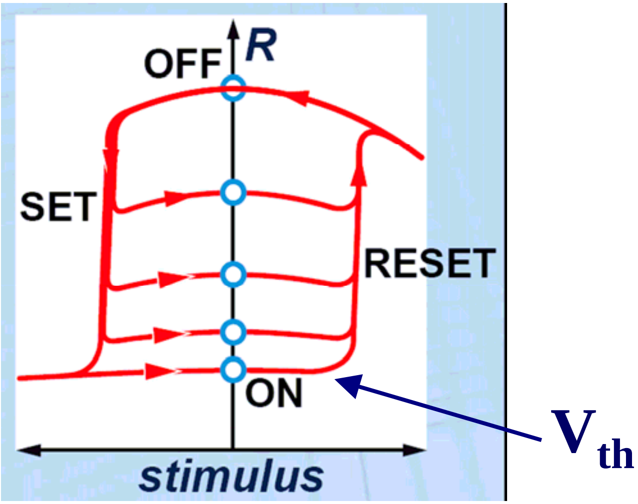
Yang et al., Nature Nano (2008)



Memristor

Memristor =

- **Nano resistance**
- **Tunable (multi-states of resistance available)**
- **Non volatile**
- **Non-linear : $V < V_{th}$ read, $V > V_{th}$ write**



Memristor technologies

After (and even before) Hewlett-Packard TiO_2 memristor was proposed, many other very different memristor concepts were identified :

Erokhin et al., Surface and thin films (2007) PANI
A.A. Zakhidov et al., Organic elec. (2009) metal/mixed conductor/metal
F. Alibart et al., Advanced Func. Mater. (2009) Pentacene + gold particles
Ben Jamaa et al., IEEE Nano (2009) Poly-cristalline Si nanowires
Derycke et al., TNT (2009) Carbone nanotubes
Driscol et al., APL (2009) Phase change material
Gergel et al., IEEE EL (2009) flexible TiO2
Jo et al., Nanoletters (2009) Ag/Si
Wang et al., IEEE EL (2009) spintronics
Kim et al., Nanoletters (2009) nanoparticle assemblies
Jeong et al., Nanoletters (2010) graphene
Lee et al., Nature Materials (2011) Ta2O5
Ohno et al., Nature Materials (2011) atomic switches
Chanthbouala, Grollier et al., Nature Physics (2011) spintronics
….

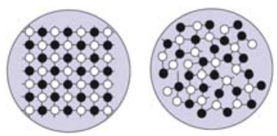
In particular, all resistive switching devices are memristors

Memristor classification

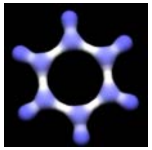
Red-Ox

$$MX + \delta e^{-} \rightleftharpoons MX_{1-\delta} + \delta X^{-}$$

Phase change



Organic



Purely electronic effects

Memristor classification

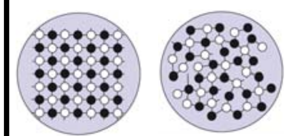
Red-Ox

$MX + \delta e^-$

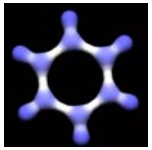
$\uparrow\downarrow$

$MX_{1-\delta} + \delta X^-$

Phase change



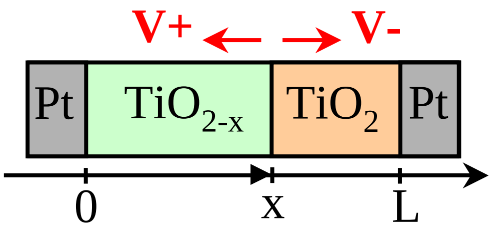
Organic



Purely electronic effects

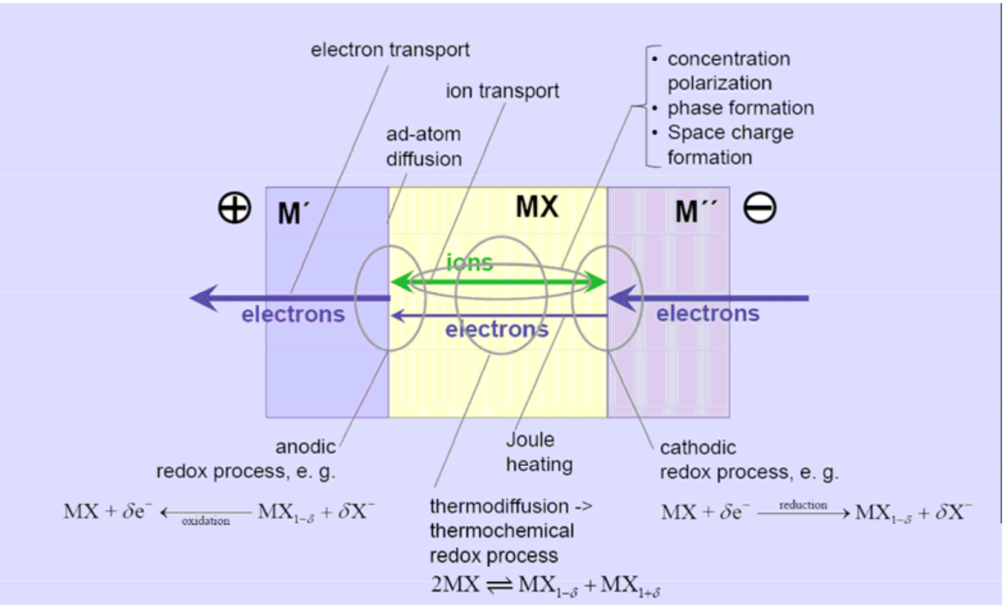
Red-Ox memristors

ex : the HP memristor



ions electromigration

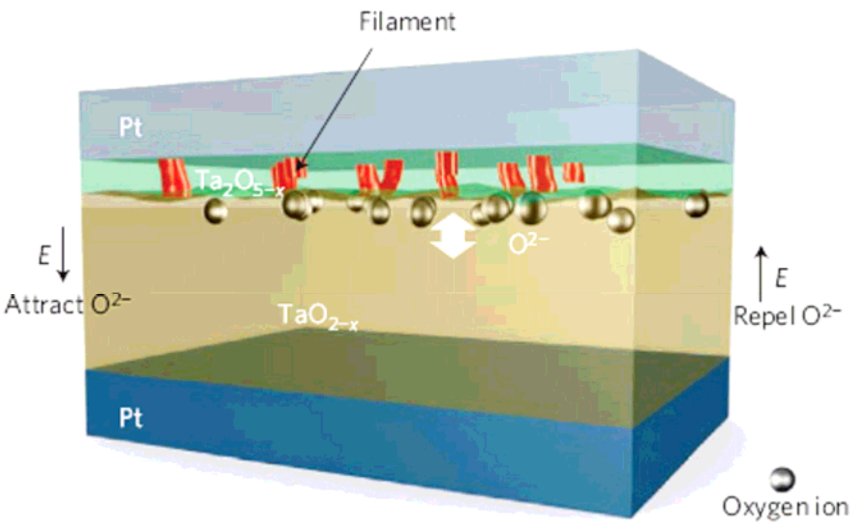
R. Waser *et al.*, talk at ISIF 2001



Resistance changes due to a mix of : reduction-oxidation processes, ionic motion, phase transition and thermal effects

Red-Ox memristors : TaO_x

M-J. Lee *et al*., Nature Mat. 2011



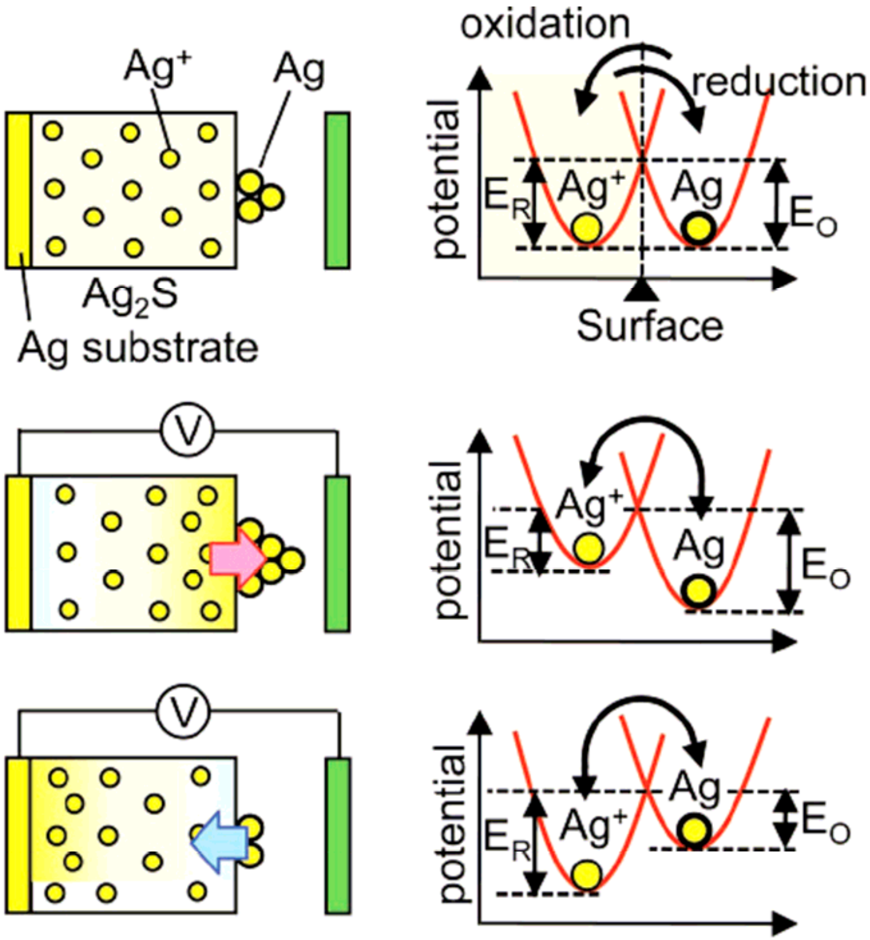
Formation of conductive filaments

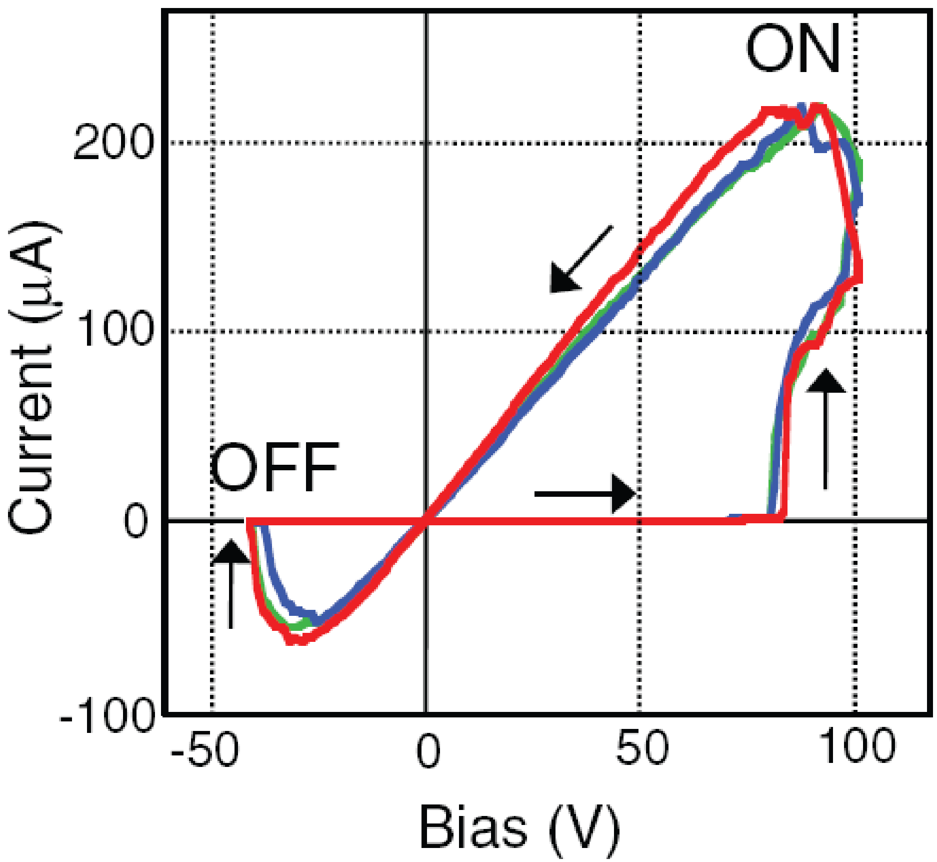
Pt/TaO_x/Pt

Szot, Waser et al., Nanotechnology 2011 :
TiO_2, a prototypical memristive material

The physics of the Pt/TiO_2/Pt memristor is not as simple as originally described by HP team : filaments / phase change

Red-Ox memristors : atomic switch



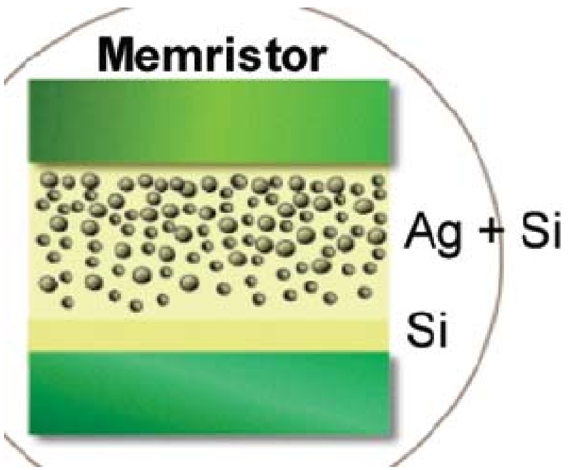


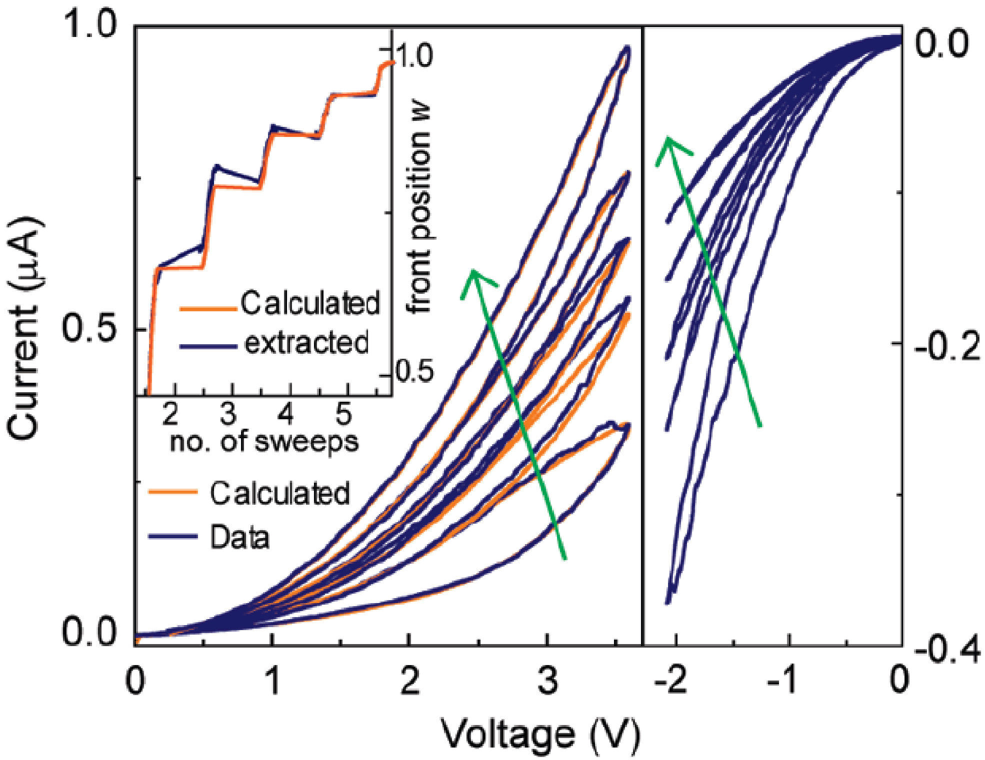
Diffusion of Ag^+ cations and reduction to Ag

Hasegawa, Aono et al, Adv Mater 2012

Red-Ox memristors : co-sputtered Ag/Si

Jo, Lu *et al.*, Nanoletters 2009





Ag in Si matrix

Co-sputtering : gradient of Ag

No forming process

Continuous propagation of the conductive front

Memristor classification

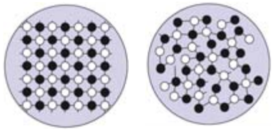
Red-Ox

$MX + \delta e^-$

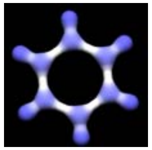
$\uparrow\downarrow$

$MX_{1-\delta} + \delta X^-$

Phase change



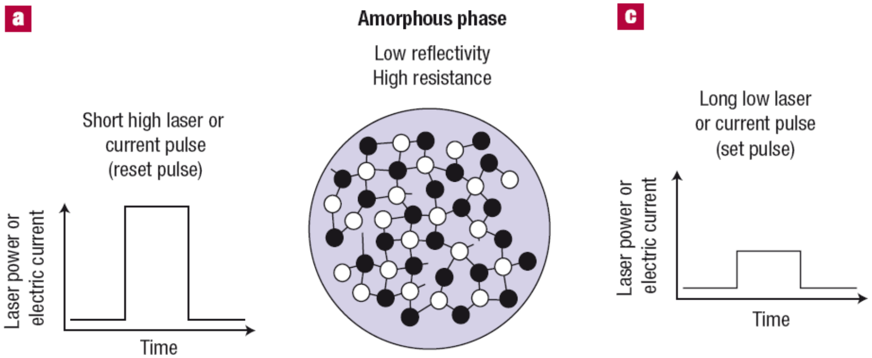
Organic



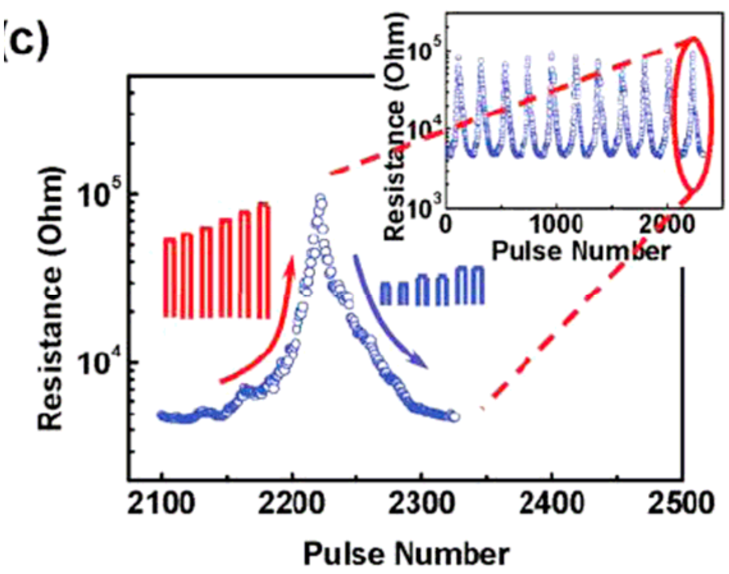
Purely electronic effects

Phase change memristors

ex : chalcogenide glass ($Ge_2Sb_2Te_5$)



Waser et al., Nature Mat. 2007



Kuzum et al., Nanoletters 2011

Phase change memristor : unipolar switching → complications

Memristor classification

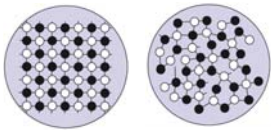
Red-Ox

$MX + \delta e^-$

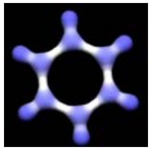
$\uparrow\downarrow$

$MX_{1-\delta} + \delta X^-$

Phase change



Organic



Purely electronic effects

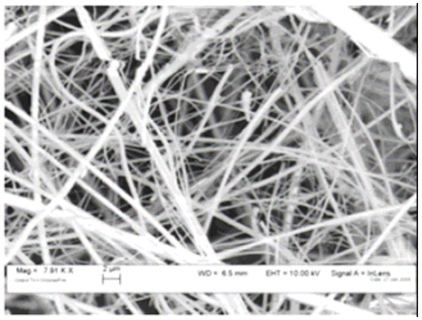
Organic Memristor

- ***Organic memristors :*** NOMFET (polymer), CNT-FET, PANI….

- additional functionalities
ex : interaction with light

- bottom up approach
ex : self-organization

- high density



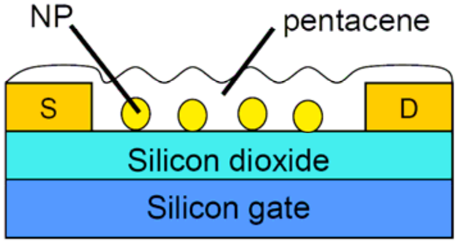
Erokhin et al., NanoNet 2009

- very promising

- time scale > 10 years

Physical origin : charge trapping effects
problem of memory retention time (< 1 h)

The gold nanoparticles = nanoscale capacitance to store the electric charge
Transistor transconductance tuned by charge amount



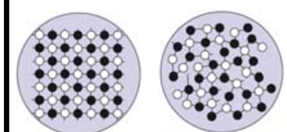
F. Alibart *et al.*, Advanced Func. Mater. (2009)

Memristor classification

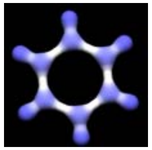
Red-Ox

$$MX + \delta e^- \rightleftharpoons MX_{1-\delta} + \delta X^-$$

Phase change



Organic



Purely electronic effects

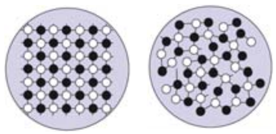
Purely electronic effects memristors

Red-Ox

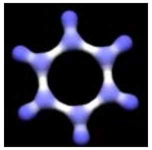
$MX + \delta e^-$

$MX_{1-\delta} + \delta X^-$

Phase change



Organic



Purely electronic effects

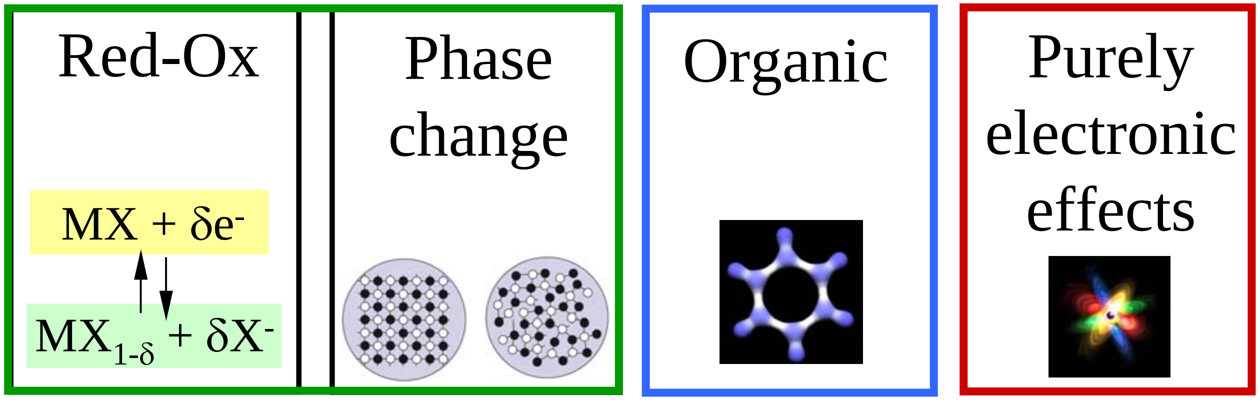
- defect-mediated : thermal effects, ionic motion

ex : HP memristor based on electromigration : reliability / endurance issues

- large local heating
- need of a forming step
- physics not understood

- promising

Purely electronic effects memristors



obtain memristive effects by purely electronic physical mechanisms

Spintronic memristor (MRAM based)

A. Chanthbouala, J. Grollier, R. Matsumoto, V. Cros, A. Anane, A. V. Khvalkovskiy, A. Fert

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A.M. Prokhorov General Physics Institute of RAS, Russia
Istituto P.M. s.r.l., Italy

K. Nishimura, Y. Nagamine, H. Maehara, K. Tsunekawa

Process Development Center, Canon ANELVA Corporation, Japan

A. Fukushima, and S. Yuasa

National Institute of Advanced Industrial Science and Technology (AIST), Japan

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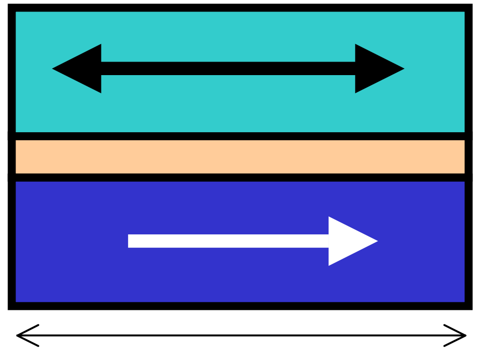
Spintronic memristor

Magnetic tunnel junction



Ferromagnetic metal 1 - free

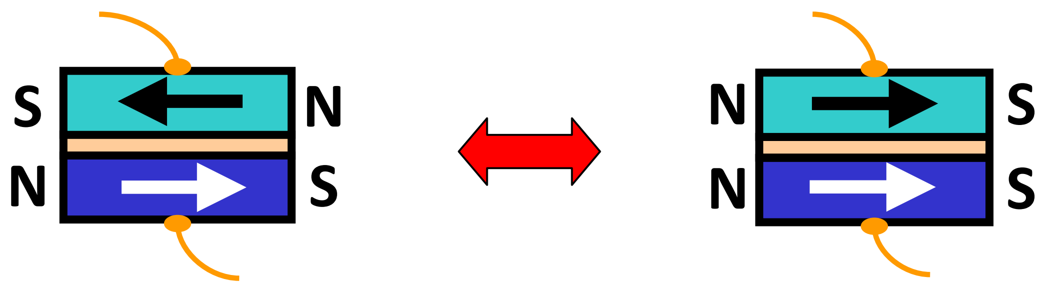
Thin insulator ~ 1-2 nm thick

Ferromagnetic metal 2 - fixed

~ 20 – 300 nm

Changing the magnetic configuration = changing the resistance

Anti-parallel state (**AP**) Parallel state (**P**)

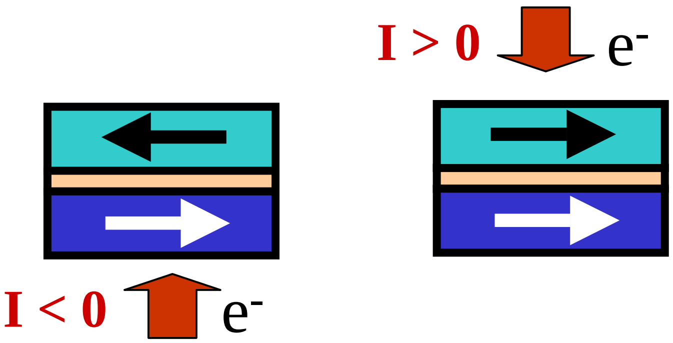


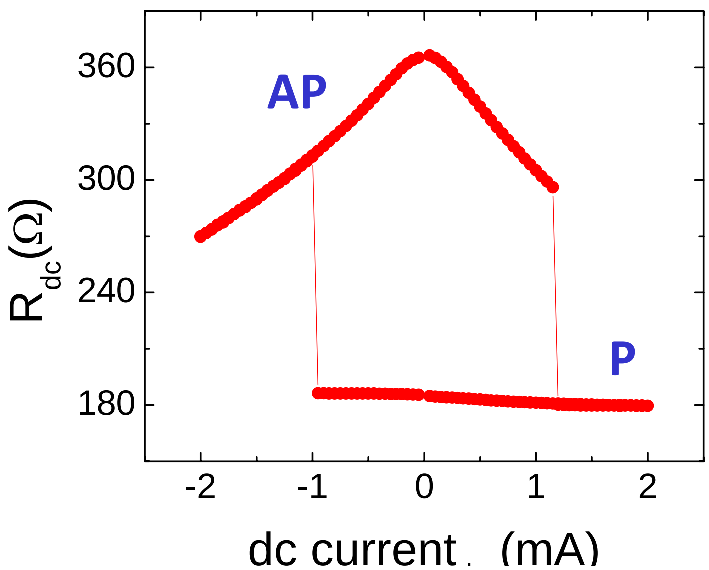
R_{AP} (logical 1) R_P (logical 0)

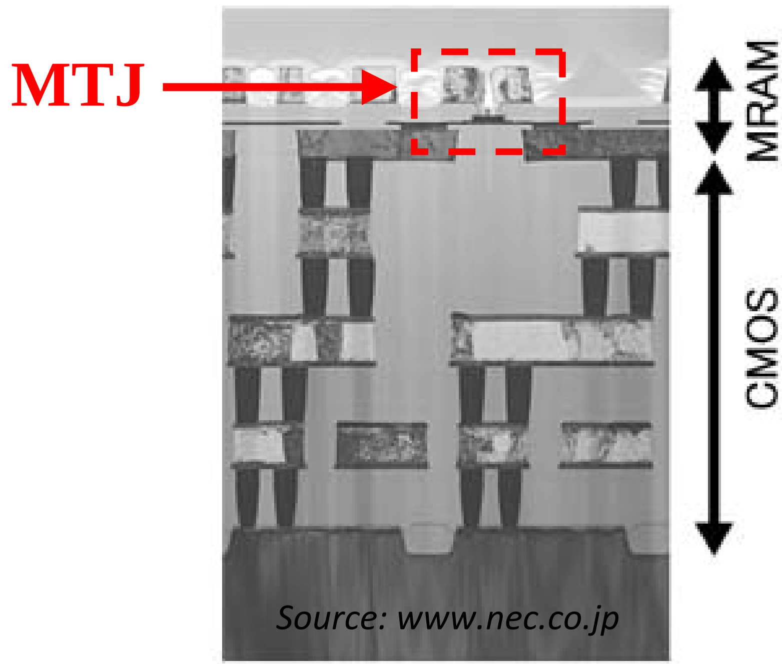
Tunnel Magneto-Resistance (TMR)

MTJ : controlling the resistance

- **with a dc current (spin torque)**



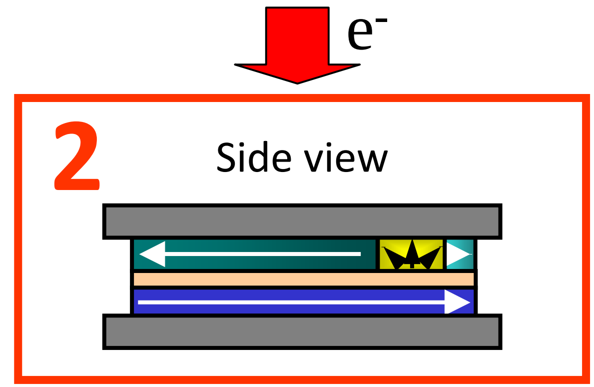


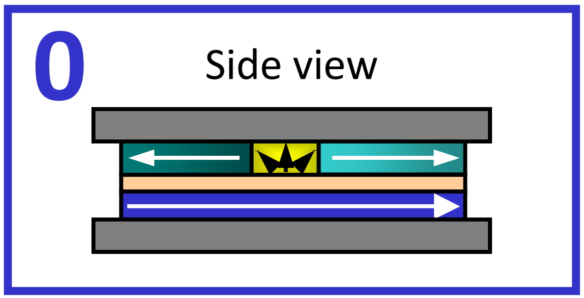


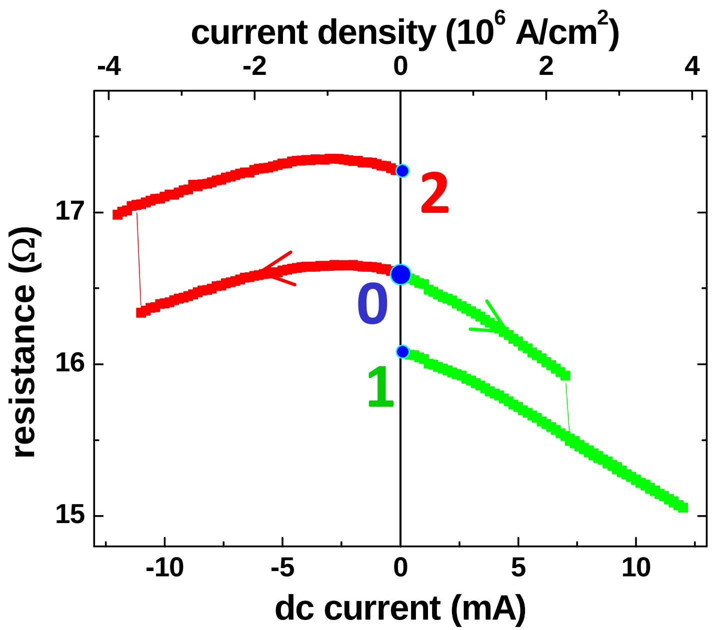
- Will be used to store information in the future STT-MRAM (Magnetic Random Access Memory)
- out to market in < 5y
- Target : D-RAM applications

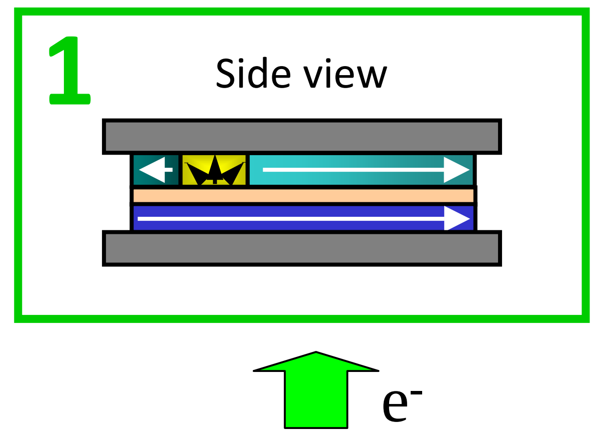
Spintronic memristor

A. Chanthbouala, JG *et al.*, Nature Phys., 2011









Idea : introduce a magnetic domain wall

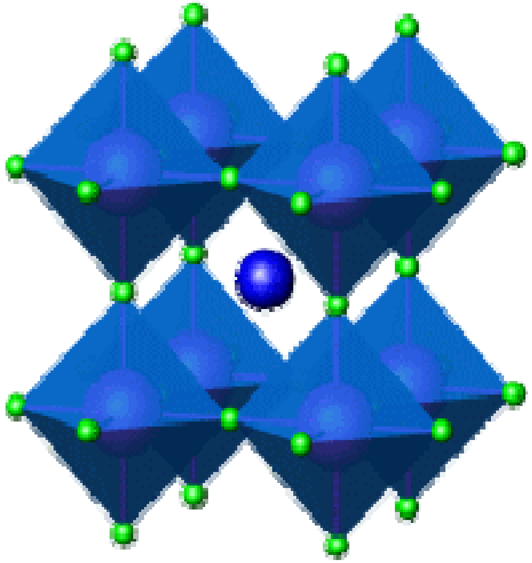
→ multi-resistance state memory

→ sub-ns switching

Ferroelectric memristor

**André Chanthbouala[1], Vincent Garcia[1] , Arnaud Crassous[1], Ryan Chérifi[1],
Karim Bouzehouane[1], Stéphane Fusil[1], Xavier Moya[2], Stéphane Xavier[3], Cyrile Deranlot[1], Neil Mathur[2],
Manuel Bibes[1], Julie Grollier[1] & Agnès Barthélémy[1]**

[1]Unité Mixte de Physique CNRS-Thales, Palaiseau, France
[2]Department of Materials Science, University of Cambridge, UK
[3]Thales Research and Technology, Palaiseau, France



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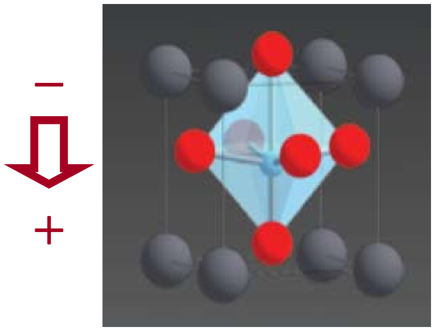
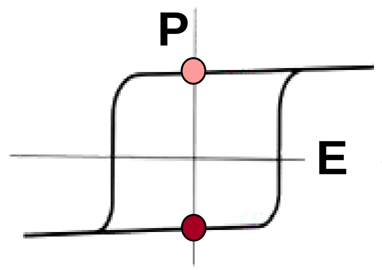
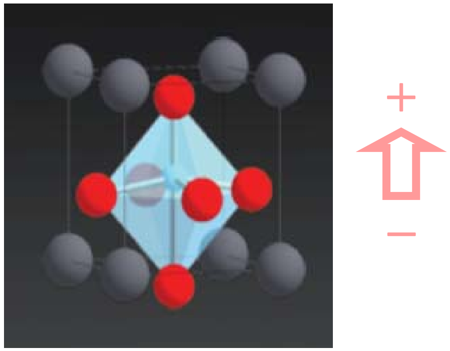
Ferroelectric memristor

Switching of the polarization with an electric field

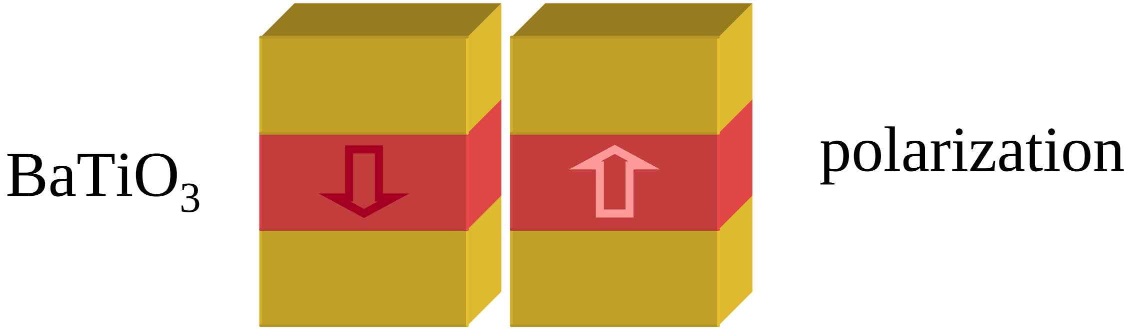
Ferroelectrics







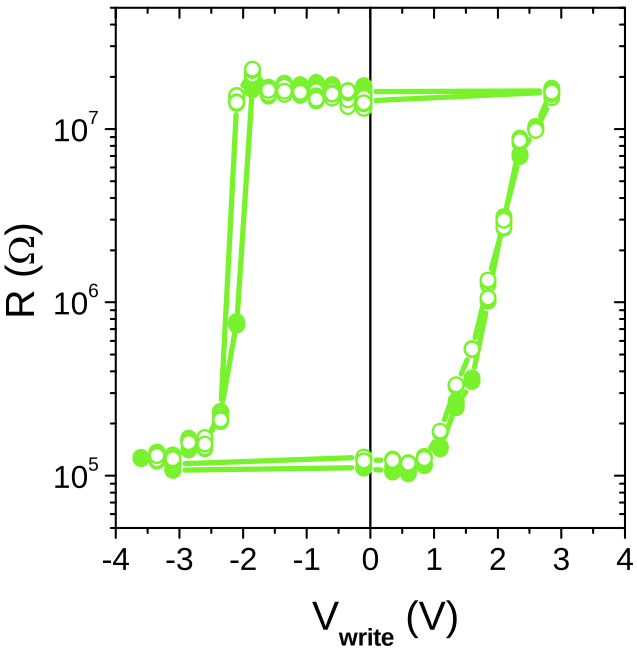
Ferroelectric tunnel junctions

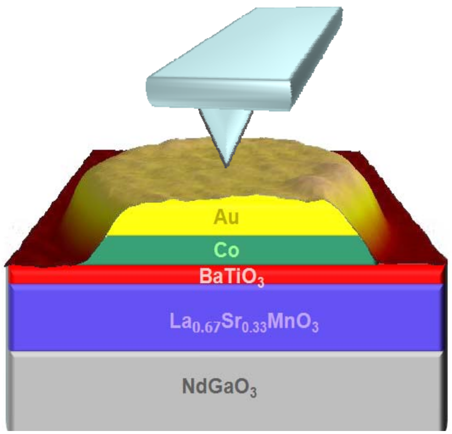


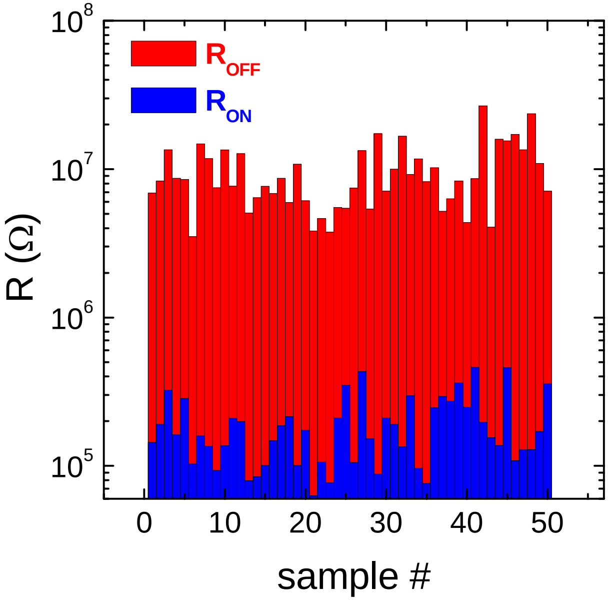
Low $R = R_{ON}$ Large $R = R_{OFF}$

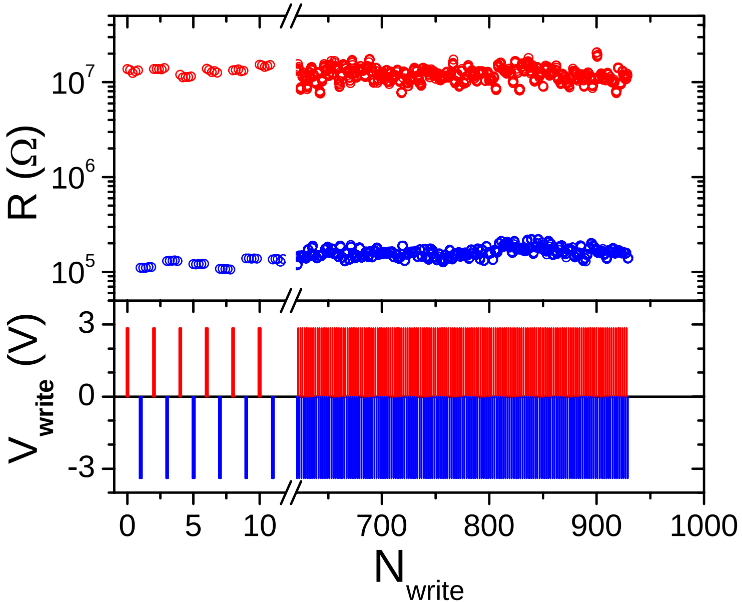
Garcia *et al.*, Nature **460**, 81 (2009)

Ferroelectric vs Resistive switching









Cyclability measurements limited by tip drift

Reproducible, fast (10 ns pulses) and reversible switching

A. Chanthbouala, JG *et al.* Nature Nano. 2011

Outline

1- memristor devices : introduction

2- memristors as digital memory

3- memristors for logic applications

4- memristors for neuromorphic computing

Memristors as memory

Hewlett-Packard annouced ReRAM out on the market in 2013 !

Last 5 years : large improvements of memristor devices performance

→ switching speed
→ endurance, reliability etc.

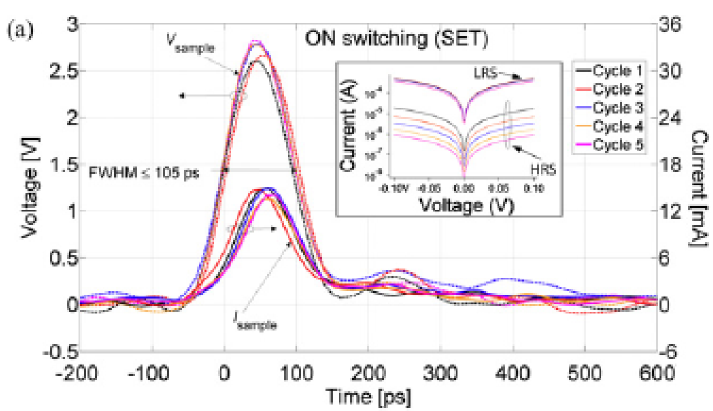
Memristors as memory : switching speed

IOP PUBLISHING NANOTECHNOLOGY

Nanotechnology **22** (2011) 485203 (7pp) doi:10.1088/0957-4484/22/48/485203

Sub-nanosecond switching of a tantalum oxide memristor

Antonio C Torrezan, John Paul Strachan, Gilberto Medeiros-Ribeiro and R Stanley Williams



100 ps !

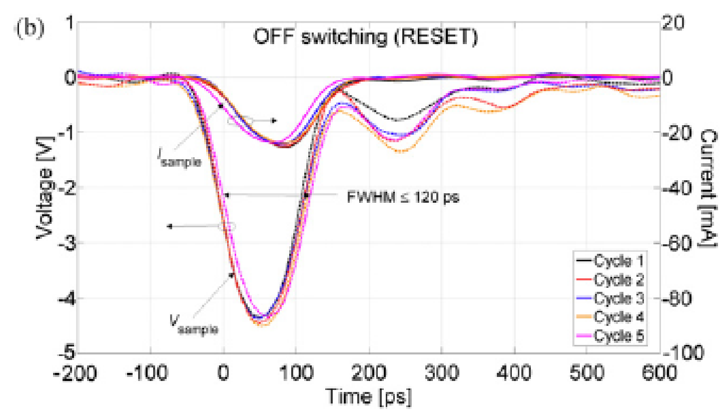


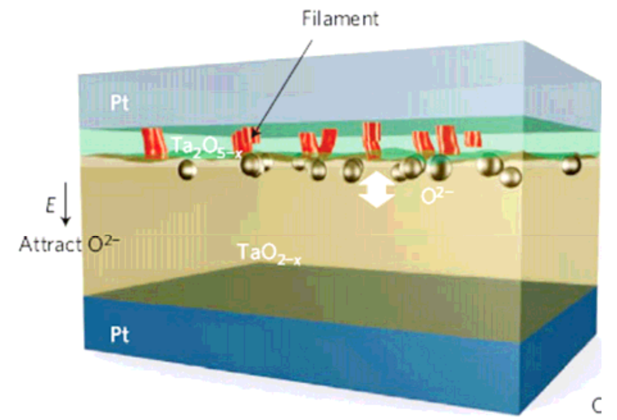
Figure 4. Fast (a) ON switching and (b) OFF switching of a 2 μm memristor over five consecutive cycles. The voltage across the sample V_{sample} and the sample current data I_{sample} are displayed as dashed and solid lines, respectively. The inset in (a) shows the low bias current–voltage sweep of the device resistance state after each SET and RESET operation.

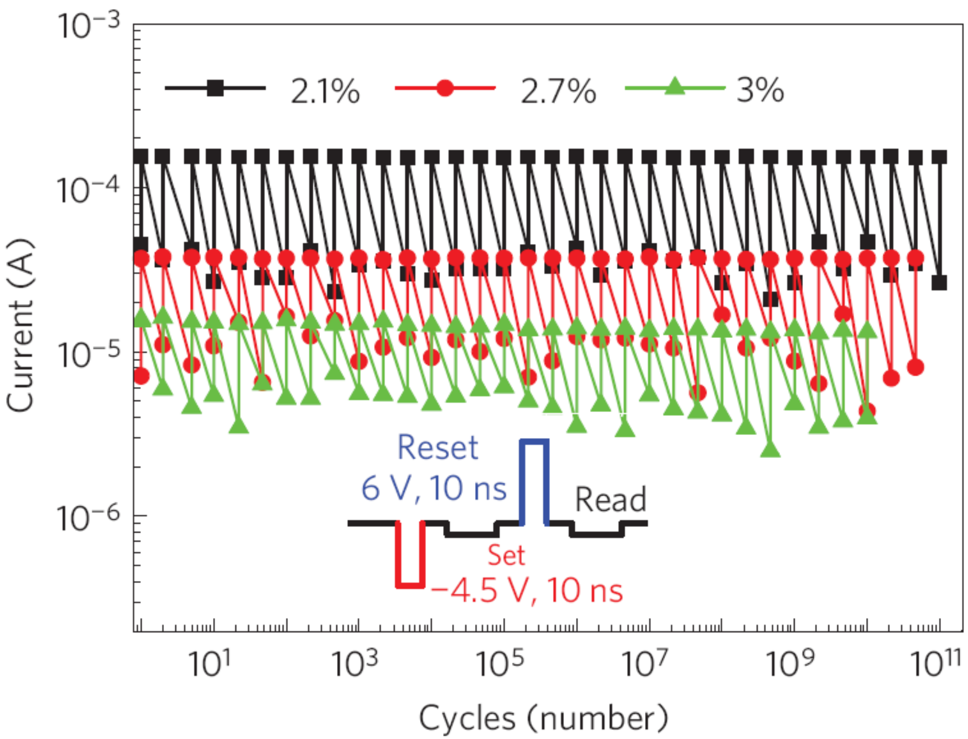
Memristors as memory : endurance

nature materials
ARTICLES
PUBLISHED ONLINE: 10 JULY 2011 | DOI: 10.1038/NMAT3070

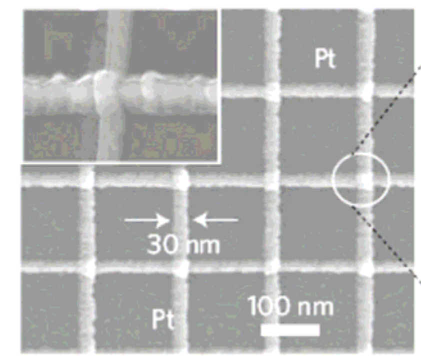
A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta_2O_{5-x}/TaO_{2-x} bilayer structures

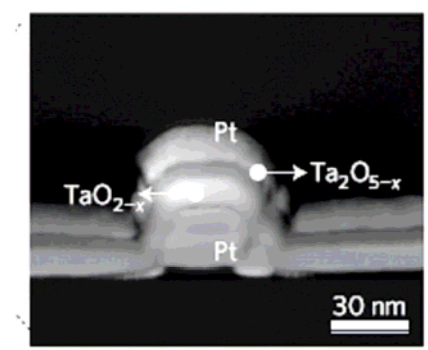
Myoung-Jae Lee[1]*, Chang Bum Lee[1], Dongsoo Lee[1], Seung Ryul Lee[1], Man Chang[1], Ji Hyun Hur[1], Young-Bae Kim[1], Chang-Jung Kim[1]*, David H. Seo[1], Sunae Seo[2], U-In Chung[1], In-Kyeong Yoo[1] and Kinam Kim[3]





10^{11} cycles





Technology *digital memristor*	**PCM**	**Red-Ox**	**FeTJ**	**STT**
Gain, Signal/Noise ratio **Non-linearity**	N/A			
Speed **Power consumption**	50 ns 6 pJ	10 ns < 1 pJ	10 ns 10 fJ	25 ns 0.02-5pJ
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	6 F^2	5/8 F^2	5/8 F^2	20/40 F^2
Other specific properties				
prototypes	commercial	some	---	yes
forming step	no	some	no	no
switching	unipolar	both	bipolar	bipolar
good theoretical understanding	yes	no	yes	yes
Manufacturability	CMOS compatible			
Timeline (When exploitable or when foreseen in production)	available	< 5 y	?	< 3 y

Memristors as memory : arrays

- **Challenges for memory to replace Flash & SRAM:**

  → Scale down below 15 nm
  + low power, high speed, dense, non-volatile

- **Memristor devices can be scaled down below 20 nm**

  → filament, atomic switch intrisically small

- **1 memory element = 1 storage device – 1 selector**

  → limiting element : selector ?

- **High enough OFF/On ratio : possibility to remove the selector**

  → crossbar array (10^3 x 10^3 → OFF/ON ratio 10^7)

  → or combine memristor type 1 : storage, memristor type 2 : selector

Memristors as memory SWOT

Strengths

- Scalability
- Non-volatility
- Multilevel
- Cost

Weaknesses

- physics ?
- forming step (to be removed)
- reliability / endurance

Opportunities

- crossbar arrays (no selector)
- 3D integration

Threats

- defects when scaling down
- reliability
- need to find agreement on the best technology (TiO_2, TaO_2, Atomic switch, Spintronic, Ferroelectric etc.)

Outline

1- memristor devices : introduction

2- memristors as digital memory

3- memristors for logic applications

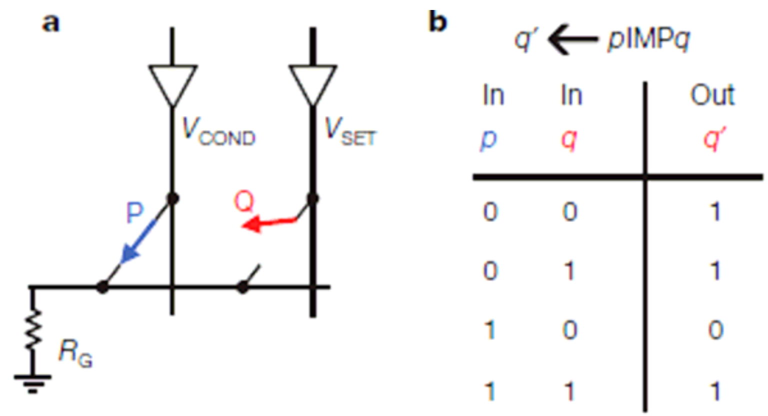
4- memristors for neuromorphic computing

Memristors for logic

If the OFF/ON ratio is large enough, memristors could be used as latches (replacing transistors)

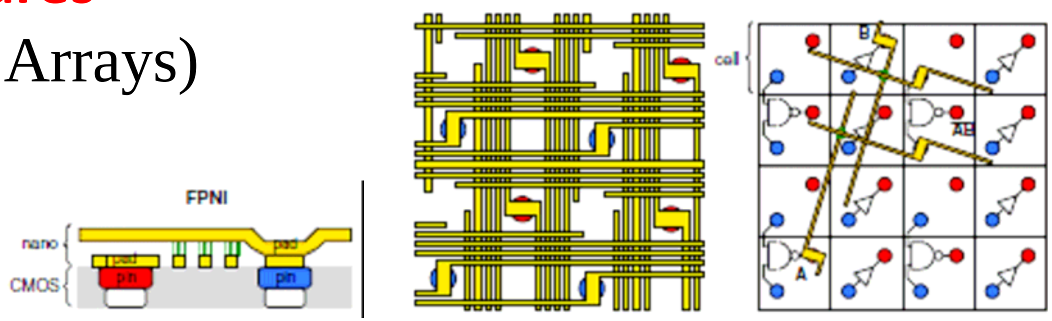
- **logic functions**

Kuekes et al., JAP 2005
Borghetti et al., Nature 2010



- **Reconfigurable Architectures**

(Field Programmable Gate Arrays)
Snider et al., Nanotechnology 2007
Field Programmable Nanowire Interconnect



A particularly good candidate is the atomic switch

Memristors for logic : atomic switch

ADVANCED MATERIALS 2012
www.advmat.de
MaterialsViews
www.MaterialsViews.com

Tsuyoshi Hasegawa,* Kazuya Terabe, Tohru Tsuruoka, and Masakazu Aono

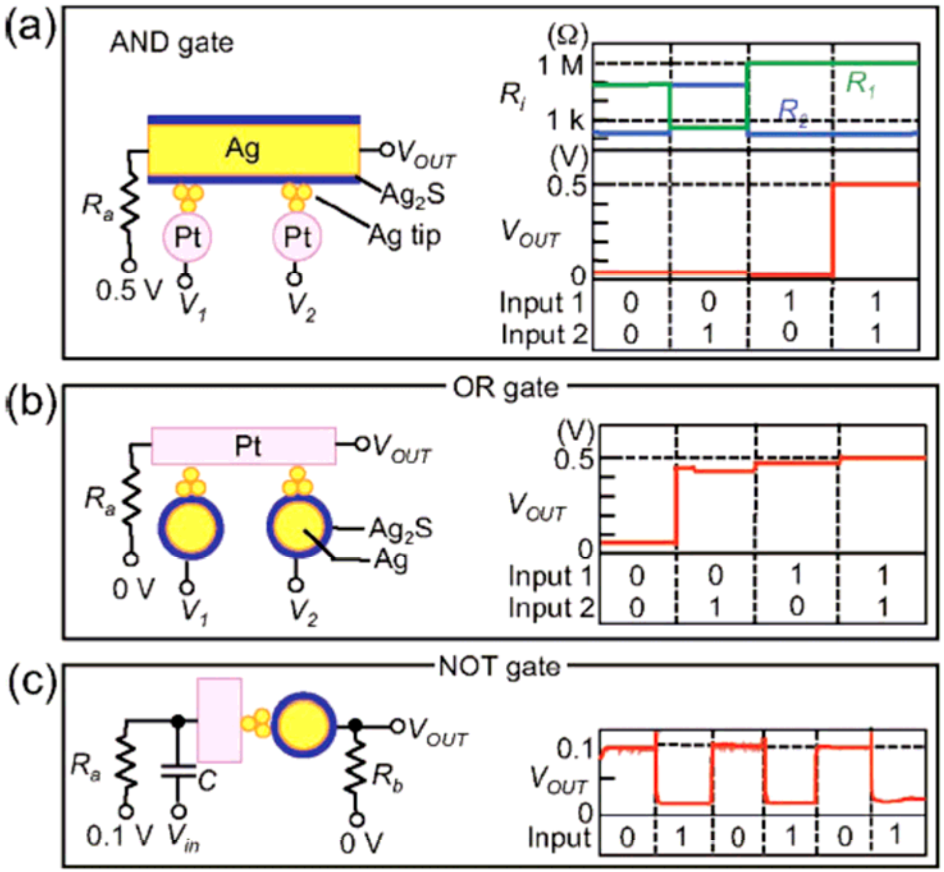


Figure 7. Logic gates configured by gap-type atomic switches in a crossbar circuit. (a) AND gate, (b) OR gate and (c) NOT gate. Reproduced with permission.[15] Copyright 2005, NPG.

examples of logic gates based on the atomic switch

Memristors for logic : circuits

IOP PUBLISHING NANOTECHNOLOGY

Nanotechnology **21** (2010) 235203 (6pp) doi:10.1088/0957-4484/21/23/235203

A memristor-based nonvolatile latch circuit

Warren Robinett, Matthew Pickett, Julien Borghetti, Qiangfei Xia, Gregory S Snider, Gilberto Medeiros-Ribeiro and R Stanley Williams

Hewlett Packard Labs, Palo Alto, CA, USA

A hybrid nanomemristor/transistor logic circuit capable of self-programming

Julien Borghetti, Zhiyong Li, Joseph Straznicky, Xuema Li, Douglas A. A. Ohlberg, Wei Wu, Duncan R. Stewart, and R. Stanley Williams[1]

HP PNAS 2009

Memristors for logic SWOT

Strengths

- low power
- speed
- non-volatility

Weaknesses

- need to improve OFF/ON ratio
- physics ?

Opportunities

- possibility of 3T devices (ex atomic switch)
- new reconfigurable architectures
- logic in memory

Threats

- not endurant enough

Outline

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Von Neumann vs. Neuromorphic computing

- **Human brain**

parallel architecture	**analog**
10^{11} neurons	10 Hz
10^{15} synapses	20 W

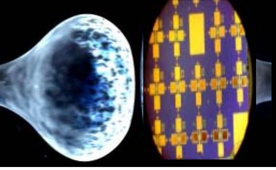
- **Simulations of mouse cortex on Blue Gene L**

Von-Neumann architecture	**digital**
8.10^{4} neurons	1 GHz
5.10^{10} synapses	40 kW

super-computers slower than mouse ($\times$10)

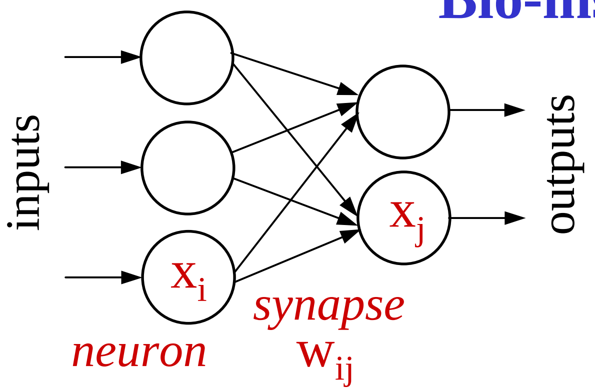
- **Advantages of parallel, analog architecture**

speed, low energy consumption, defect tolerance



Artificial Neural Networks (ANNs)

Bio-inspired computing architectures



- w_{ij} : synaptic weights
  - network memory
  - efficiency to transmit information
  - adjustable = **plasticity** = learning
- huge interconnectivity

parallel, analog architecture : speed, low energy consumption, defect tolerance

Artificial Neural Networks (ANNs)

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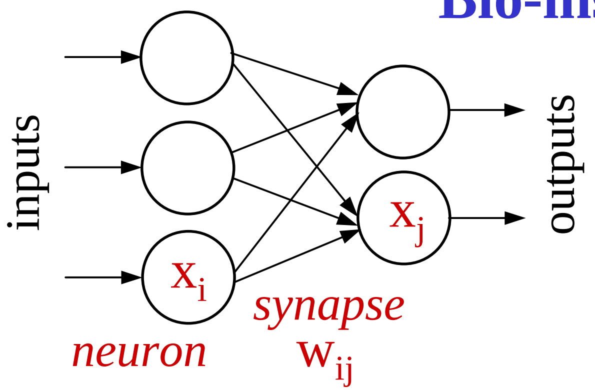

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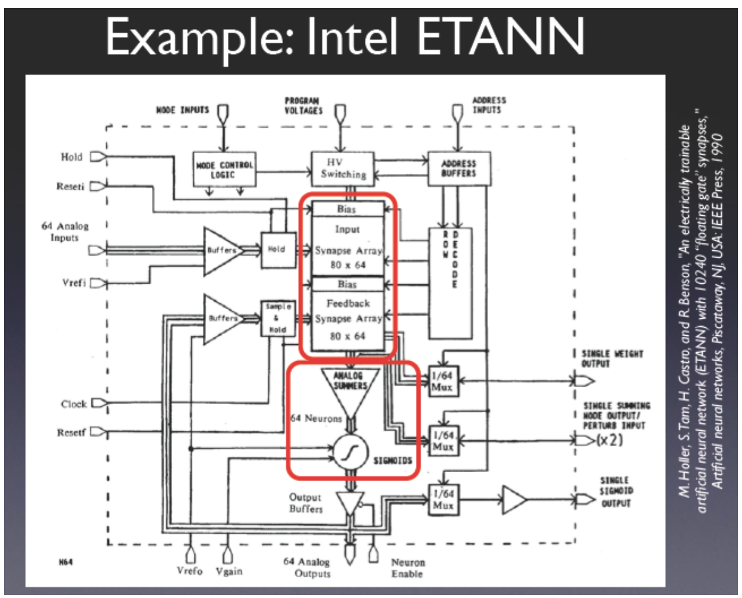
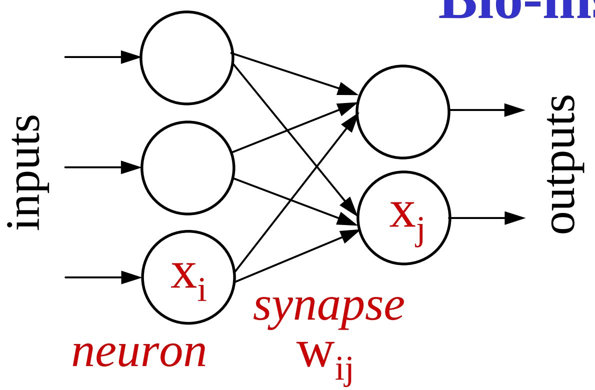


Before 1990
Attempts to build such architectures in hardware

But could not keep up with the boom of GPUs

Artificial Neural Networks (ANNs)

Bio-inspired computing architectures



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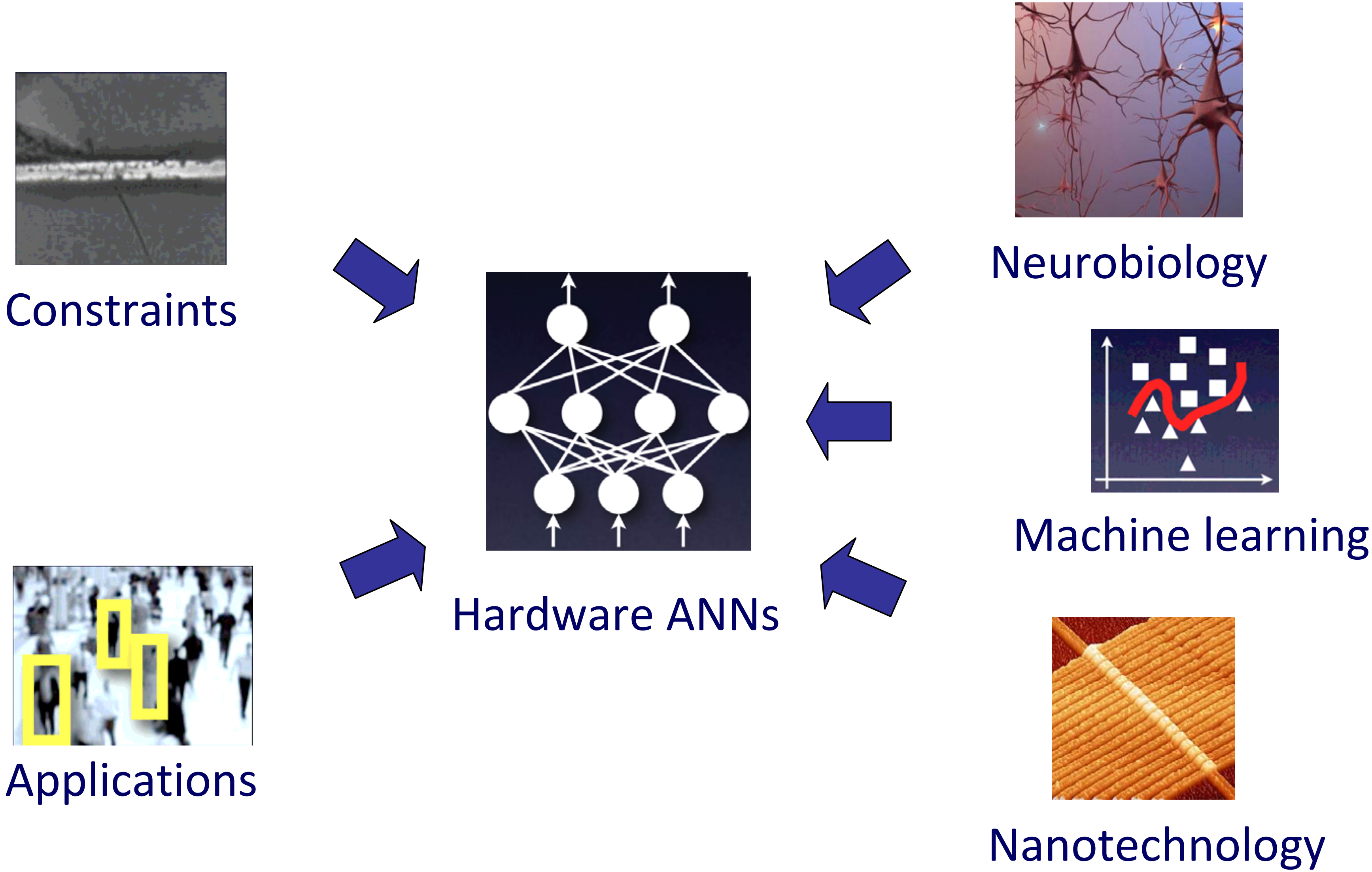
parallel, analog architecture : speed, low energy consumption, defect tolerance

this is no longer true :

the time is ripe to build neuromorphic chips

Convergence of trends



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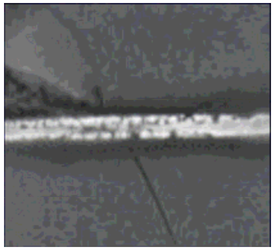
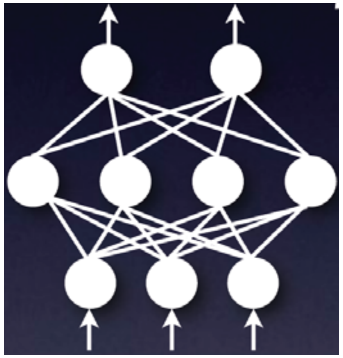
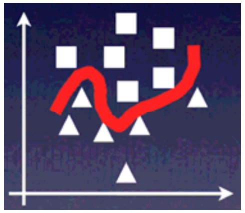


Constraints

Neurobiology

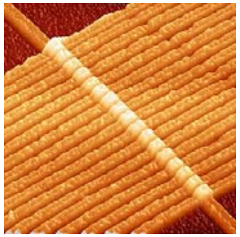


Hardware ANNs



Machine learning

Applications



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Convergence of trends

- power limita- -tions : Multi-cores
- defects
- heterogeneous multi-cores

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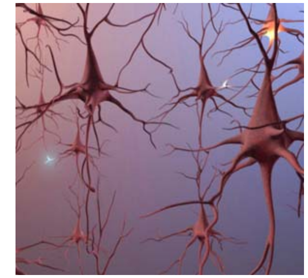

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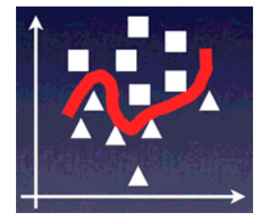

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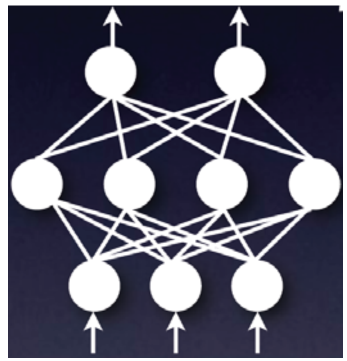

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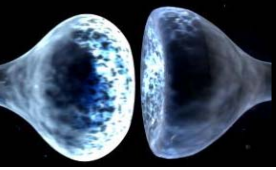

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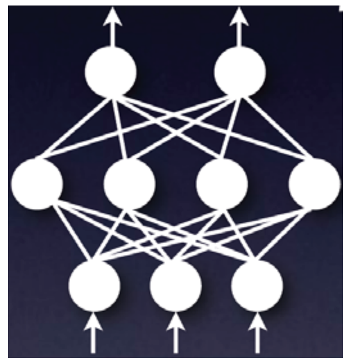

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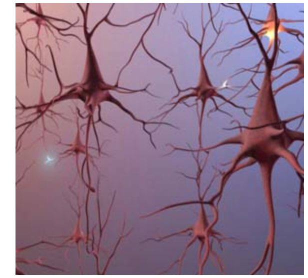

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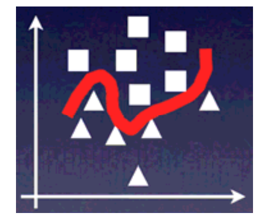

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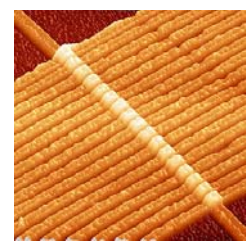

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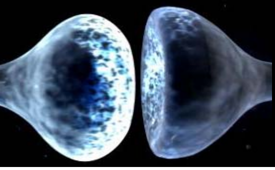

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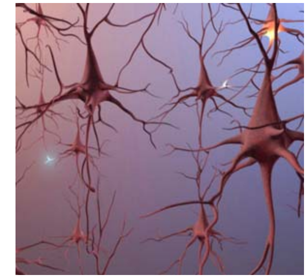

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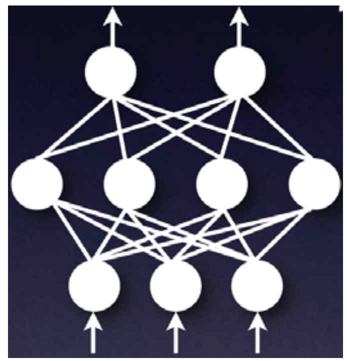

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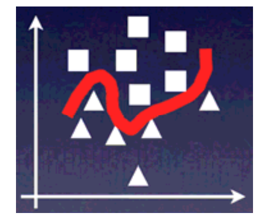
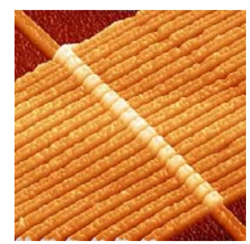


Machine learning

Intel 2005 :
- Recognition
- Mining
- Synthesis

Applications



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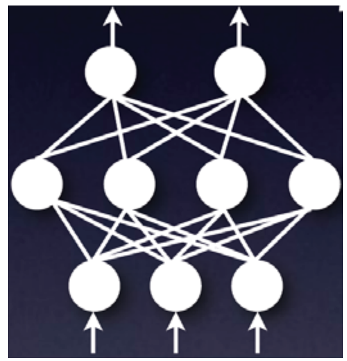

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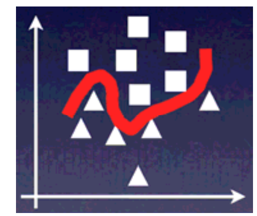

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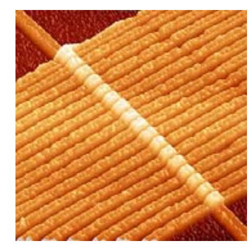

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- brain reverse enginering
- visual cortex ex : T. Poggio

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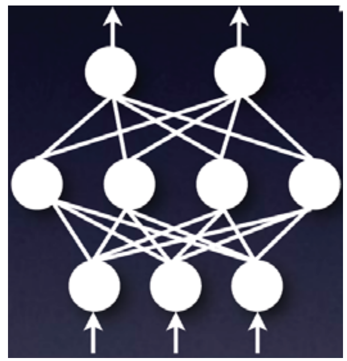

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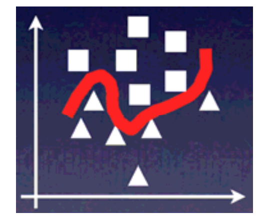

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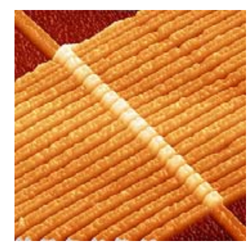

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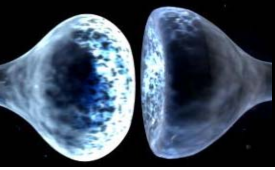

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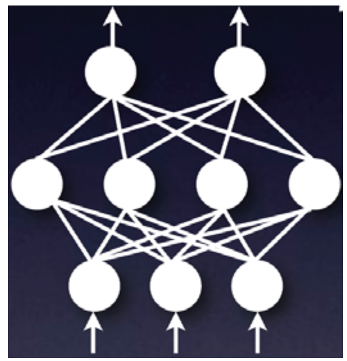

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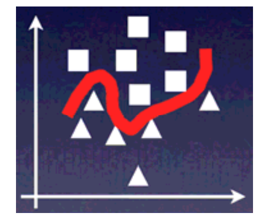

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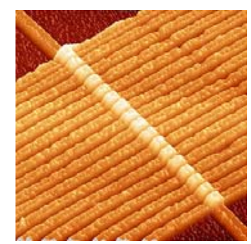

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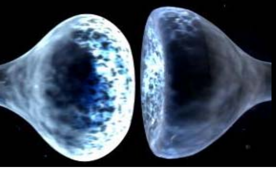

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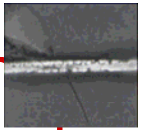

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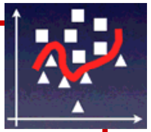

- deep networks
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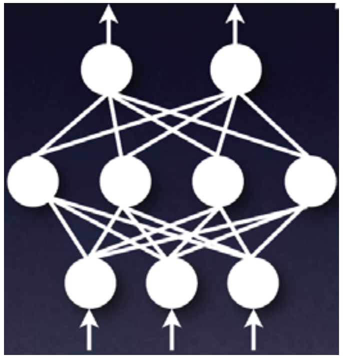
Machine learning



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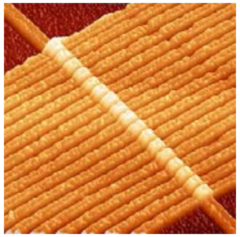

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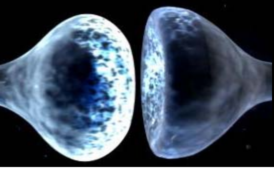

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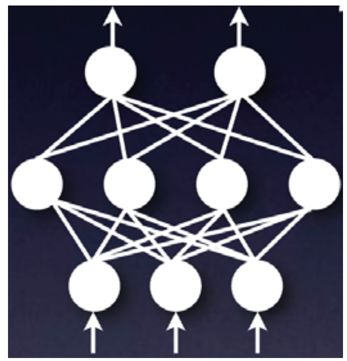

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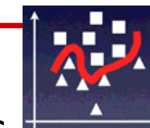

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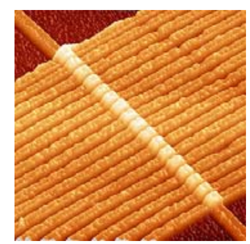

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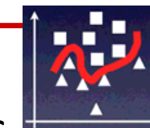
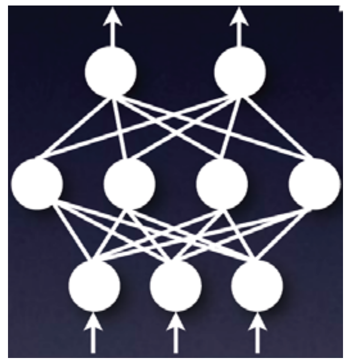
- visual cortex ex : T. Poggio

Neurobiology



- deep networks
- powerfull classifiers

Machine learning



Hardware ANNs

Intel 2005 :

- Recognition
- Mining
- Synthesis

Applications

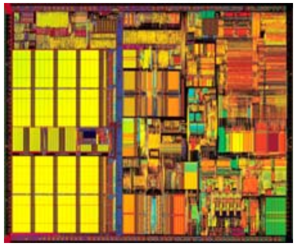
- 1 memristor = 1 synapse
- 3D stacking
- 10^4 synapses/neuron

Nanotechnology

O. Temam, The rebirth of Neural Networks, Proc. ISCA'2010

Hardware ANNs : applications

Hardware ANNs : good at certain tasks
Classical architectures : good at other tasks

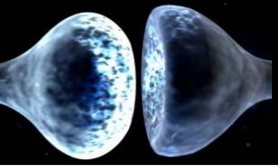


- **Hybrid architectures Von Neumann / ANN**

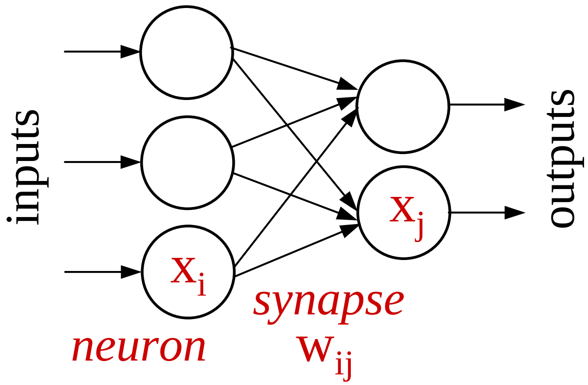
heterogenous multi-core, embedded applications
Goal : accelerating specific tasks
example : digital camera, accelerate smile recognition
voice recognition…

- **Large scale hardware simulations of the human brain ?**

faster and less power consumption than supercomputer simulations
Goal : understanding the human brain
cf : european projects FACETS/Brainscales
& Human Brain flagship project



Criteria for artificial synapses



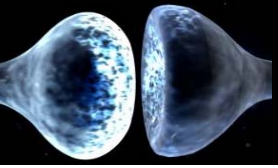
- **synapses should have a memory : the weights have to be stored**
  (non-volatility)

- **synapses should be small : 10^4 synapses/neuron in human brain**

- **synapses should be plastic : synaptic plasticity**

Biological synapse : change in strength in response to either use or disuse of transmission
Artificial synapses : the weigths w_{ij} should be adjustable

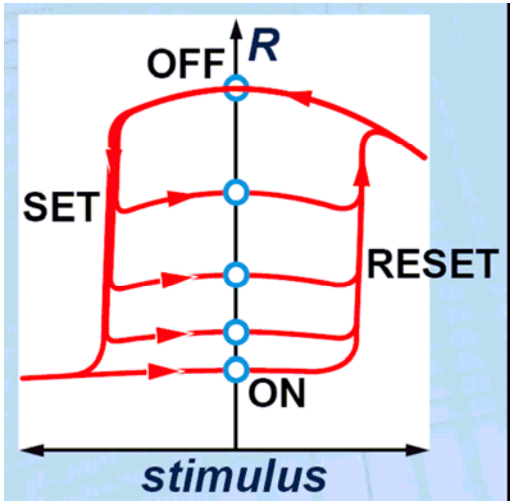
a learning rule specifies how to adjust the weights for a given input/output pair



Memristors : artificial synapses

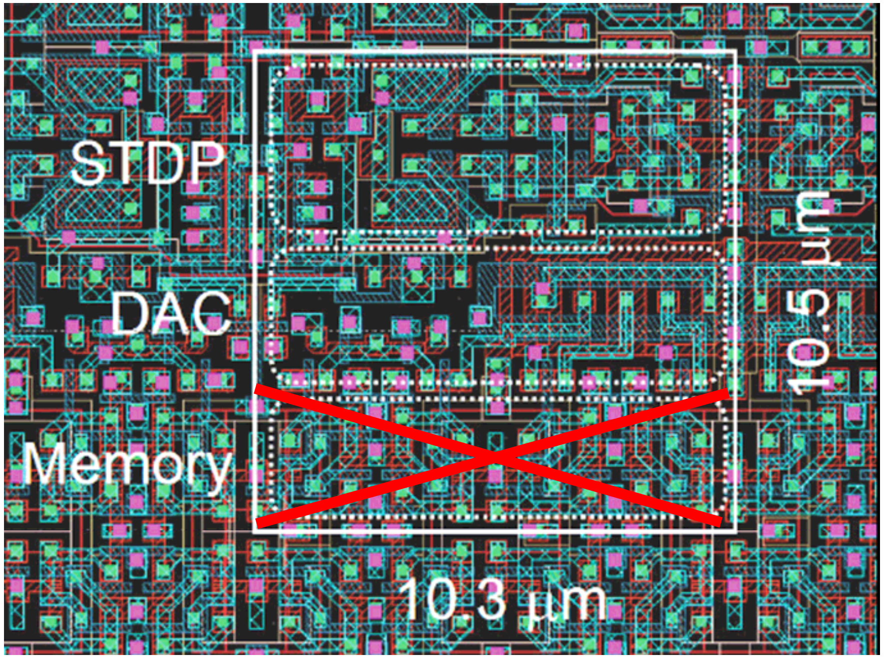
- **Memristors have a memory :**
  they directly store the synaptic weights *(w = conductance)*

Non-volative multi-valued resistances

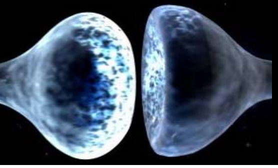


no need for space consuming SRAM banks to store the weights

CMOS artificial synapse made at Kirchhoff Institute



Schemmel *et al.*, IJCNN 2006

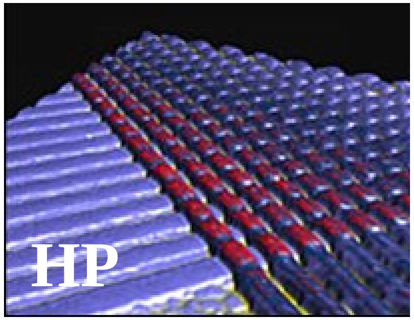


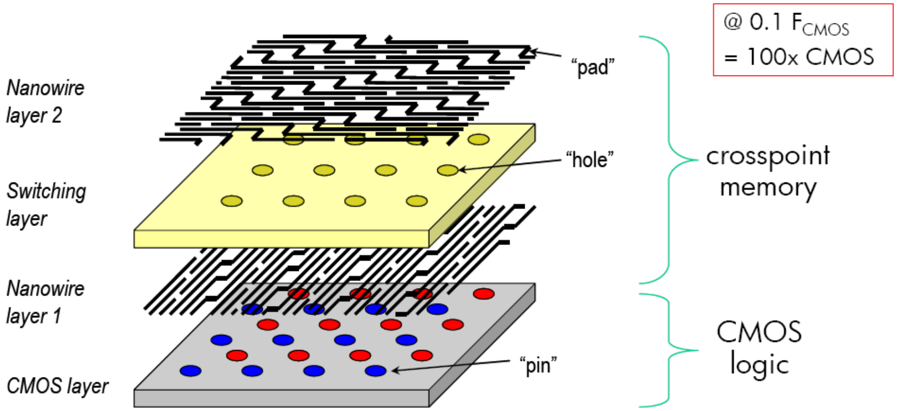
Memristors : artificial synapses

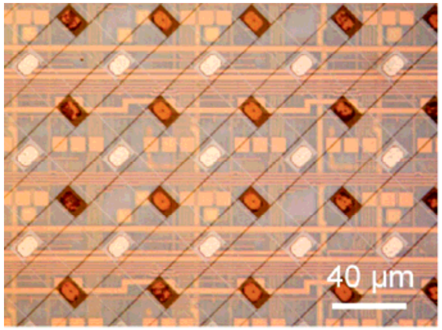
- **Memristors are small *(< 50 x 50 nm^2)***

interconnection issue : about 10^4 synapses per neuron in the brain

ex : CMOS "neurons" + **memristive "synapses"**





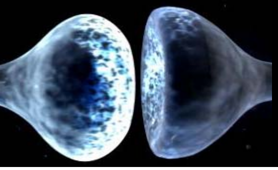


Xia *et al.*, Nanoletters (2010)

memristor crossbar arrays

No demonstration yet of operational mixed memristor/CMOS cognitive chip

to be solved : cross-talk, sneak paths, lithography



Memristors : crossbar arrays

NANO LETTERS **2011** LETTER

pubs.acs.org/NanoLett

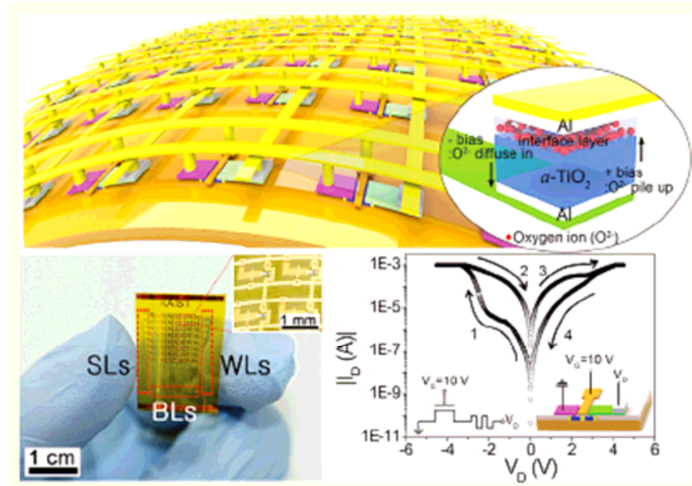
Flexible Memristive Memory Array on Plastic Substrates

Seungjun Kim,[†] Hu Young Jeong,[†,§] Sung Kyu Kim,[†] Sung-Yool Choi,[‡,⊥] and Keon Jae Lee[*,†]

[†]Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 305-701, Republic of Korea

[‡]Electronics and Telecommunications Research Institute (ETRI), Daejeon 305-700, Republic of Korea

TiO_2 8 x 8



NANO LETTERS **2012** Letter

pubs.acs.org/NanoLett

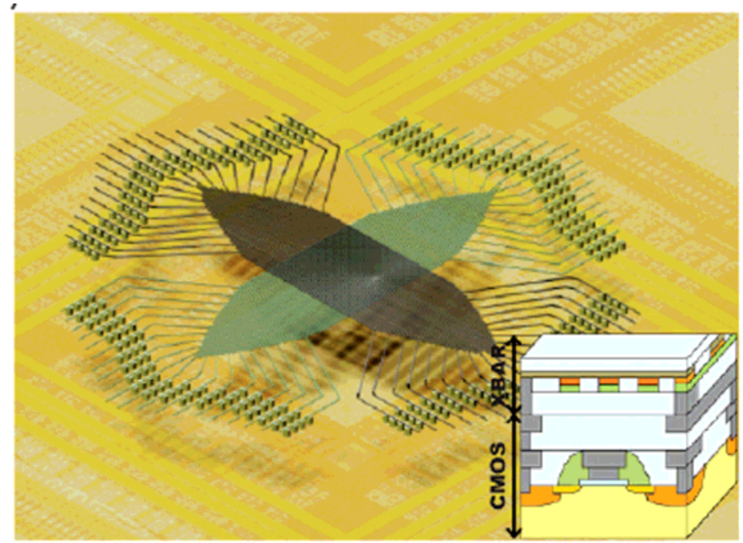
A Functional Hybrid Memristor Crossbar-Array/CMOS System for Data Storage and Neuromorphic Applications

Kuk-Hwan Kim,[†] Siddharth Gaba,[†] Dana Wheeler,[‡] Jose M. Cruz-Albrecht,[‡] Tahir Hussain,[‡] Narayan Srinivasa,[‡] and Wei Lu[*,†]

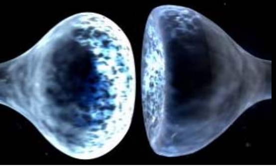
[†]Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, Michigan 48109, United States

[‡]HRL Laboratories LLC, 3011 Malibu Canyon Road, Malibu, California 90265-4797, United States

Si/Ag 40 x 40



Small demonstrators exist



Memristors : artificial synapses

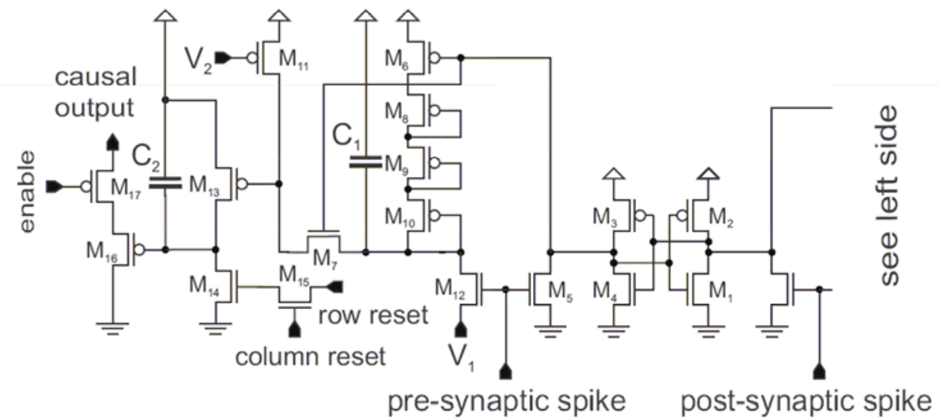
- **Memristors directly implement the synaptic plasticity** **$v = M(q)\,i$**

$M(q)$ is continuously tunable between R_{ON} and R_{OFF}

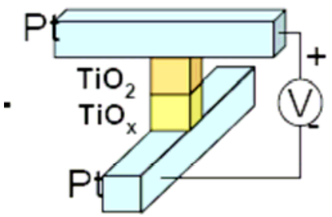
No need for space consuming complicated CMOS circuits

CMOS synapse emulating a learning rule called :
Spike Timing Dependent Plasticity (STDP)

1 memristor directly implements STDP



< 30x30 nm^2

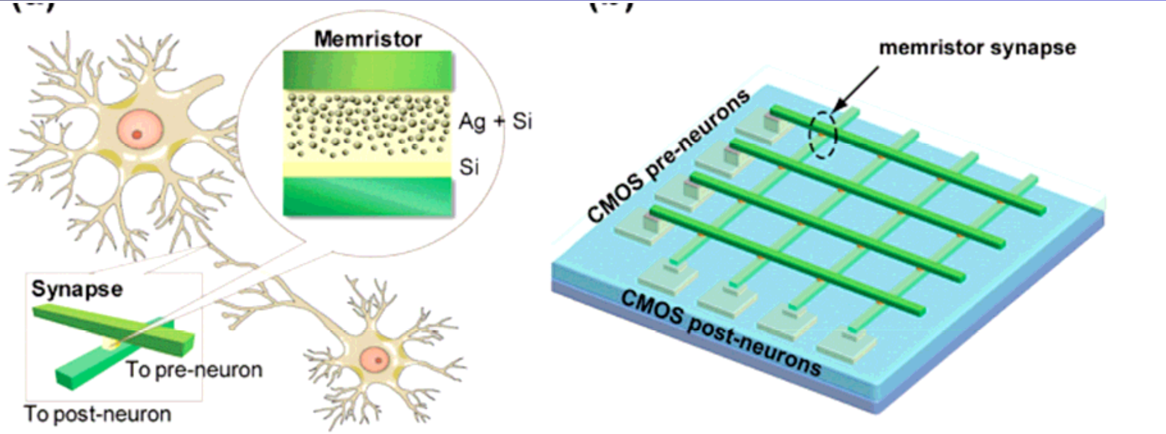


- Jo *et al.*, Nanoletters 2010
- Linarres-Barranco *et al.*, Frontiers in Neuroscience, 2011

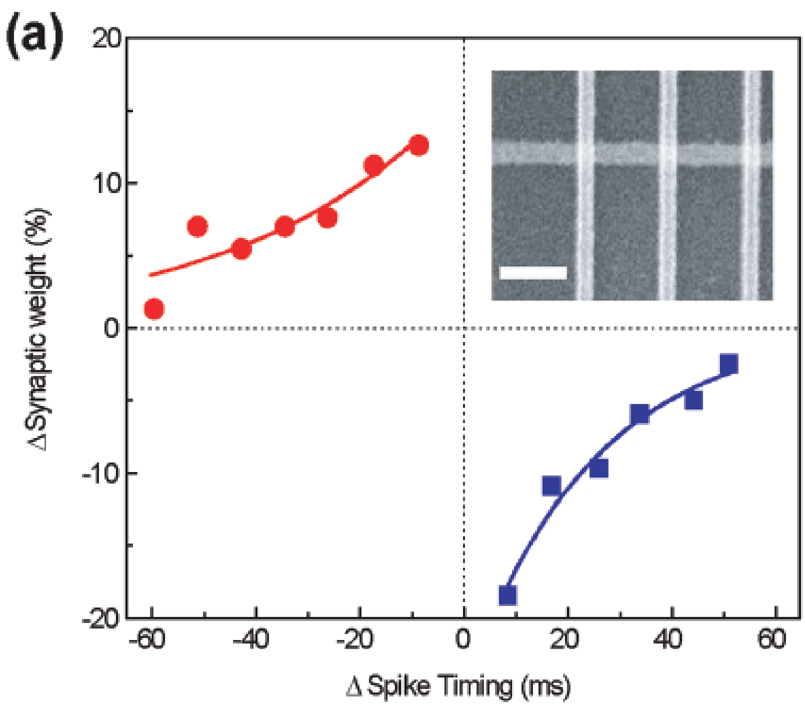
Schemmel *et al.*, IJCNN 2006

STDP : experimental implementation

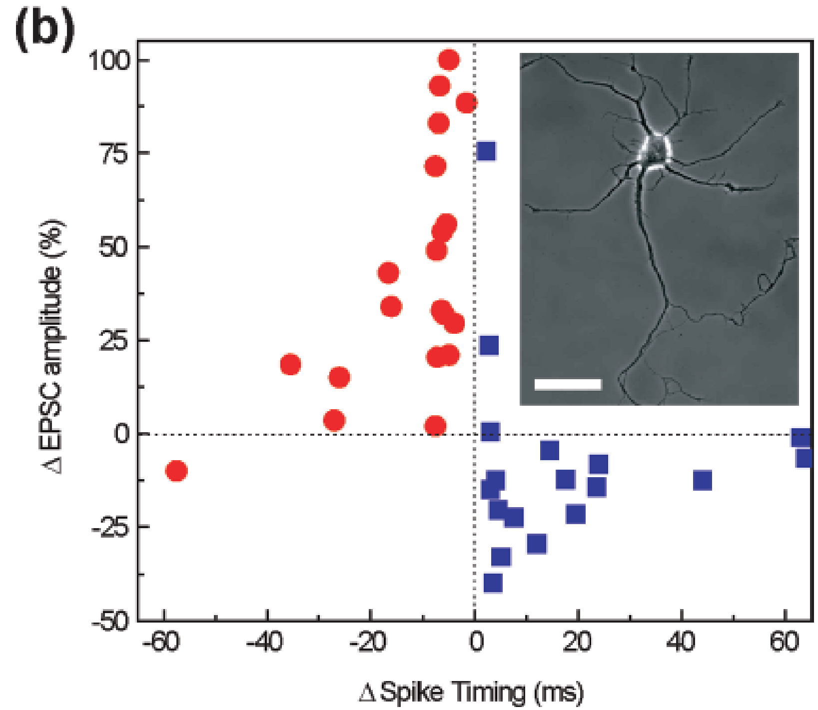
Jo *et al.*, Nanoletters 2010



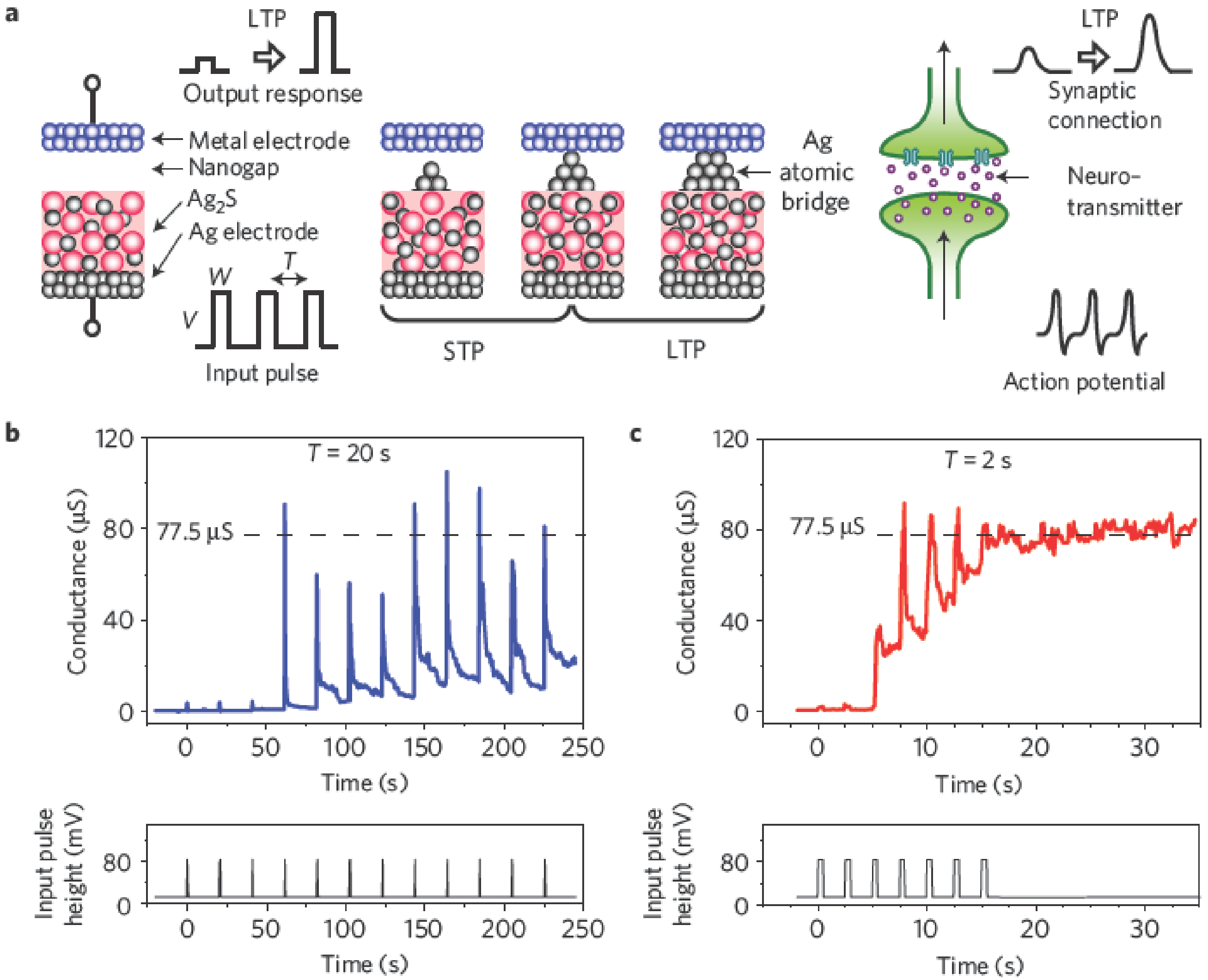
Memristor STDP curve



Bi & Poo 1998

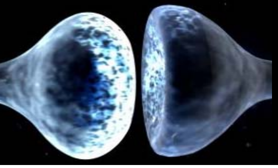


Atomic switch



Ohno, Aono *et al.*, Nature Mat. 2011

Short term versus long term memory



neuromorphic architectures

- inspiration from biology and cell signalling process

- different levels of abstraction

  → at the cell level (neuron)

  → at the molecular level (biochemival reaction)

- common points

  → massively parallel

  → take advantage of the noise (stochasticity)

- common challenges

  → interconnect

  → programming

  → communication with classical computing architectures

Neuromorphic Computing SWOT

Strengths
- speed
- low power
- defect tolerance

Weaknesses
- interconnect
- programming
- design : to be invented
- control device stochasticity

Opportunities
- use differently memory devices
- accelerators for specific functions to interface in heterogeneous multi-core architectures
- adaptive architectures, able to compute with incomplete data → robotics, unmanned vehicles etc.

Threats
- the density cannot be reached
- the interconnection problem cannot be solved
- heat management

MemCo Workhop

"Memristors for Computing"

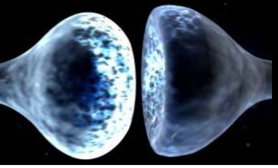
19-21 November 2012, Fréjus, France

INVITED SPEAKERS

- M. Di Ventra (UC San Diego, USA)
- Y. Frégnac (UNIC, Gif s.Yvette, FRA)
- V. Garcia (CNRS/Thales, Palaiseau, FRA)
- T. Hasegawa (Nims MANA, Tsukuba, JAP)
- B. Jackson (IBM Almaden, USA)
- D. Kuzum (Stanford Univ., USA)
- B. Linares-Barranco (IMSE Sevilla, SPA)
- W. Lu (Univ. of Michigan, USA)
- T. Prodromakis (Imperial College London, UK)
- D. Querlioz (IEF Orsay, FRA)
- D. Strukov (UCSB, USA)
- S. Thorpe (CerCo, Toulouse, FRA)
- S. Williams (Hewlett Packard, Palo Alto, USA)
- D. Wright (Exeter University, UK)

Inscriptions and abstract submission deadline : July, 31st 2012

http://www.trt.thalesgroup.com/ump-cnrs-thales/memco



General conclusion

- Many opportunities for memristors
- Same device / different ways to compute with it

→ **exploit multi-functionality**

Digital memories — **Logic circuits** — **Neuromorphic computing**

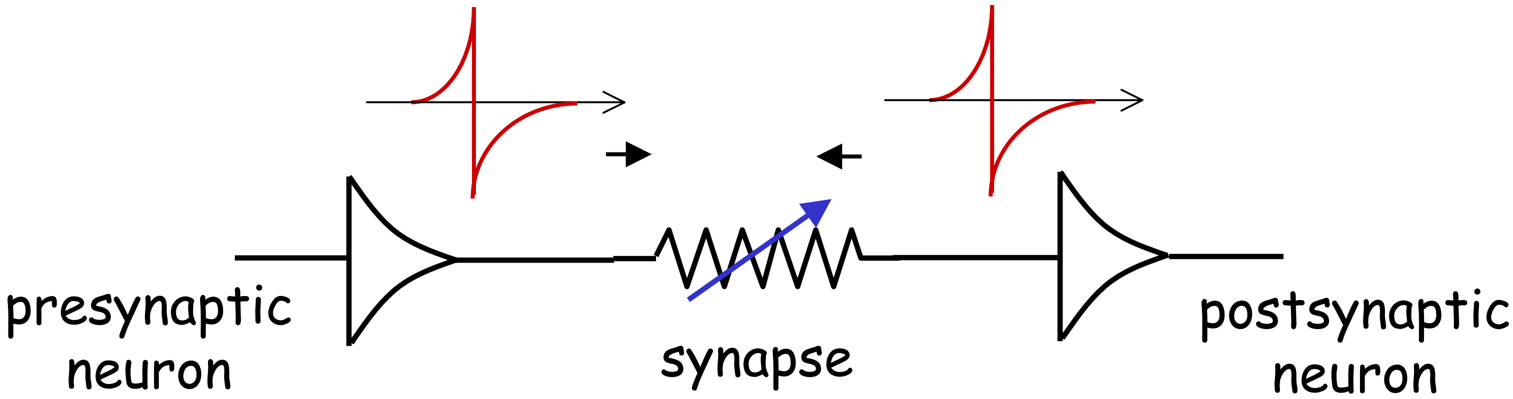
2012 — 2016 — 2020 — 2030 ? → t

Hebbian learning

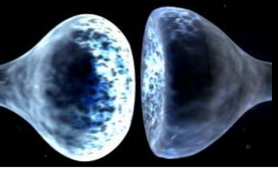
• **Learning rule :**

« Neurons that fire together wire together » Hebb, 1949

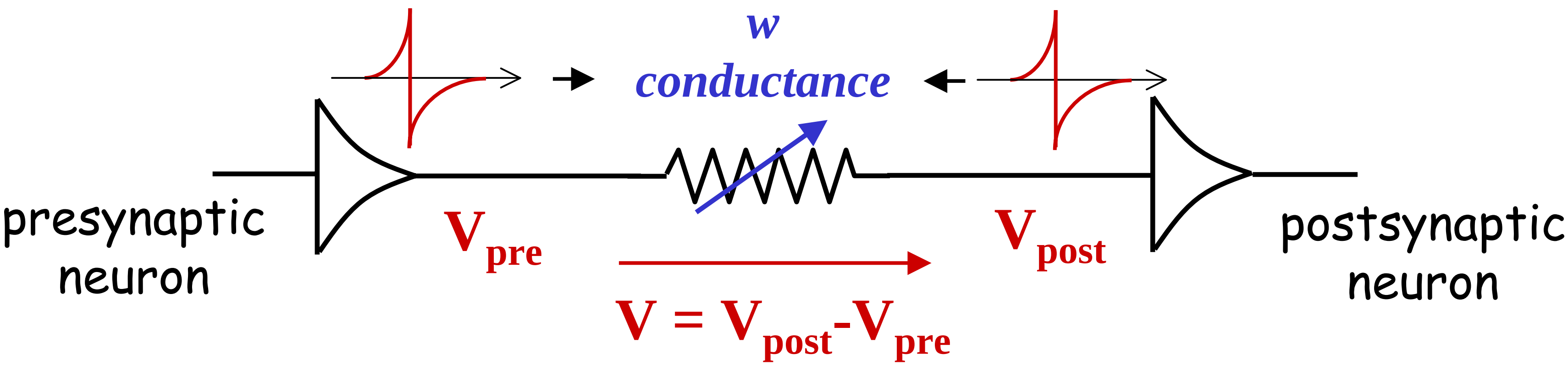
• **Spike timing dependent plasticity :**



- causality is important:
transmission enhanced if post-neuron fires after pre-neuron
- timing is important :
–ΔT small, large transmission changes



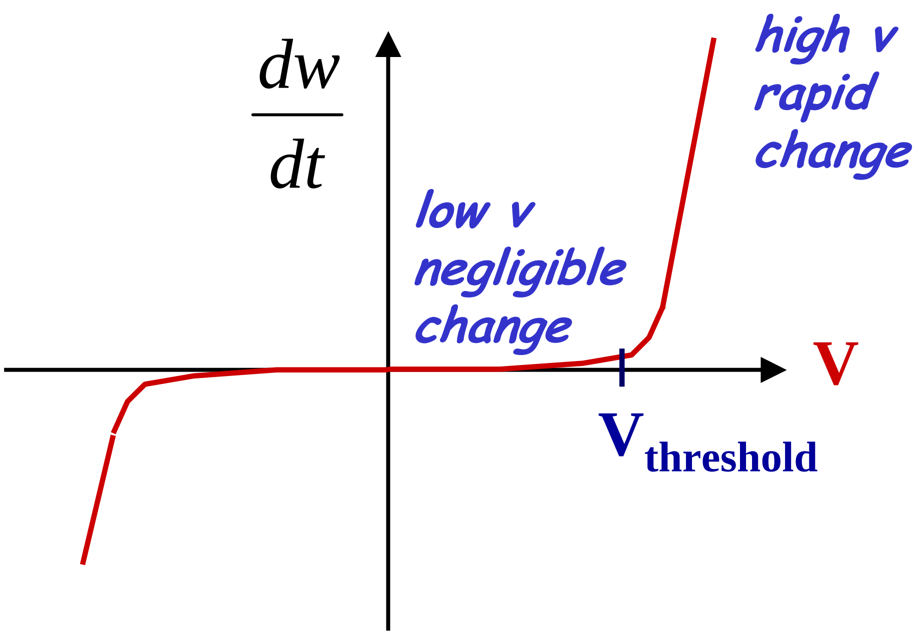
Spike timing dependent plasticity



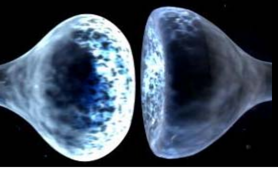
- **change of conductance vs. applied voltage :**

general shape for memristors

enables learning



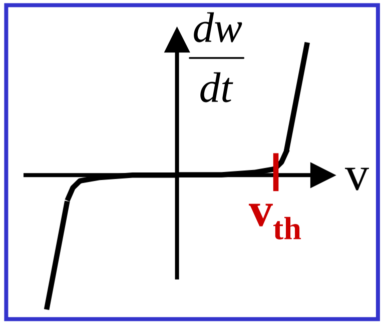
Snider *et al.*, Nanotechnology 2007

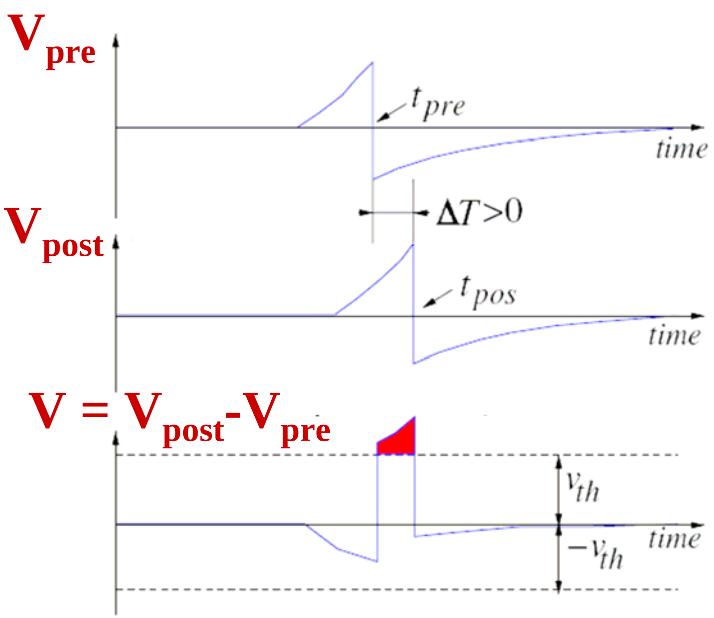


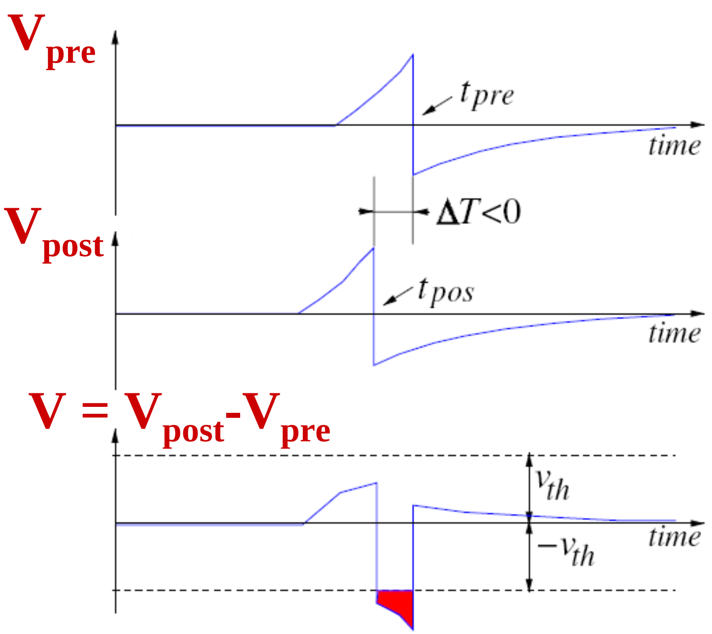
Spike timing dependent plasticity

Memristor change of conductance (synapse weight)

Linarres-Barranco *et al.*, frontiers in Neuroscience, 2011





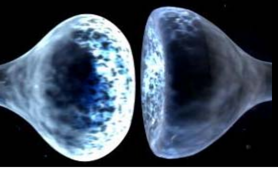


conductance increase

potentiation

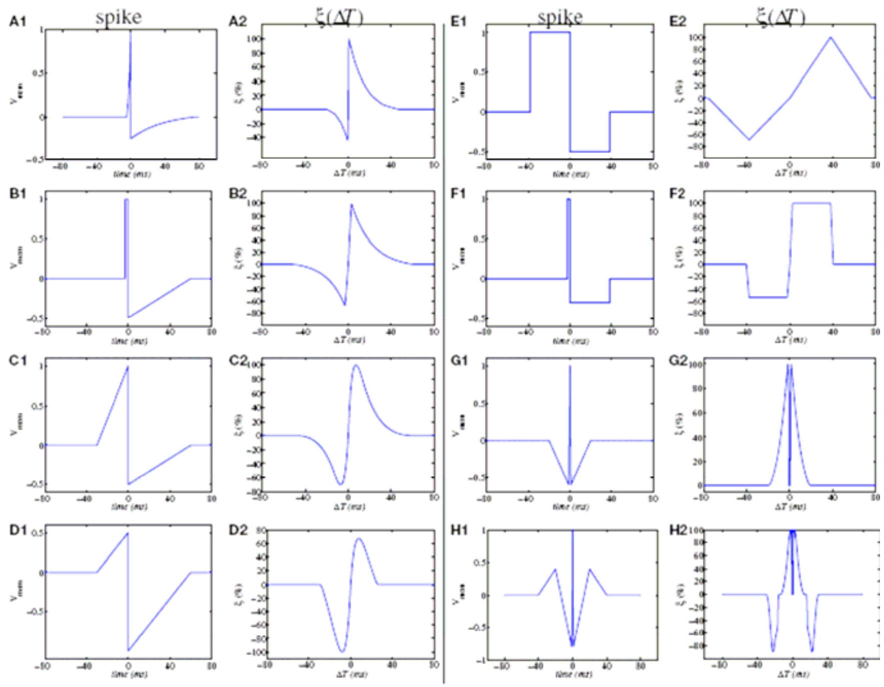
conductance decrease

depression



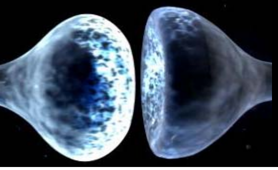
STDP curve vs action potential shape

Linarres-Barranco *et al.*, frontiers in Neuroscience, 2011



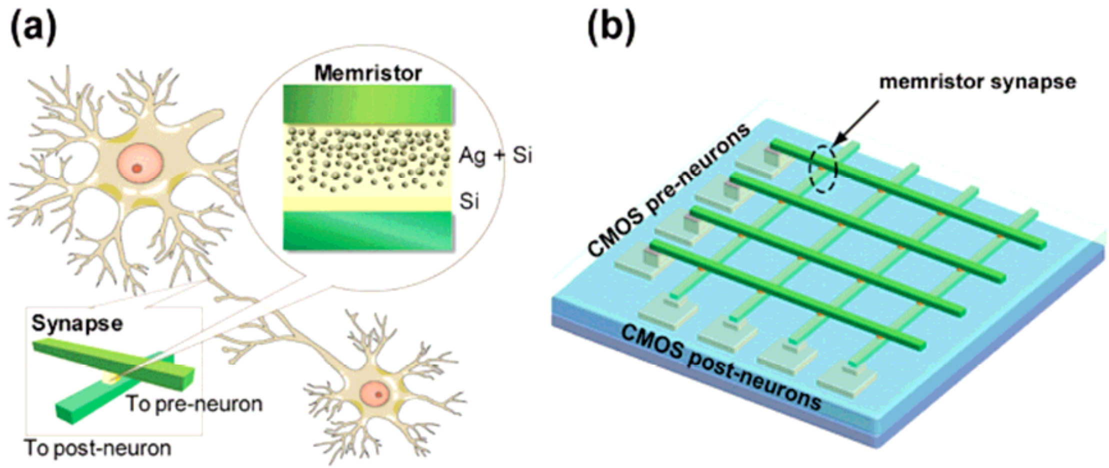
possibility to implement different kinds of STDP with a single device

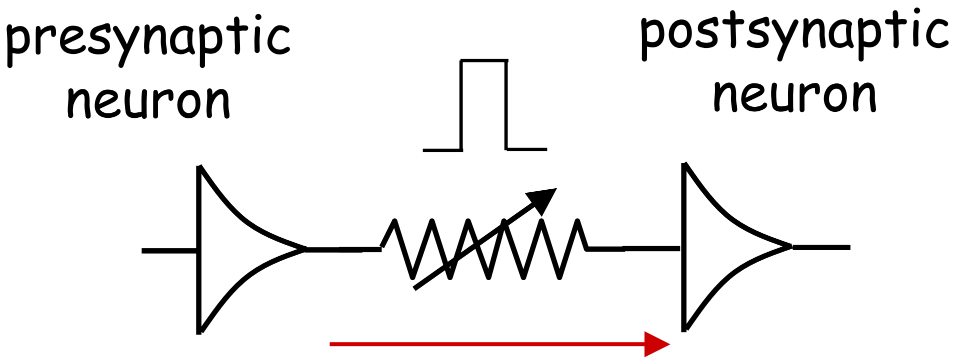
STDP allows unsupervised learning (image recognition etc.)



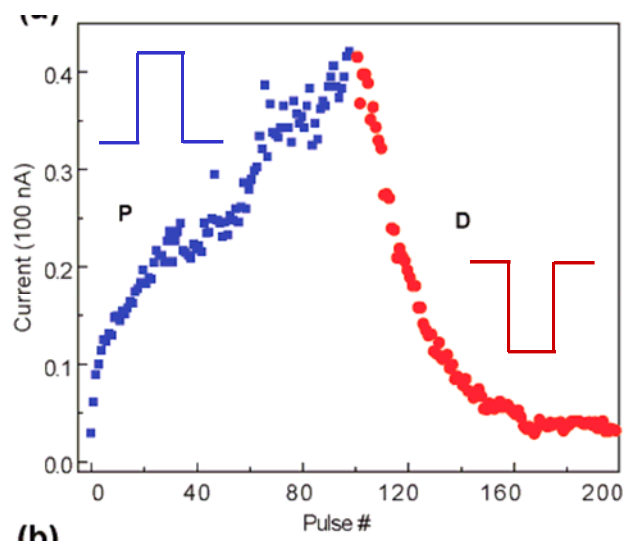
STDP : experimental implementation

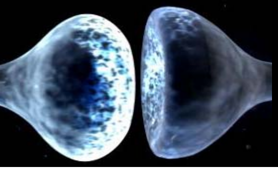
Jo *et al.*, Nanoletters 2010





$V = V_{post} - V_{pre}$





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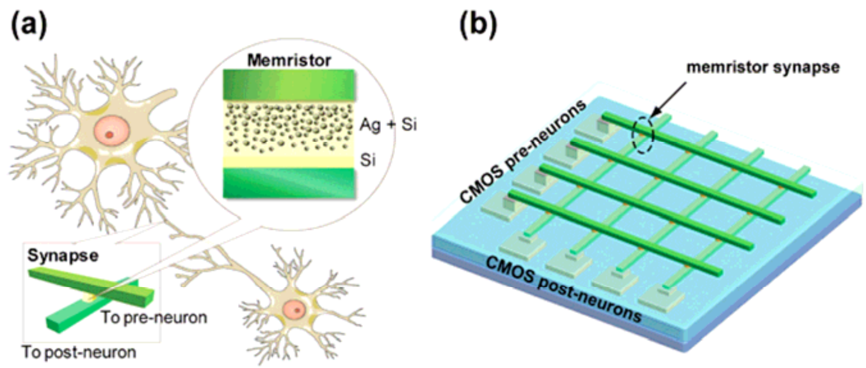
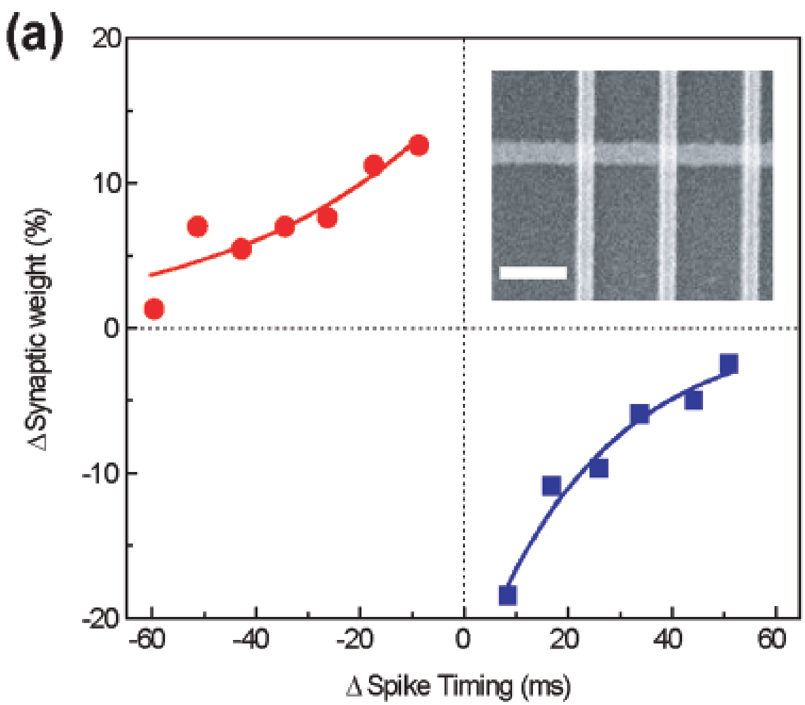
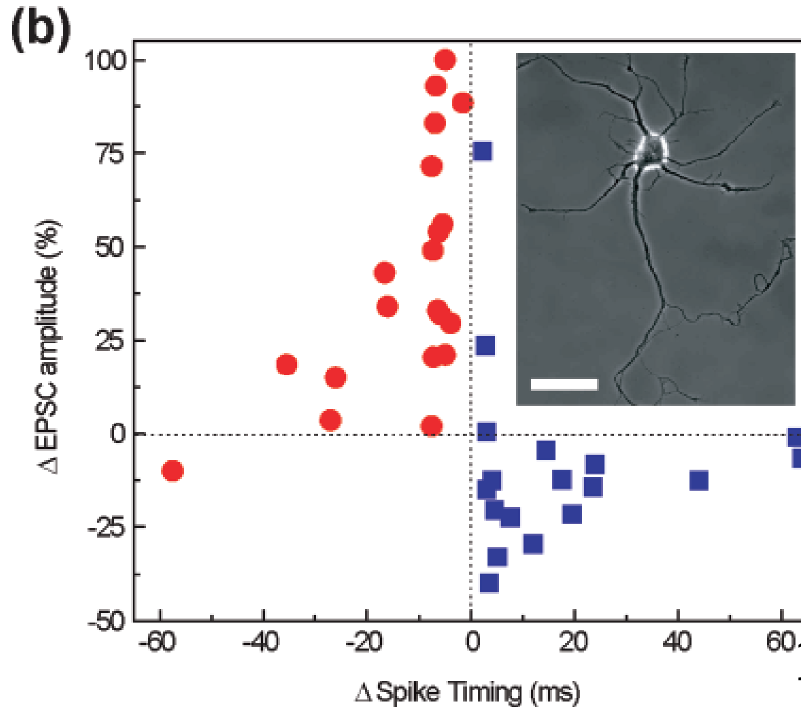
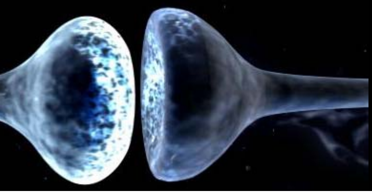


Memristor STDP curve



Bi & Poo 1998





Memristors around the world

- **US** : 2009 DARPA "SyNAPSE" program

Systems of Neuromorphic Adaptive Plastic Scalable Electronics

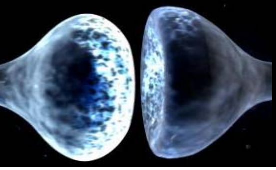
define a new path forward for creating
useful, intelligent machines

3 funded projects (*~ 5 M$ each for the first phase*)

- Hewlett-Packard (*memristors*) - HRL labs (*memristors*) - IBM (*?*)

- **Europe** :

FP7 Nabab, FP7 Bion (ended)
ERC NanoBrain & ERC Femmes projects, Chist-Era PNEUMA



Conclusion & perspectives

• State of the art memristor : exciting potential of memristor devices as artificial synapse

• spintronic memristor : resistance switching based on purely electronic effects

⇨ very promising : endurance, speed, power consumption

• Young topic : no demonstration yet of a cognitive chip based on memristors

• Dedicated architectures and programmation schemes to be developed

• Which type of memristor for which application ?

Acknowledgements

Funding :

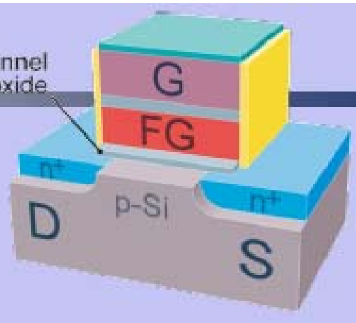
- **ERC Starting Grant 259068 Nanobrain**

- **ANR P2N MHANN « Memristive Hardware Artificial neural Networks Accelerators »**

- **PEPS project ACME « Memristive Accelerators »**

	Volatile		Non-volatile				
	DRAM	SRAM	NAND Flash	Trapping charge	FERAM	MRAM	PCM
Storage mechanism	Charge on capacitor	Interlocked state of logic gates	Charge on floating gate	Charge trapped in gate insulator	Ferroelectric polarization	Magnetization	Amorphous /cristalline phases
Cell elements	1T1C	6T	1T	1T	1T1C	1(2)T1C	1T1R
Feature size (nm)	50	65	90	50	180	130	65
Cell area	$6F^2$	$140F^2$	$5F^2$	$6F^2$	$22F^2$	$45F^2$	$16F^2$
W/E time	<10 ns	0.3 ns	0.1 ms	20 µs	10 ns	20 ns	50 ns
Retention time	64 ms	0	> 10 y	> 10 y	> 10 y	>10 y	>10 y
Write cycles	>1E16	>1E16	>1E5	>1E5	1.00E+14	>1E16	1.00E+09
Write voltage	2.5	2.5	15	8	0.9-3.3	1.5	3
Read voltage	1.8	1	2	1.6	0.9-3.3	1.5	3
Write energy	5 fJ	0.7 fJ	10 fJ	100 fJ	30 fJ	100 pJ	6 pJ

Requirements



... to compete with Flash

Endurance:	**> 10^7 cylces** (Flash 10^3 ... 10^7)
Resistance ratio:	**R_{OFF} / R_{ON} > 10**
Scalability:	**F < 22 nm and/or 3-D stacking**
Write voltage:	**approx. 1 ... 5 V** (Flash > 5 V)
Read voltage:	**0.1 ... 0.5 V**
Write speed:	**< 100 ns** (Flash > 10 μs)
Retention:	**> 10 yrs**

R. Waser, ISIF 2011