Universidad de Granada
Departamento de Electrónica y Tecnología de Computadores

Nanoelectronics Research Group

Francisco Gamiz

CITIC-UGR

Universidad de Granada

Welcome to Granada !!

Welcome to NANOTEC!!

Who we are

Prof. Francisco Gámiz
Professor

Dr. Juan B. Roldan
***Associate** professor*

Dr. Andres Godoy
Associate professor

Dr. Francisco Jimenez
Associate professor

Dr. Pedro Cartujo
Associate professor

Dr. Carlos Sampedro
Assistant professor

Dr. Noel Rodriguez
Assistant professor

Dr. Francisco Garcia
Assistant professor

Dr. Isabel Tienda
Assistant professor

Dr. Luca Donetti
Researcher

Dr. Blanca Biel
Researcher

Mr. Andres Roldan
Lecturer

Mr. Francisco Carricondo
PhD Student

Mr. José L. Padilla
PhD Student

Ms. Maria Balaguer
PhD Student

Mr. Celso Martínez
PhD Student

Who we are

- The “numbers” of the group (during the last five years):

  - More than 2.5 M€ in European, National and Regional projects.

    FP6: SINANO and EUROSOI (0.5M€)
    FP7: NANOSIL and EUROSOI+ (0.5M€)
    Spanish Goverment: 5 projects (1.5M€)
    Regional Goverment: 3 projects (0.3M€)

  - Coordination of EUROSOI and EUROSOI+ European projects.

  - More than 60 publications in journals and international conferences (ESSDERC, IEDM, IWCE, ULIS ..) in the last 5 years.

  - More than 500 citations

  - 2 international patents

  - 3 PhD Thesis

What we do

The main topics of the group are:

1. SIMULATION

- ✓ Electrostatics 1-D y 2-D
- ✓ Poisson + Schrödinger (quantum simulation)
- ✓ Psi-MOS
- ✓ Ergodic transport and Ensemble MonteCarlo, multisubband, k·p ...

2. MODELING

- ✓ Short channel effects
- ✓ Corner Effects
- ✓ Quantum corrections
- ✓ Special devices

3. CHARACTERIZATION

- ✓ I/V, C/V,
- ✓ Pulsed,
- ✓ Transient,
- ✓ Low and High Temperature,
- ✓ Magnetotransport,...

Simulation and modeling

Before we begin...

1. Why do we simulate?

- To **explain** the characteristics of manufactured devices.
- To **predict** the behavior of which will be fabricated in the next (or not so next…) future.

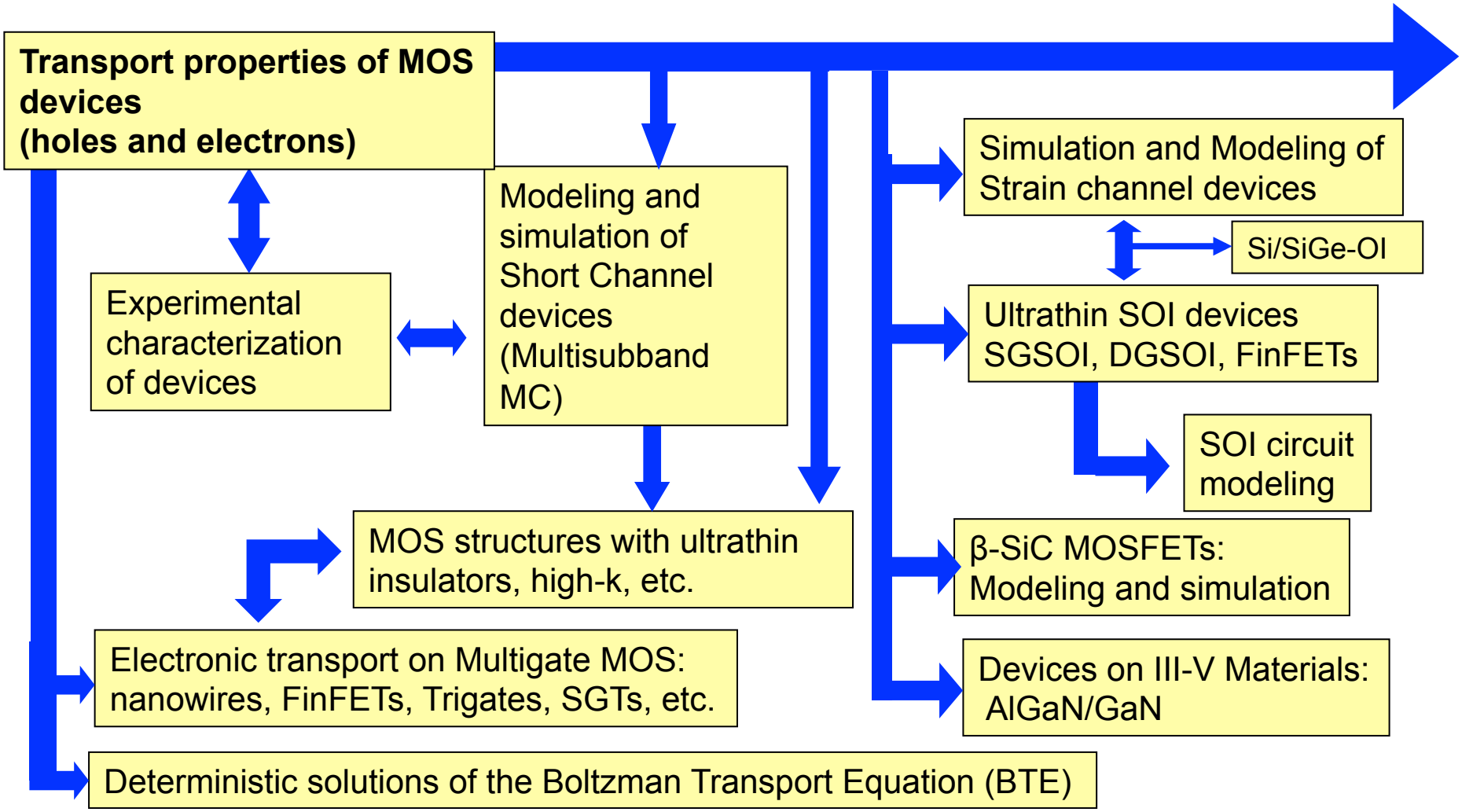
2. Why modeling?

- To help **designing** complex circuits: from logic functions to processors.

Simulation and modeling

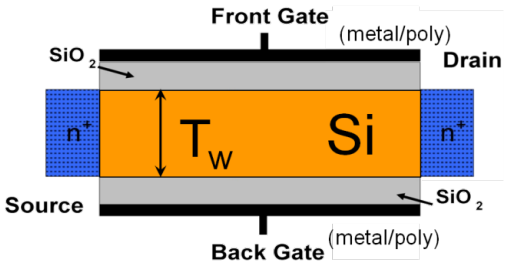
We try to simulate the behavior of several different devices

… **it is a complex task!!**

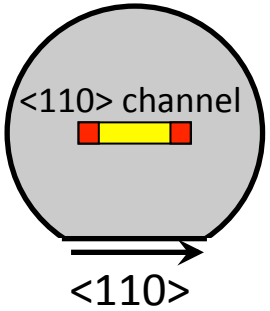


NRG group overview

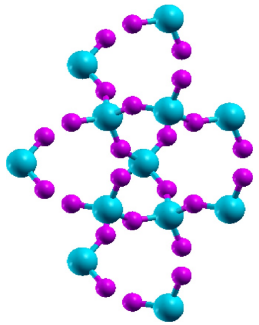
Some of the devices and techniques we study



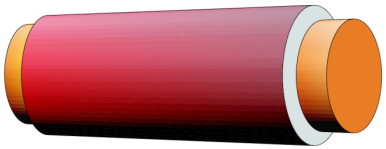
Double-Gate NMOSFETs



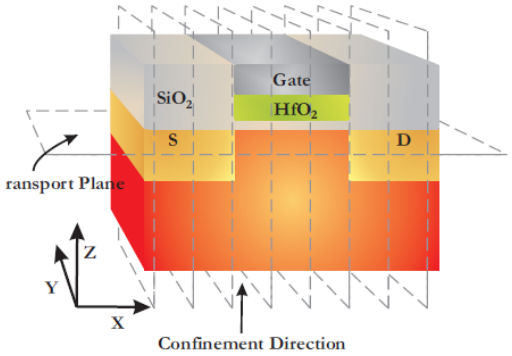
Channel orientation



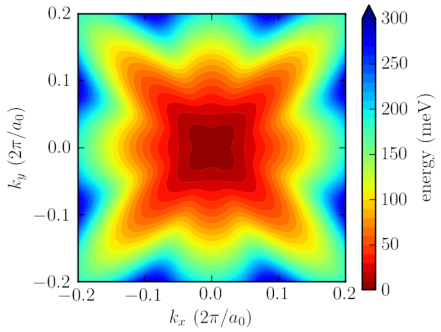
Atomistic scale simulations



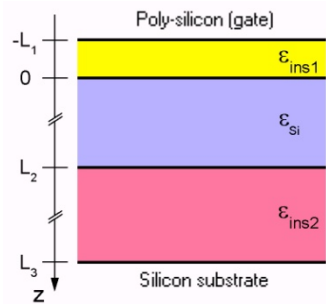
Multigate devices



Multi-Subband EMC

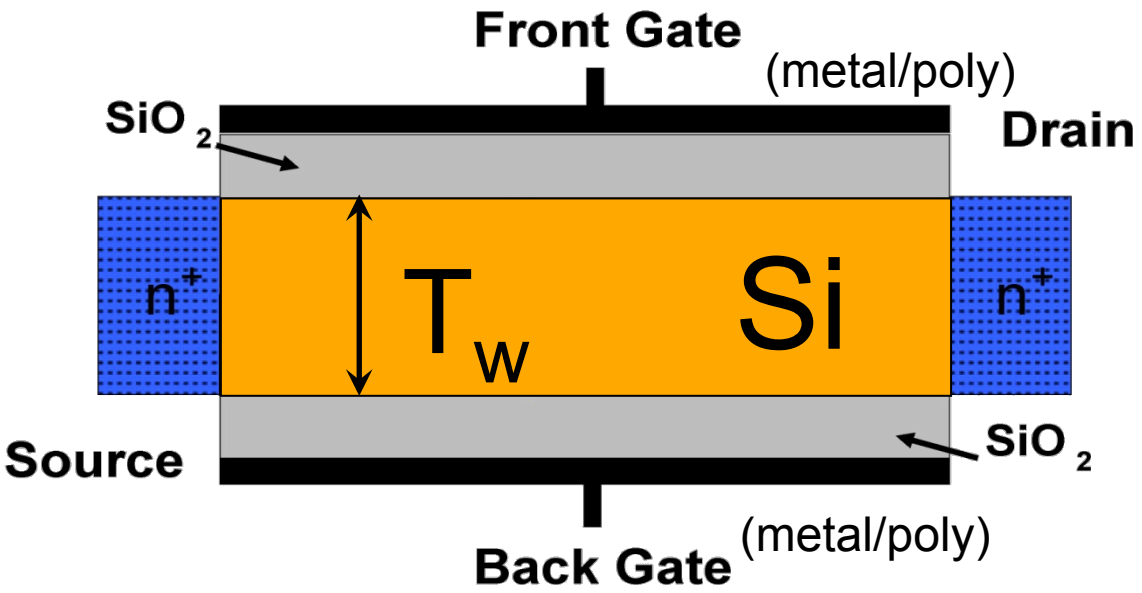


Hole Simulations



Devices with High-k

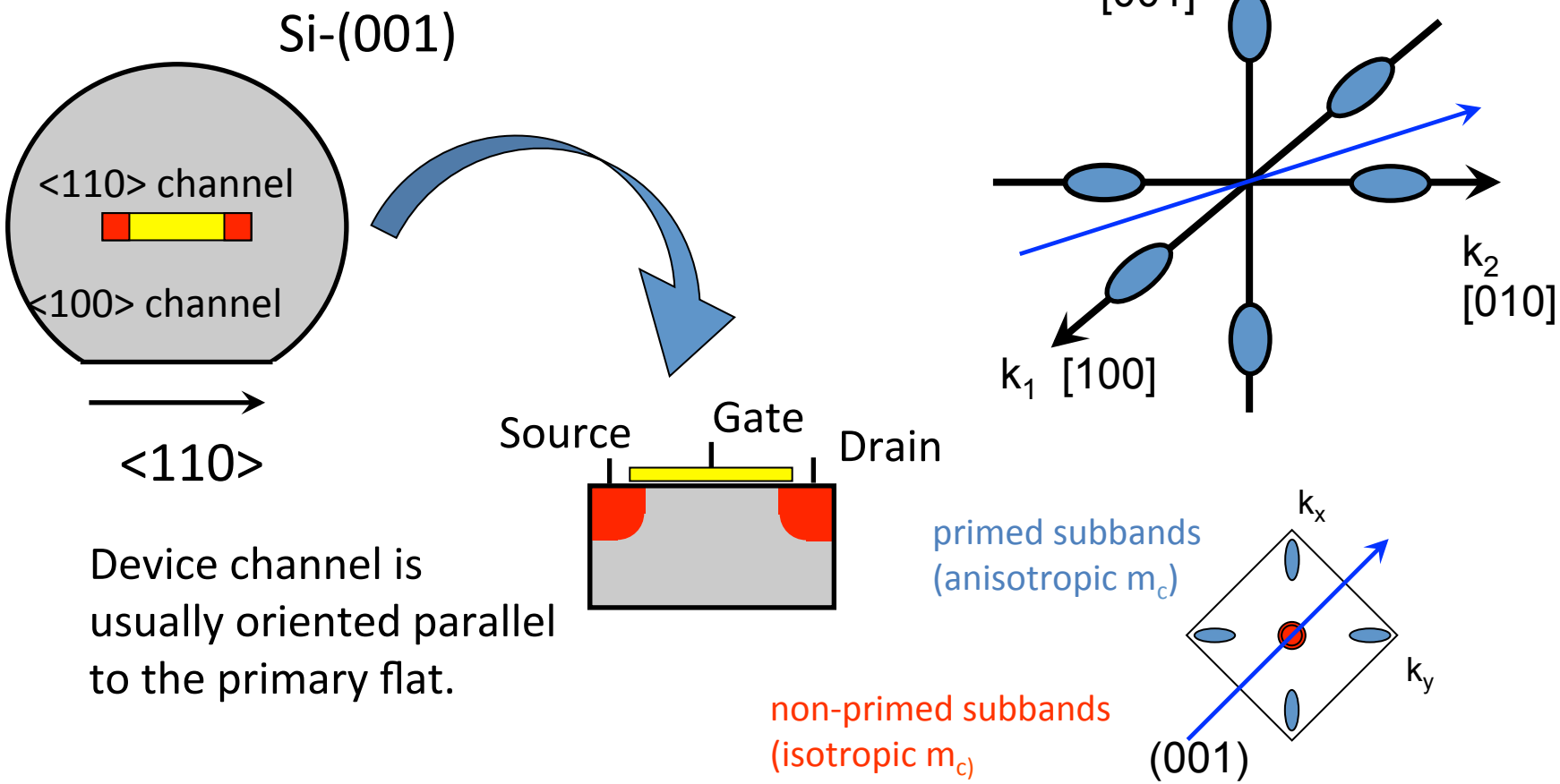
Double-Gate NMOSFET



It is useful to improve the electrostatic control of the channel and avoid the Short Channel effects appearing in devices with Silicon channel length in the range of nanometers.

Crystallographic orientation

In conventional planar Si technology, (001) crystal orientation is generally used for MOSFETs.



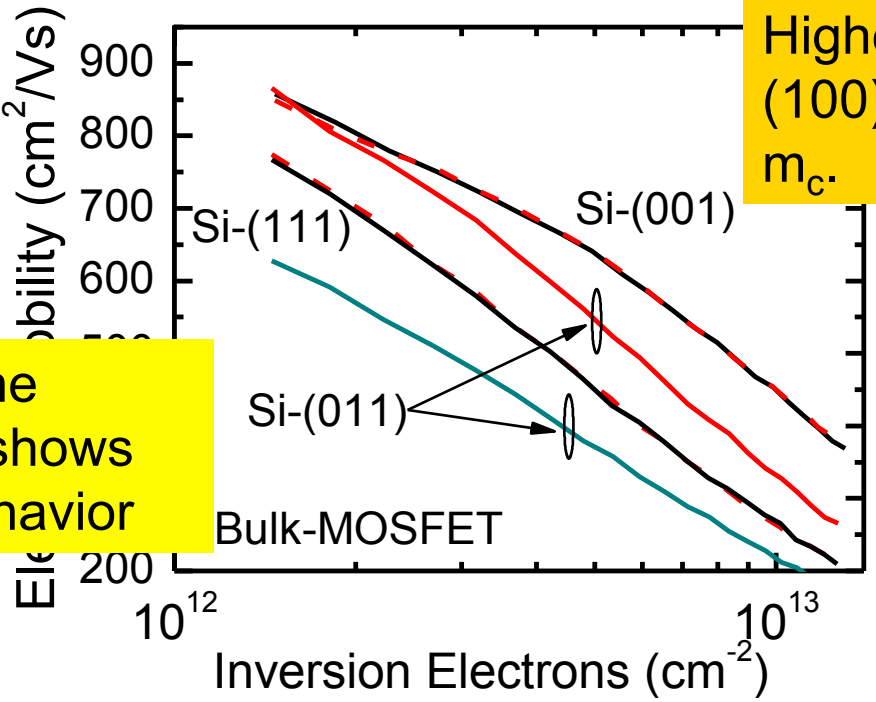
Device channel is usually oriented parallel to the primary flat.

primed subbands (anisotropic m_c)

non-primed subbands (isotropic m_c)

Mobility and orientation

Mobility is higher in Si-(001) wafers regardless the channel orientation



Higher mobility in Si-(100) due to lower m_c.

Only in Si-(110) the electron mobility shows an anisotropic behavior

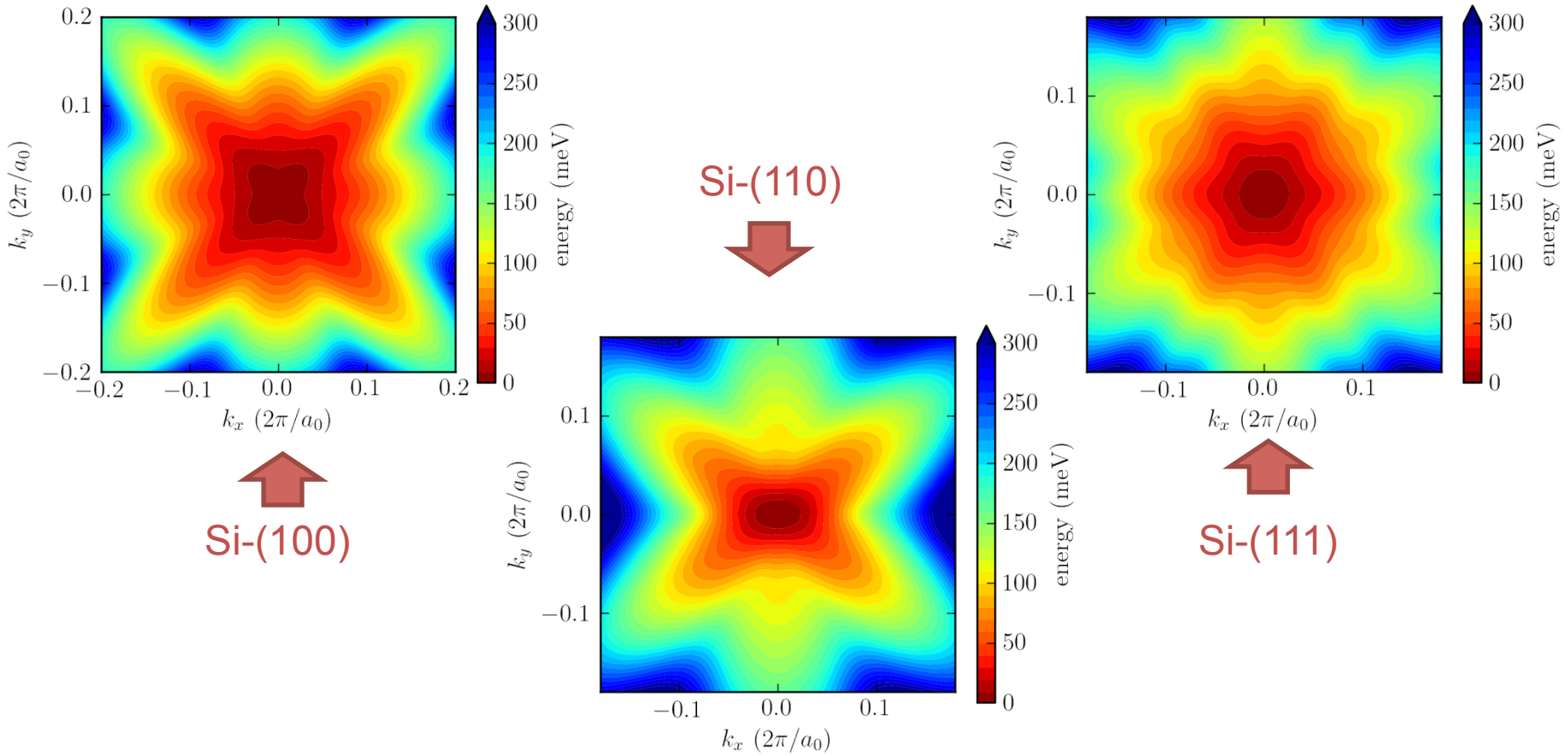
Electron mobility depends on:

1. Quantization direction
2. Channel orientation

Simulation of PMOS: Holes

For holes, energy is a non-trivial function of the moment:
To calculate it, the k·p method is employed

Some examples of auto-consistent solution of the k·p model for inversion Silicon layer: crystallographic orientation effect

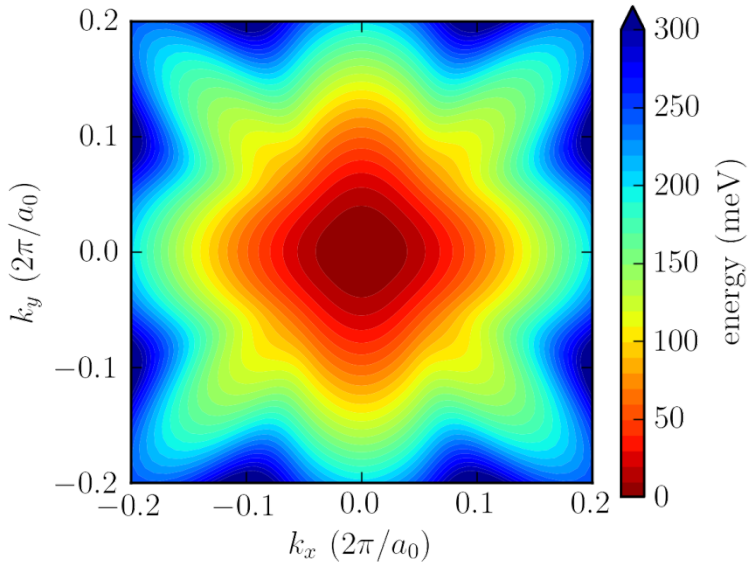


Simulation of PMOS: Holes

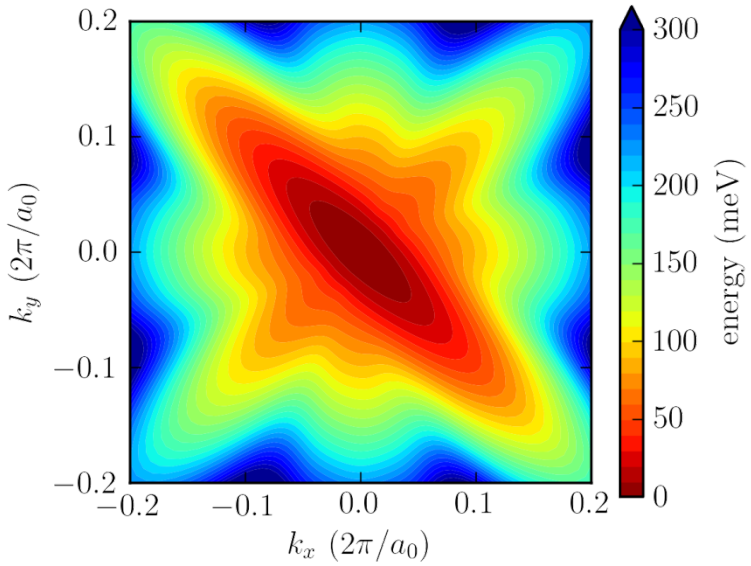
For holes, energy is a non-trivial function of the moment:
To calculate it, the k·p method is employed

Some examples of auto-consistent solution of the k·p model for inversion Silicon layer: strained substrate

Biaxal strain ($Si_{0.8}Ge_{0.2}$)



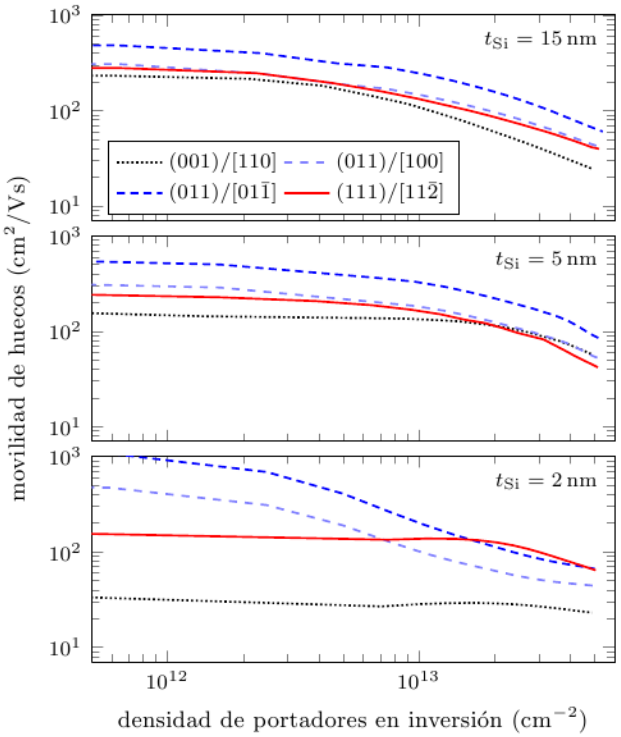
Uniaxial strain (1GP en [110])



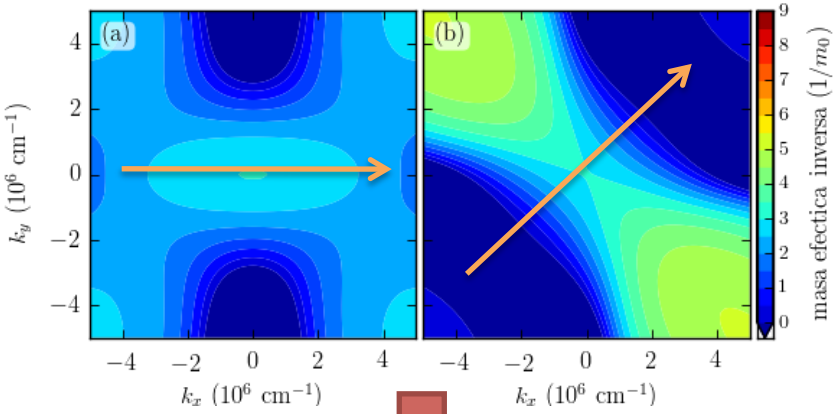
Holes: Mobility and effective mass

SOI technology devices:
Effect of the Silicon layer thickness and the orientation

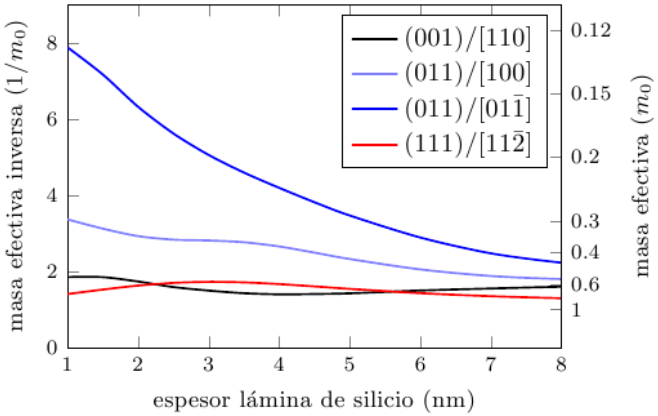
Mobility



Non-constant effective mass

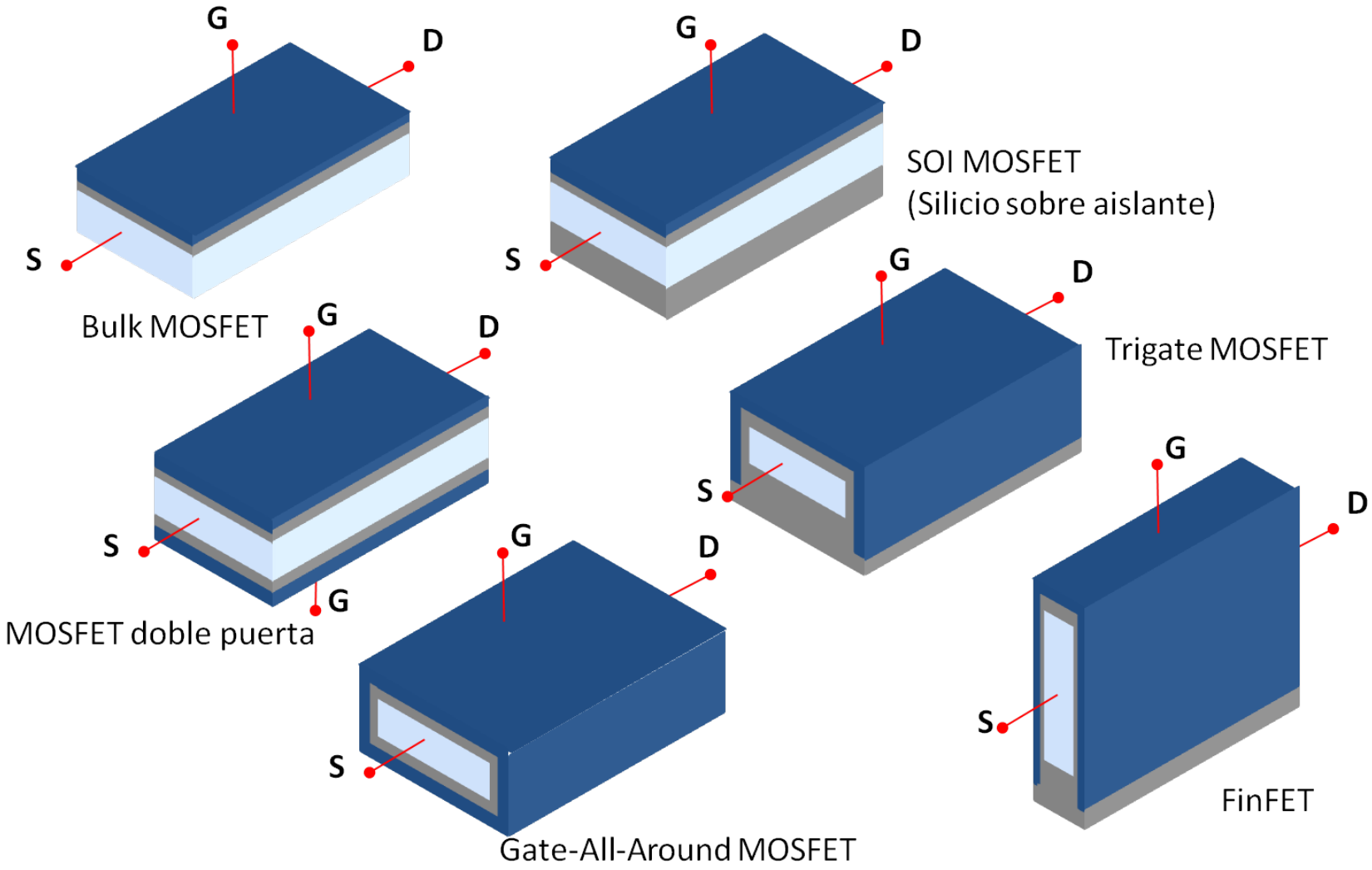


averages



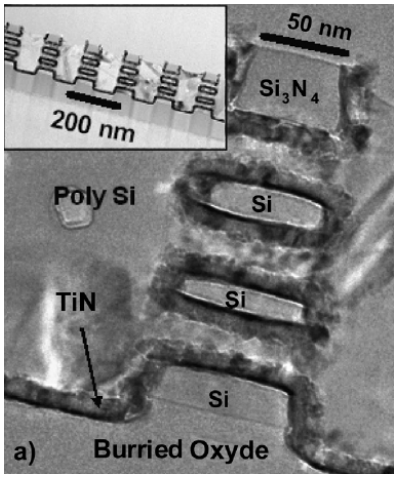
Multigate MOSFETs

Evolution of MOSFETs architecture



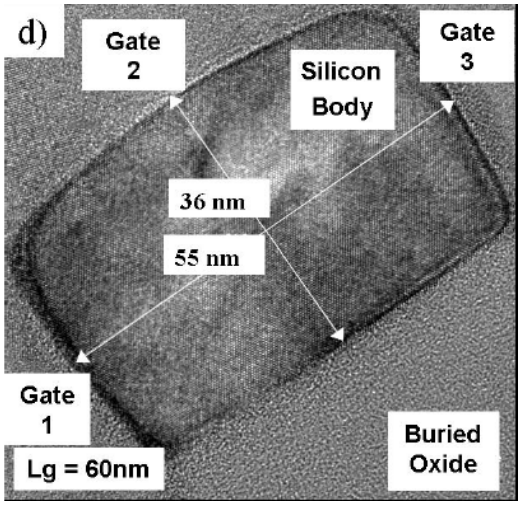
Multigate MOSFETs

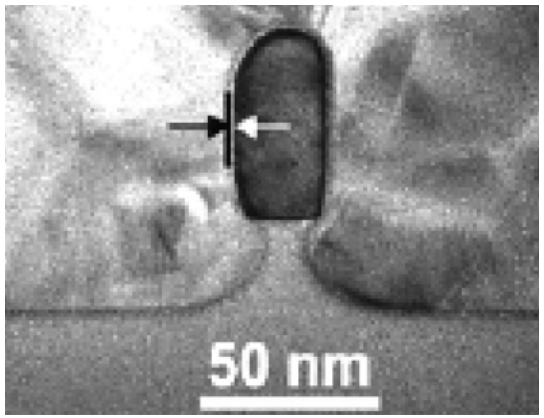
Some devices presented in the literature



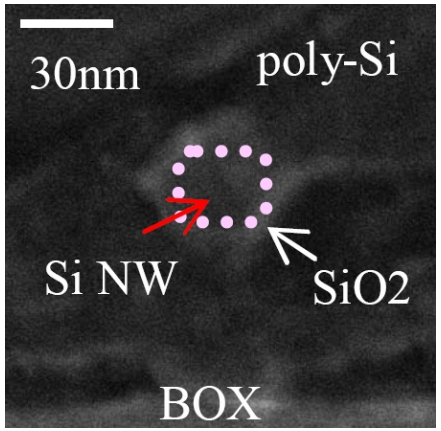
Multichannel GAA
Dupre et al., SSE 52, 519, 2008

Trigate MOSFET
Doyle et al., EDL 24, 4, 2003

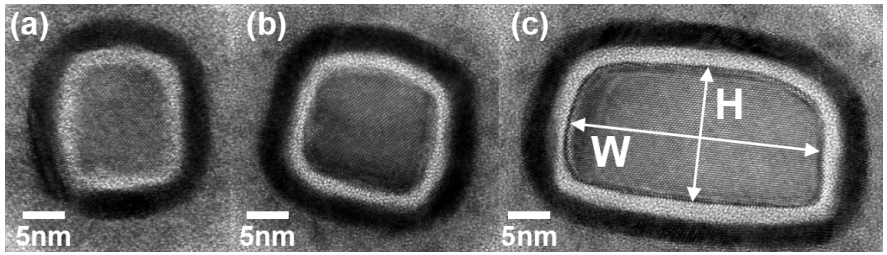




Trigate FinFET
Rudenko et al., TED 55, 12, 2008



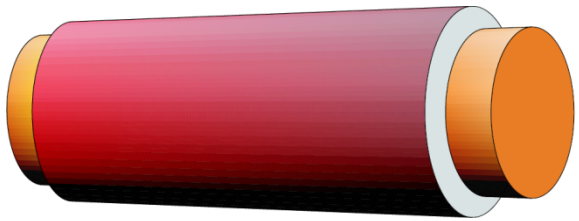
Si Nanowire
Chen et al., p. 33, VLSI 2008

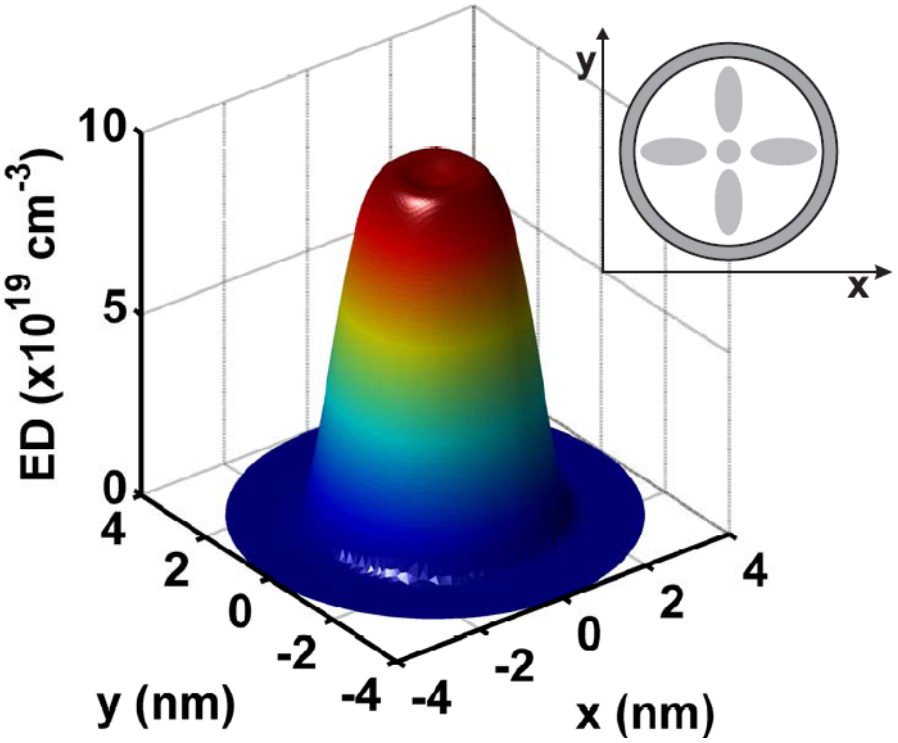


Multichannel GAA
Tachi et al., VLSI 2009.

Multigate MOSFETs

Very small devices → Quantum effects



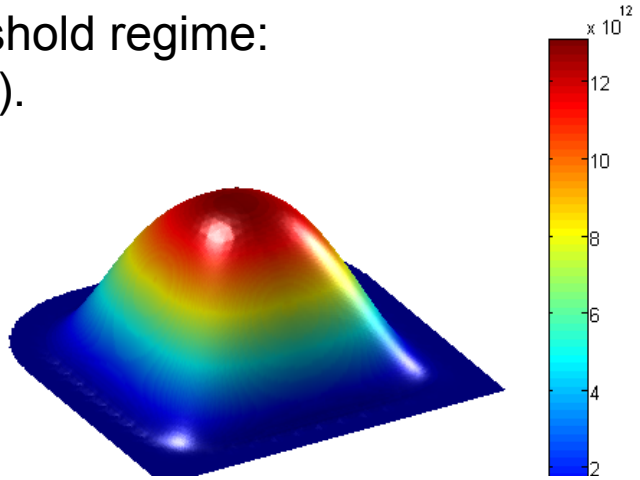


Carrier distribution in a circular section GAA with 5nm diameter.

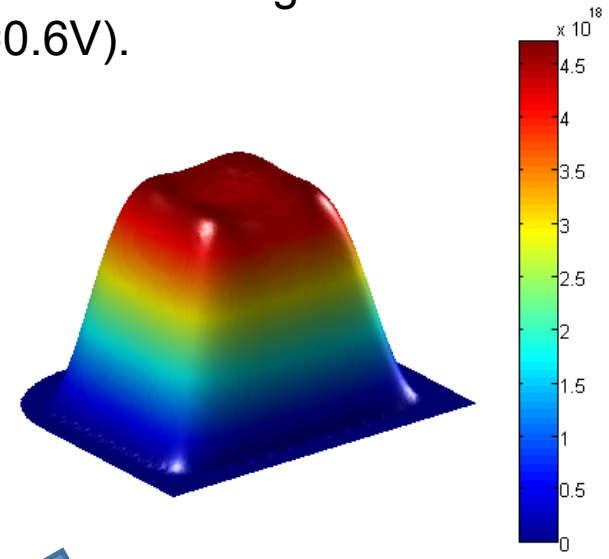
Multigate MOSFETs

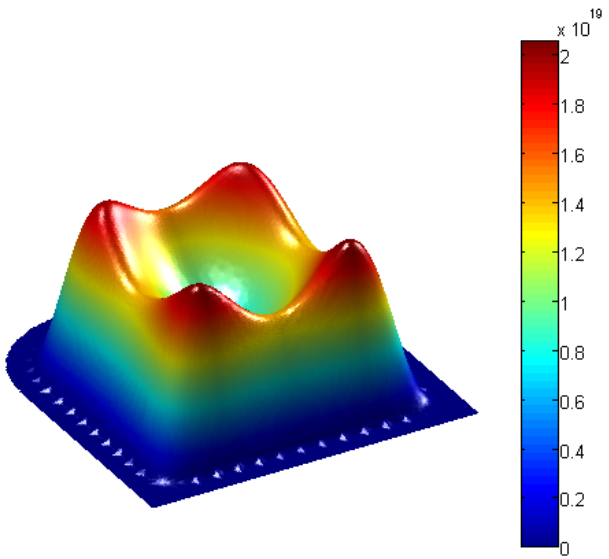
Inversion channel

Sub-threshold regime:
(V_G=0.2V).



At threshold voltage:
(V_G=0.6V).



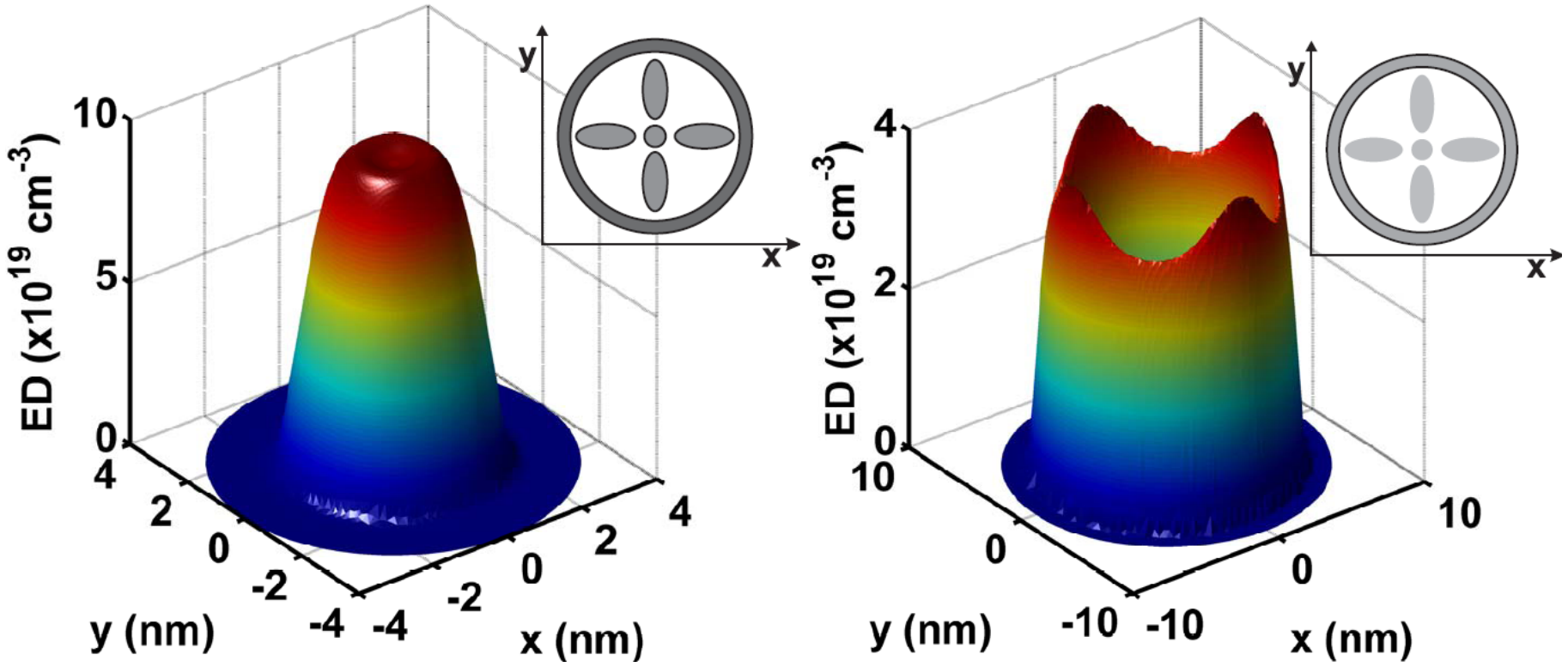


Strong inversion(V_G=0.8V).

Multigate MOSFETs

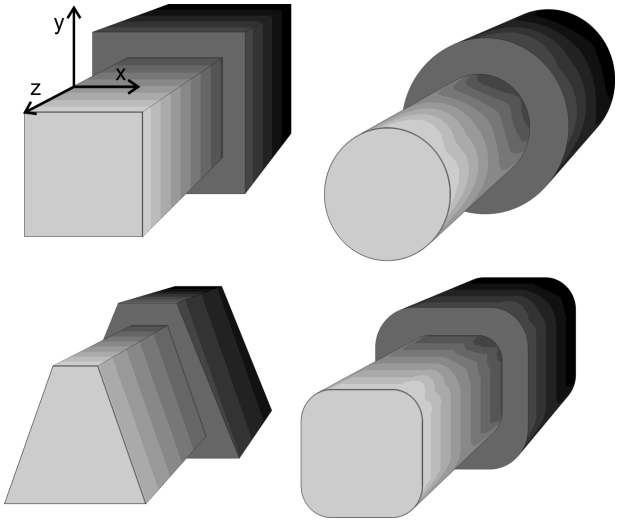
Size matters…

Comparison between d=5nm and d=15nm devices

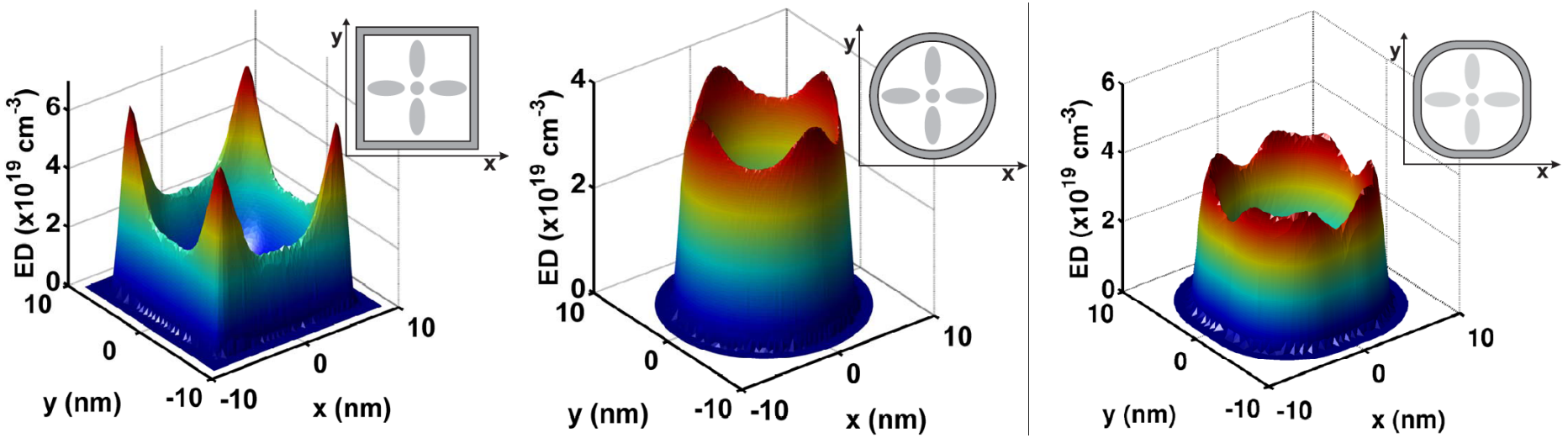


Multigate MOSFETs

Geometry effects

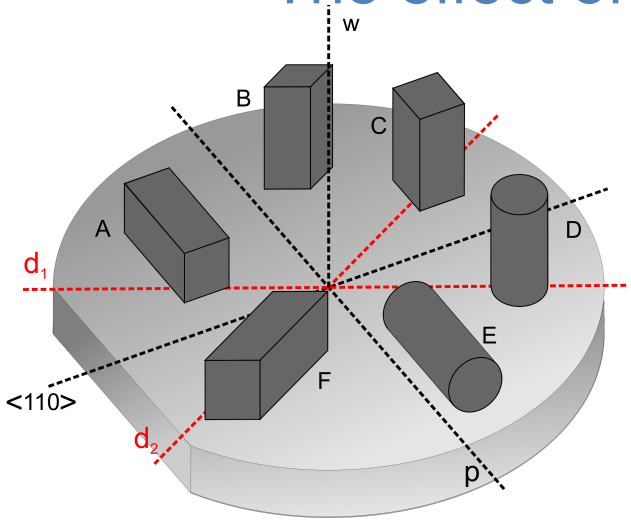


A good control of the cross-section shape may be critical

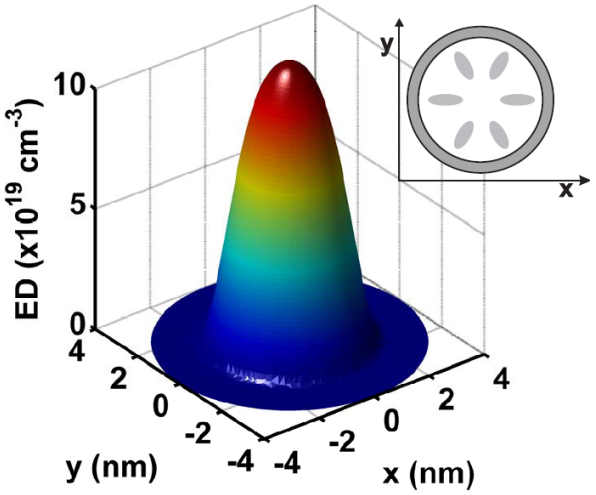


Multigate MOSFETs

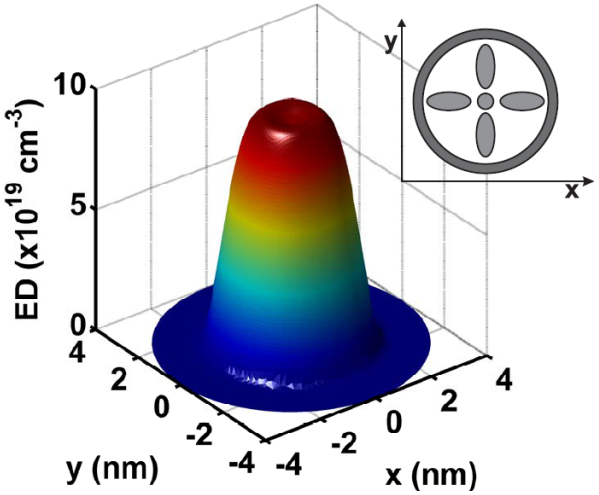
The effect of the crystallographic orientation



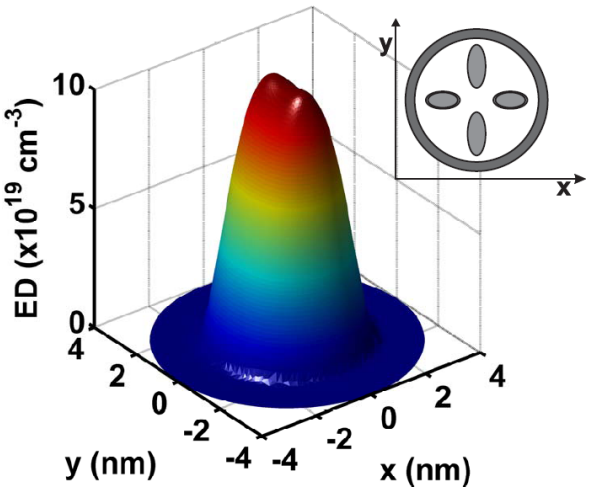
Silicon is an anisotropic material. Thus, a device characteristics depend on its orientation in the wafer.



Dirección Transporte (111)



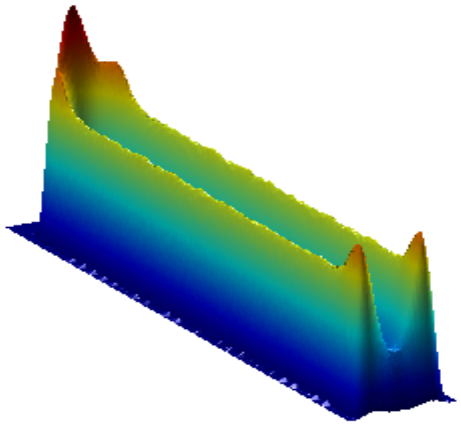
Dirección Transporte (100)



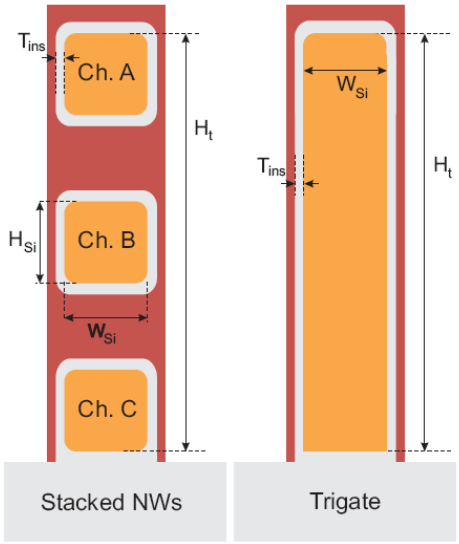
Dirección Transporte (110)

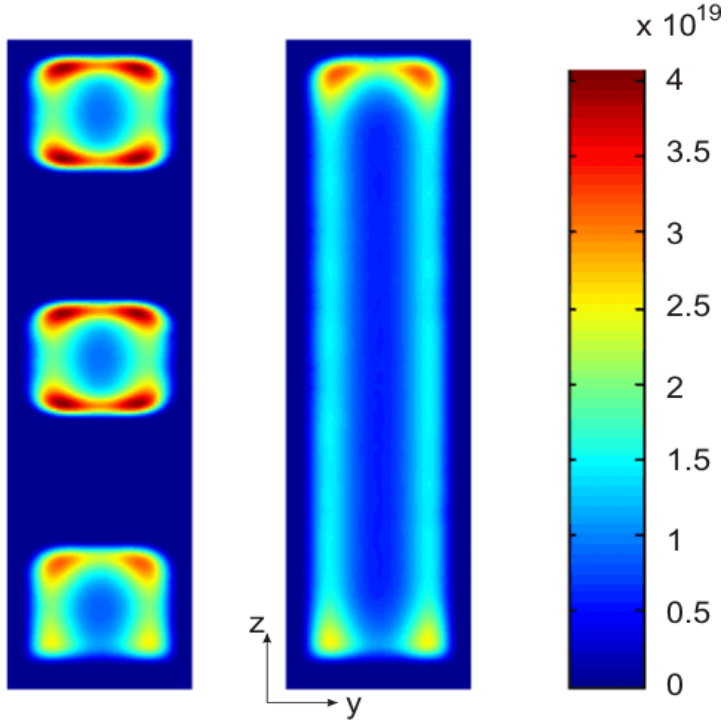
Multigate MOSFETs

Some alternatives for the design in the next technological nodes



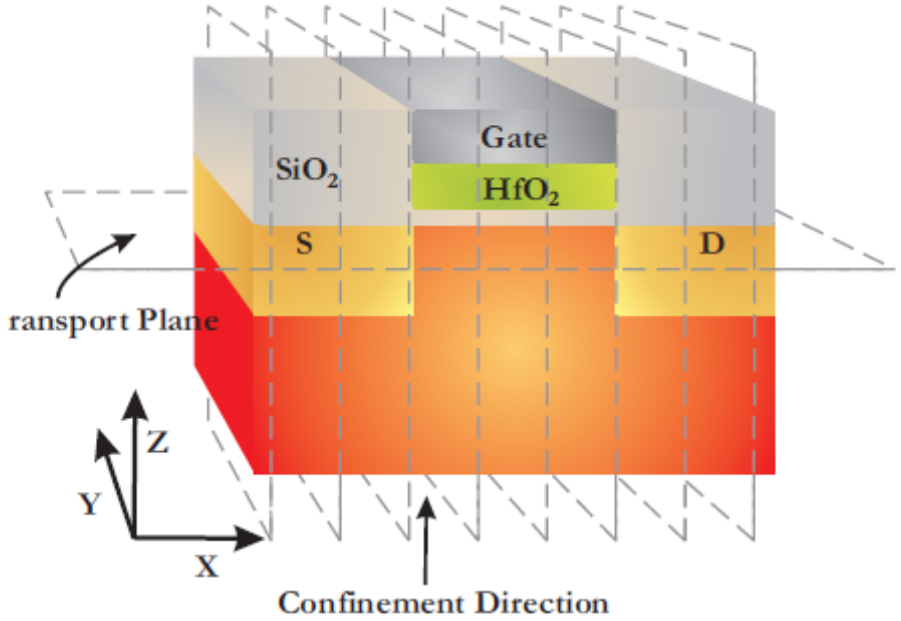
- ✓ Multigate devices → CMOS scaling
- ✓ Different design alternatives: FinFETs, MC MOSFETs, GAAs, etc.





Short Channel devices simulation: Multi-Subband EMC

Based on the space-mode approximation [Venugopal et al 2002]



Boltzmann Transport Equation

$$\frac{\partial f}{\partial t} + \frac{\vec{p}}{m} \cdot \nabla_{\vec{r}} f + \vec{F} \cdot \nabla_{\vec{p}} f = \left.\frac{\partial f}{\partial t}\right|_{coll}$$

Poisson's Equation

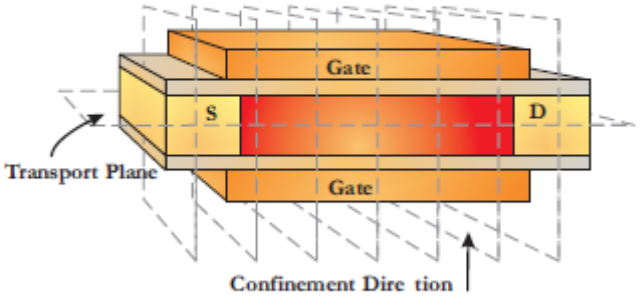
$$\nabla\left(\varepsilon \nabla V(x,z)\right) = -\rho(x,z)$$

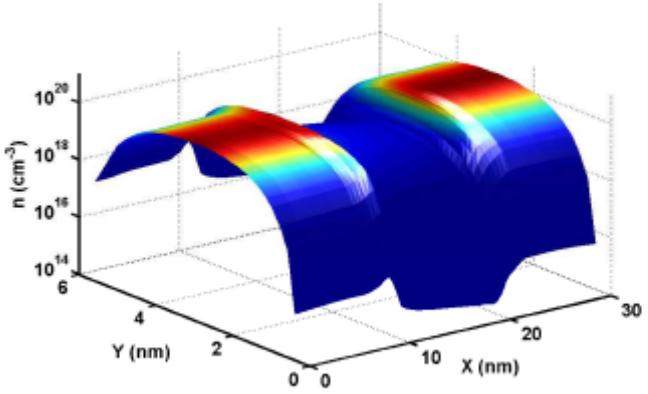
Schrödinger Equation

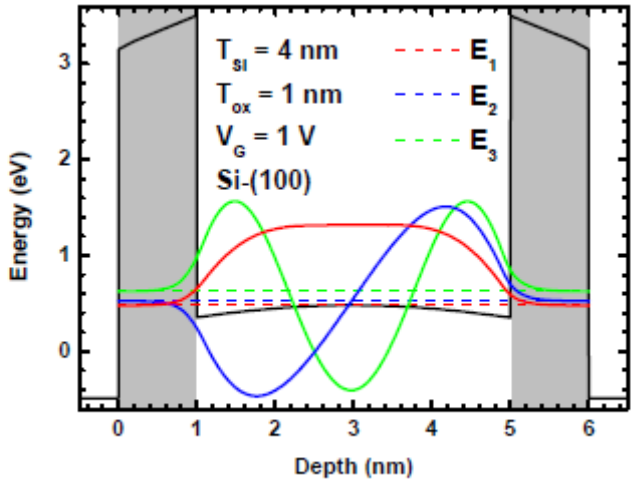
$$-\frac{\hbar^2}{2m_z^*}\frac{\partial^2}{\partial z^2}\Psi_j(z) - qV(z)\Psi_j(z) = E_j\Psi_j(z)$$

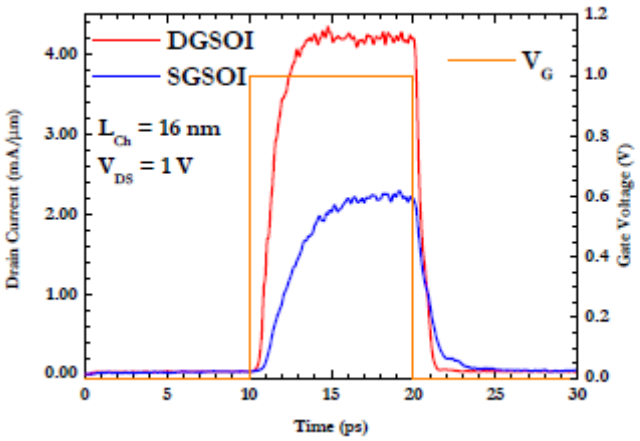
Short Channel devices simulation: Multi-Subband EMC

FDSOI, DGSOI, VMT including steady state and transient simulations





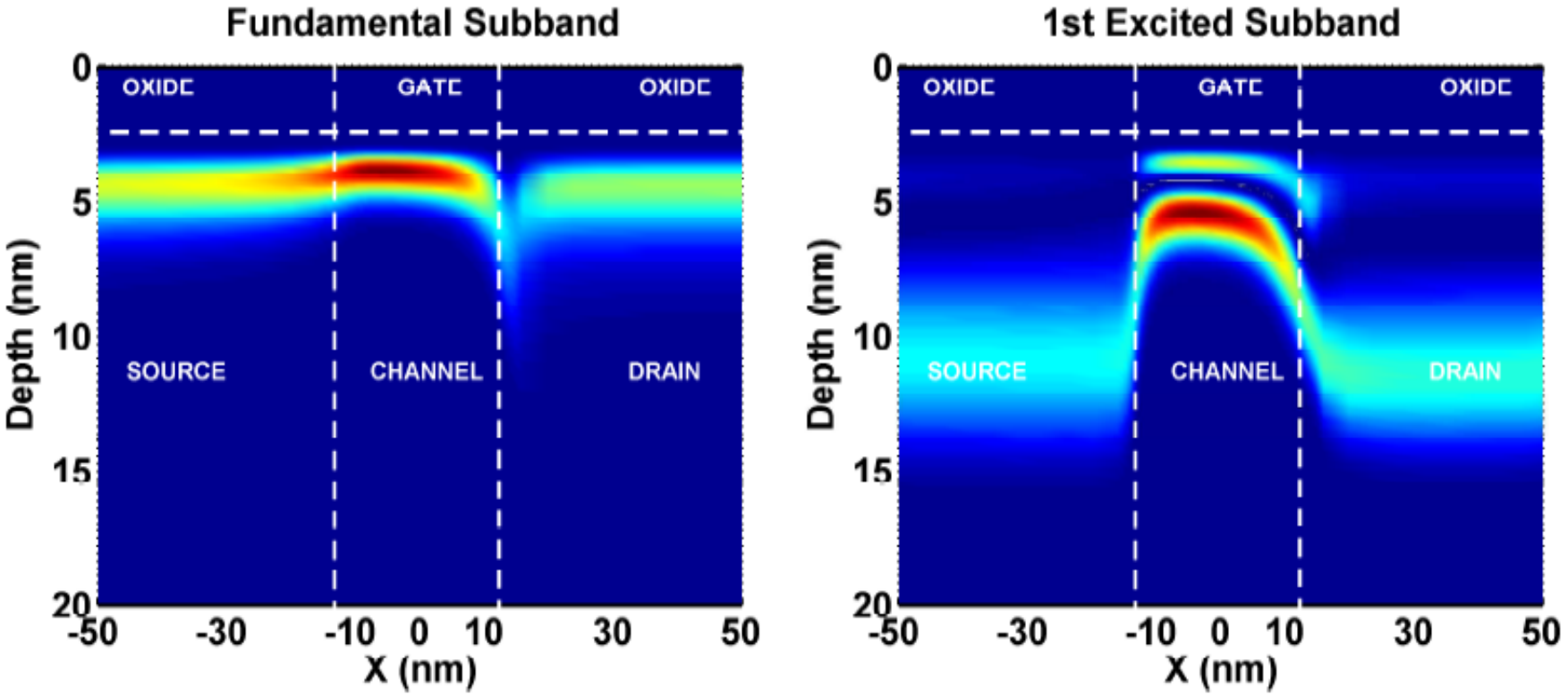




Simulation of short channel devices: Multi-Subband EMC

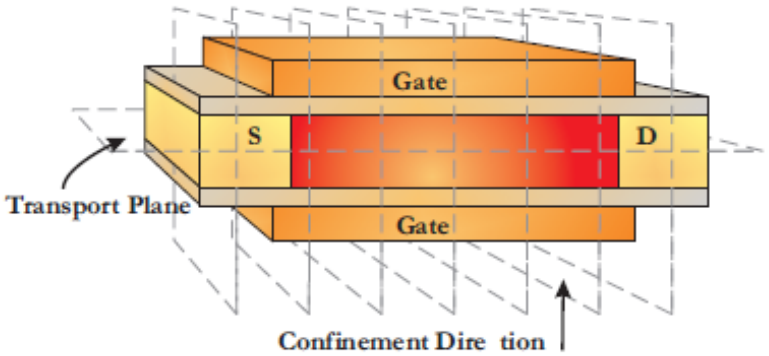
$|\psi(x,z)|^2$ calculated using the MSB-EMC

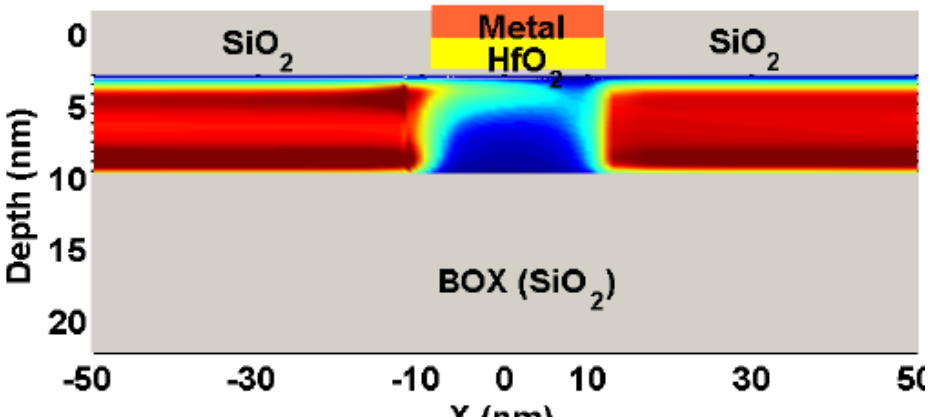
22 nm bulk-MOSFET $V_{GS} = V_{DS} = 1$ V

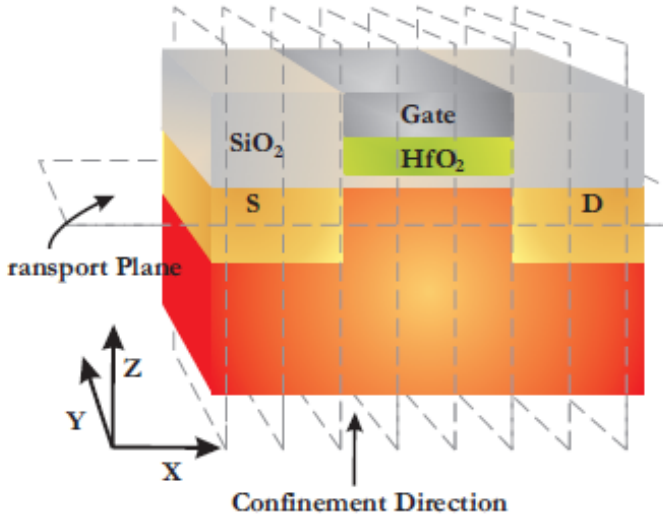


Simulation of short channel devices: Multi-Subband EMC

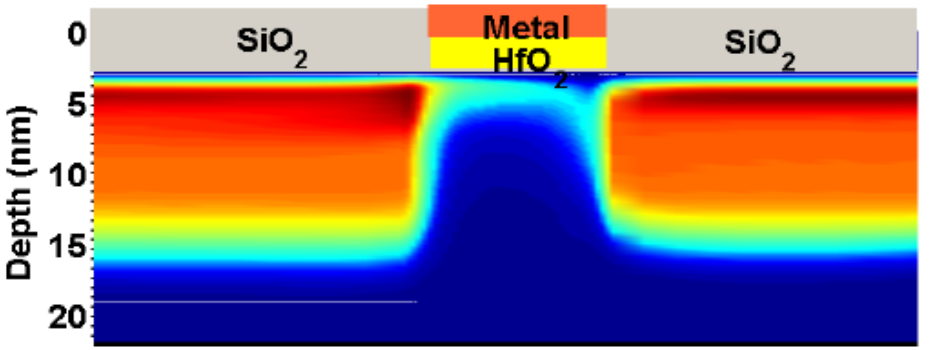
Charge distribution along the channel: SOI versus Bulk





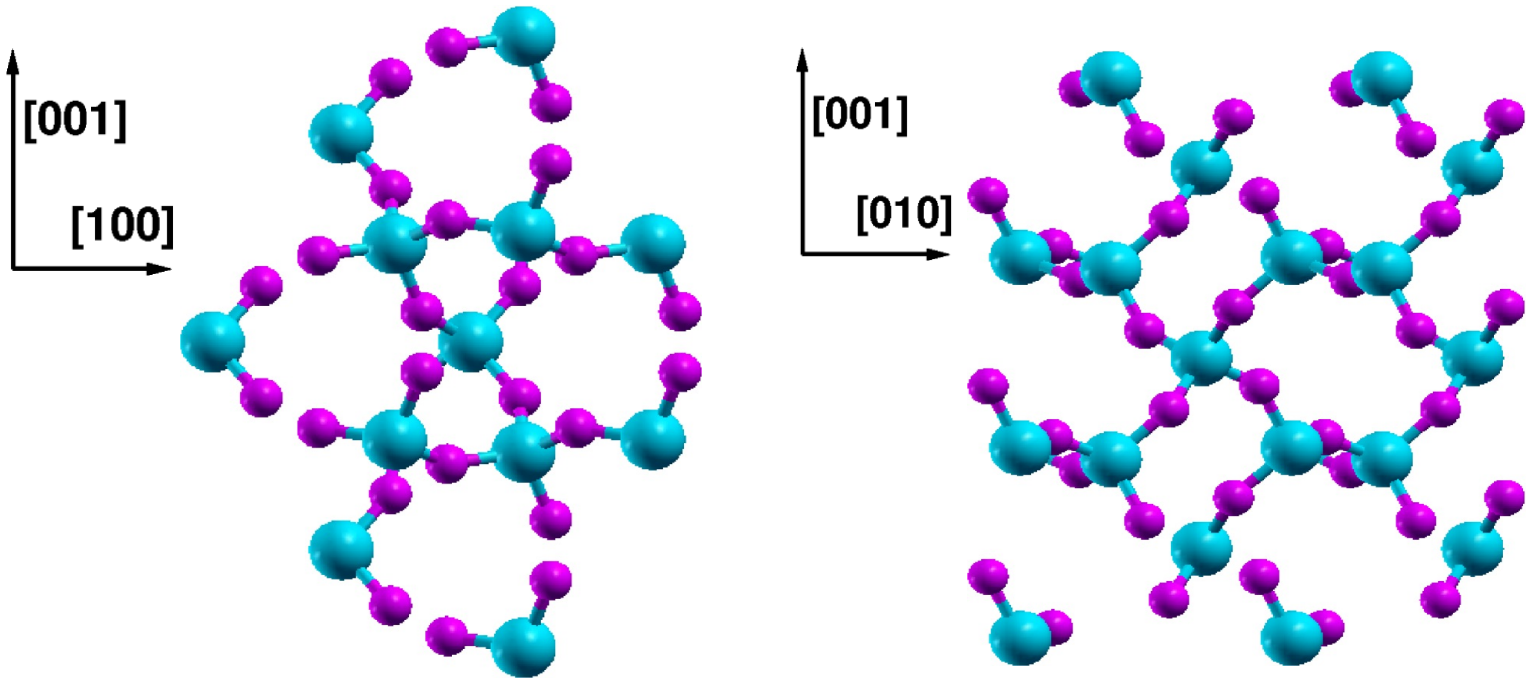


Electron Concentration (cm^{-3})



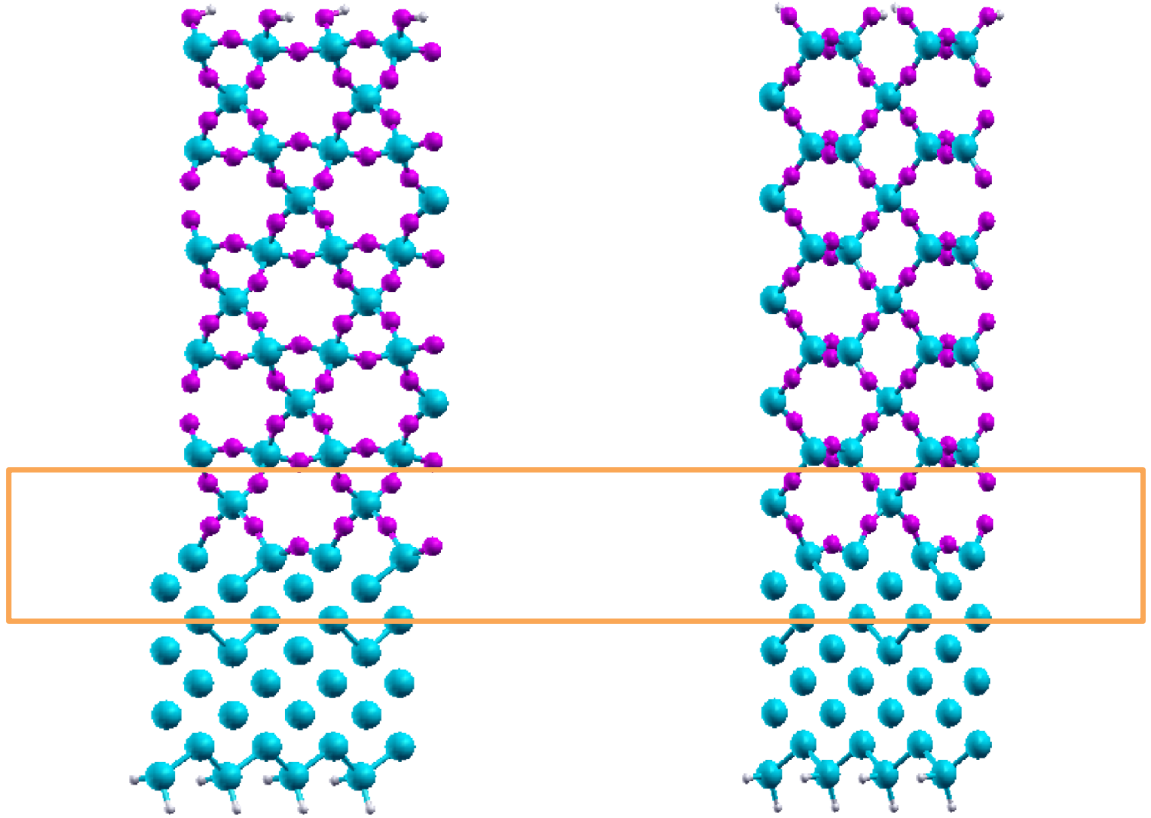
Atomistic simulations

Simulation of structural and electronic properties of bulk Silicon dioxide (SiO_2)



Atomistic simulations

Simulation of structural and electronic properties of Si/SiO2 interfaces

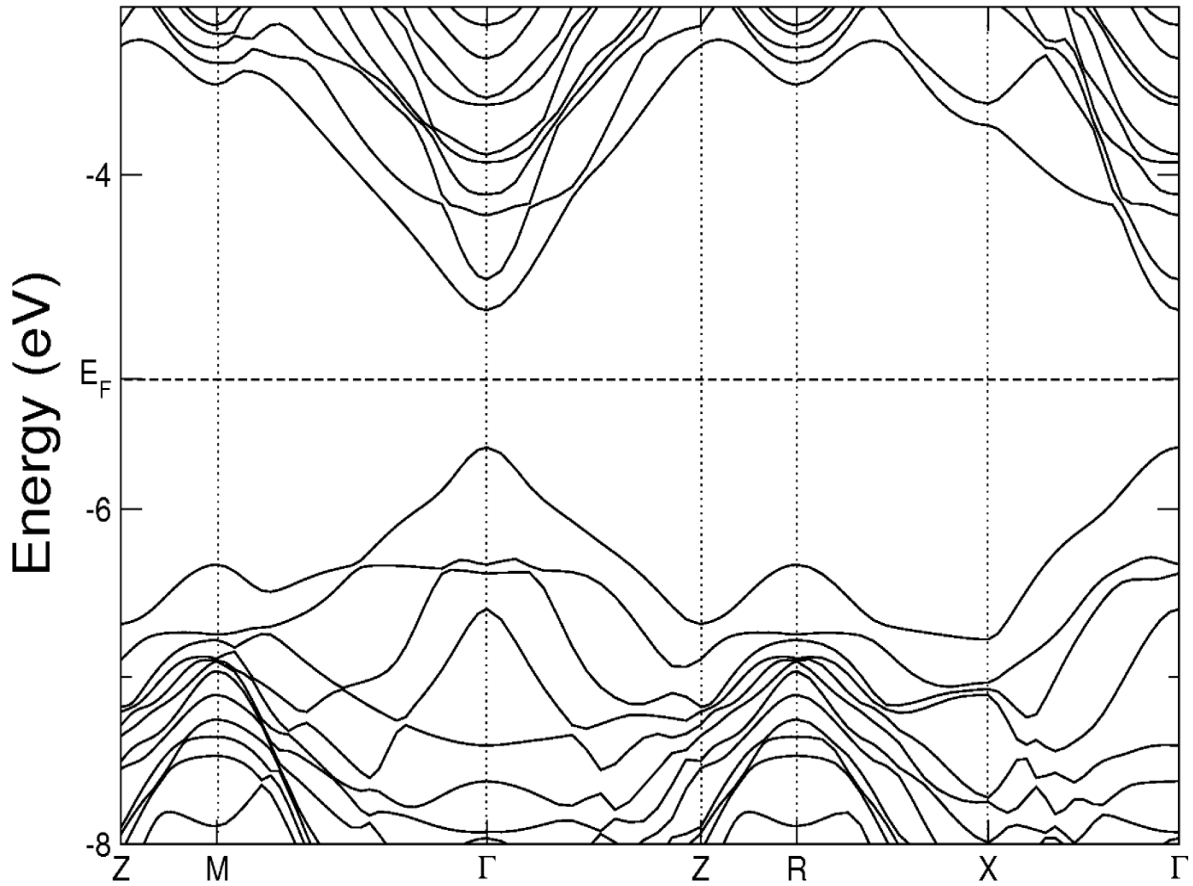


Deformation of the interface at the interfase → Deffects

Atomic structure of Silicon-on-insulator structures (Si/SiO_2)

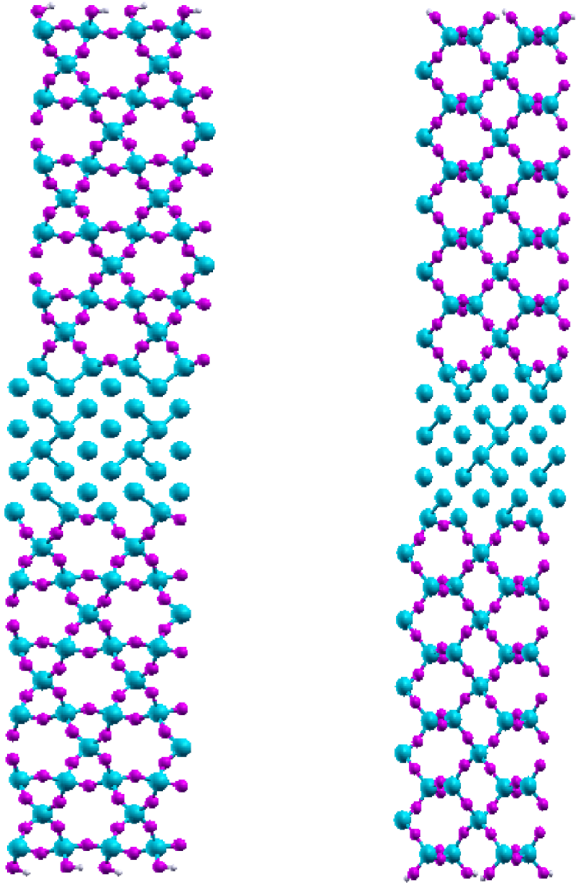
Atomistic simulations

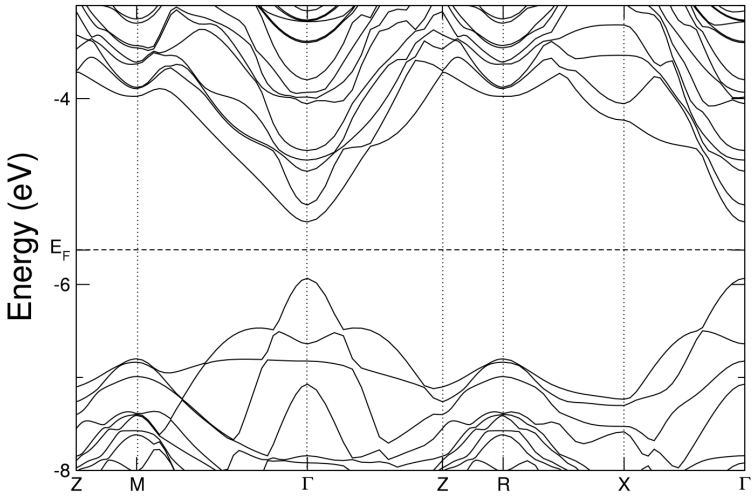
Band structure of Si (001) on SiO_2



Simulaciones atomísticas

Band structure of double-gate Si(001)/SiO_2





Possibility to study atomic-scale phenomena: dopants, dislocations, etc.

What we do

The main topics of the group are:

1. SIMULATION

- ✓ Electrostatics 1-D y 2-D
- ✓ Poisson + Schrödinger (quantum simulation)
- ✓ Psi-MOS
- ✓ Ergodic transport and Ensemble MonteCarlo, multisubband, k·p ...

2. MODELING

- ✓ Short channel effects
- ✓ Corner Effects
- ✓ Quantum corrections
- ✓ Special devices

3. CHARACTERIZATION

- ✓ I/V, C/V,
- ✓ Pulsed,
- ✓ Transient,
- ✓ Low and High Temperature,
- ✓ Magnetotransport,...

New lab

CITIC-UGR

New characterization lab

CITIC-UGR

New lab

CITIC-UGR

New lab

LAB ORGANIZATION

Low Frequency line

DC (IV, QSCV), CV, Low and High temperarure, charge pumping, Magneto-transport...

Memory line

Development of our propietary utradense memory technolgy: Transient, realibility...

High Frequency line

UWB applications, microwaves up to 26GHz

New lab

LAB ORGANIZATION

Stage 1

Basic setup

Probe stations

Psi-MOS

Semiconductor Analyzers

VNA

High-freq. Osciloscope

Stage 2

Complete UWB

Probe stations

Semiconductor Analyzers

Complete low temperature

Stage 3

Magnetotransport

Physical characterization

Opto-microwave

ICT-2007-216373

EUROSOI+

European Platform for low-power applications on Silicon on Insulator Technology

Francisco Gámiz

"Any circuit design will have the chance to become a SOI circuit using European technology"

Universidad de Granada
Departamento de Electrónica y Tecnología de Computadores

Madrid, May 7th, 2010

1. EUROSOI Network

- EUROSOI Network is funded in December 2003 with the support of the EC (Contract signed by EC on December 18th, 2003).
- 29 partners from 14 countries initially acceded to the contract.

Why EUROSOI+ initiative?

1. EUROSOI achievements have been very important; But there is plenty of challenges at the future: EUROPE is still far from the pursued international leadership in SOI.
2. There is **a lack of prototyping capability in SOI in EUROPE**, in spite of the fact that European companies have developed the most advanced SOI devices → **these devices are not accessible to many fabless companies or research groups whose designs would be much more competitive.**

Who EUROSOI+ initiative?

1. University of Granada.
2. IMEP-MINATEC
3. CEA-LETI
4. IMEC
5. Université Catholique Louvain
6. Tyndall
7. Chalmers

Work Progress (M0-M36)

- WP2. Networking activities

  - Task 2.3 Exchange program:
    1. 15 weeks in 2008
    2. 20 weeks in 2009
    3. 4 weeks in 2010
    4. 8 weeks in 2011

  - Task 2.4 Sponsoring of events:
    1. 2008 IEEE International SOI Conference
    2. Korean International Summer School on Nanoelectronics (nanoKiss)
    3. International SemOI Workshop (Ukraine)

EUROPRACTICE

EurSOI

Work Progress (M0-M36)

- WP3. Training activities
  - Task 3.2 Inventory of SOI training material
  - Task 3.3 Organization of short courses:
    - *Multigate SOI MOSFETs (Cork 2008) 46 attendees.*
    - *SOI from modelling to design (Chalmers, 2009) 45 attendees.*
    - *Exploring new routes with SOI (Grenoble 2010) 53 attendees.*
    - *Silicon on insulator technology for future electronics (Granada 2011) 75 attendees*

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EurSOI

Work Progress (M0-M36)

- WP3. Training activities
  - Task 3.4 SOI Training events.
    - 2009 MIGAS School (52 students)
    - SOI training course at ESSDERC-2010 organized by Prof.JP Colinge
    - Tutorial on Nanoelectronics technology at ESSDERC-2010 (organized by Prof.Francisco Gamiz)

EUROPRACTICE

EurSOI

Work Progress (M0-M36)

- WP4. Workshops and meetings
- **Task 4.3 Scientific & Industrial Panels**

1. **Cork-2008:**

   "Key Issues in SOI: Solutions and Ideas"

2. **Chalmers-2009:**

   "What is the killing advantage of multiple-gate SOI MOSFETs:electrostatics and scalability, transport or functionality?"

3. **Grenoble-2010:**

   "SOI technologies: What kind of research for what kind of products?"

   (SOITEC, GlobalFoundries, STMicroelectronics, Innovative Silicon, IBM, SOI Industry Consortium)

EUROPRACTICE

EurSOI

Work Progress (M0-M36)

- WP4. Workshops and meetings
- **Task 4.3 Scientific & Industrial Panels**

4. Granada-2011:

"The contribution of SOI in the brilliant future of Nanoelectronics" January, 18th, 2011

Participants:

-Bruce Doris, IBM
-Carl Das, IMEC
-Olivier Faynot, LETI
-Malgorzata Jurczak, IMEC
-Max Fischetti, TUDallas, USA
-Nobuyuki Sugii, LEAP, Japan
-Moderator: Francis Balestra, Sinano Institute, France

EUROPRACTICE

Work Progress (M0-M36)

- WP5. Platform for the design of low-power SOI circuits

“Any circuit design will have the chance to become a SOI circuit using European technology”

EUROPRACTICE

EurSOI

MPW offer through CMP: timetable first run

- 10Q4 end – Distribution of DK via CMP
- 11Q3 (sept) – GDS to be delivered to CMP
- 11Q4 beg. – Tape-out and run start
- 12Q1 end – Silicon delivery

For more information on accessing the MPW go to CMP website: http://cmp.imag.fr/

For more information on the FDSOI offer contact: carlo.reita@cea.fr

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