Si-based electronics

The last ITRS node...
Is there life beyond it?

W. Kuzmicz
Warsaw University of Technology

First NANO-TEC Workshop
Granada, 20 January 2011

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Let's look for it and call it a bridge technology

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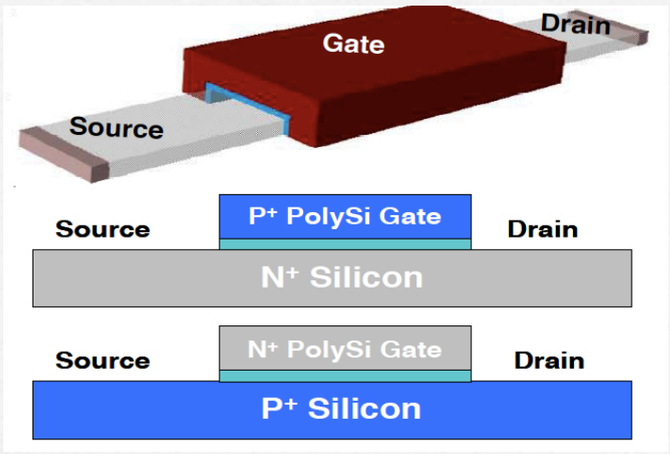
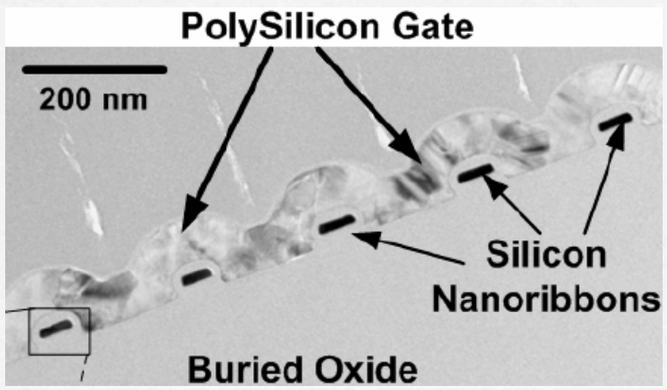
Junctionless FET

SOI Gated Resistor

J.P.Colinge et al.,
2009 IEEE Int. SOI Conf.

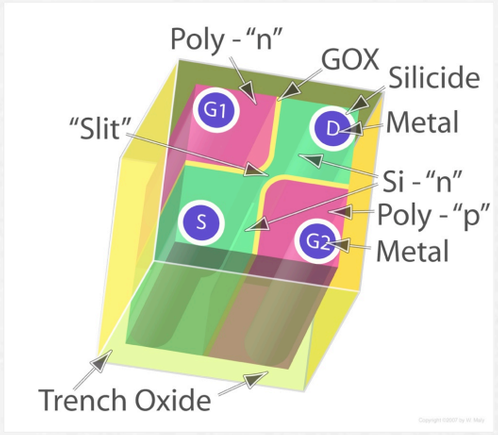


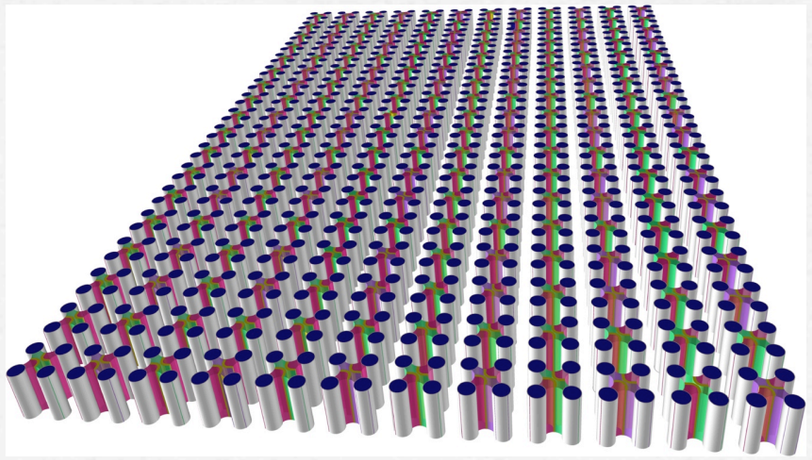


Source: J.P.Colinge et al., conference presentation

Vertical Slit FET

W. Maly,
US patent application 2007





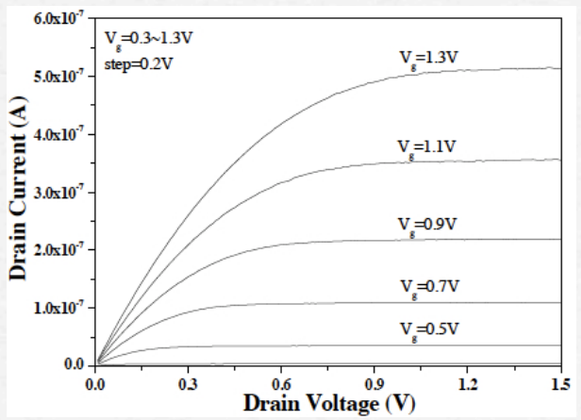
Source: courtesy of W. Maly

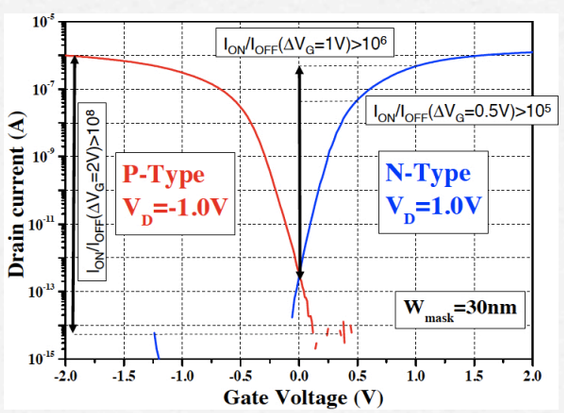
Junctionless FET

SOI Gated Resistor

Vertical Slit FET

Ideal subthreshold characteristics: ~60 mV/decade, good output characteristics





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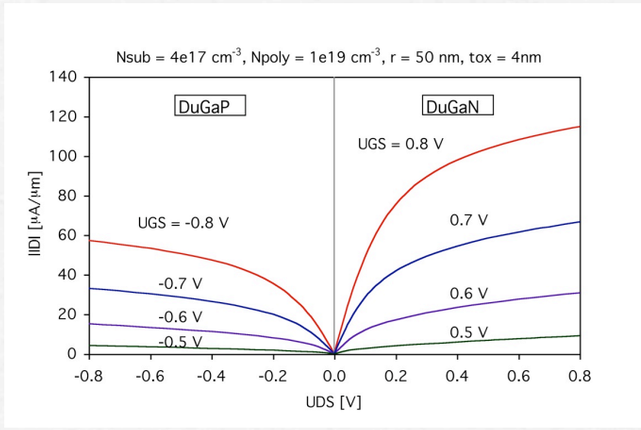
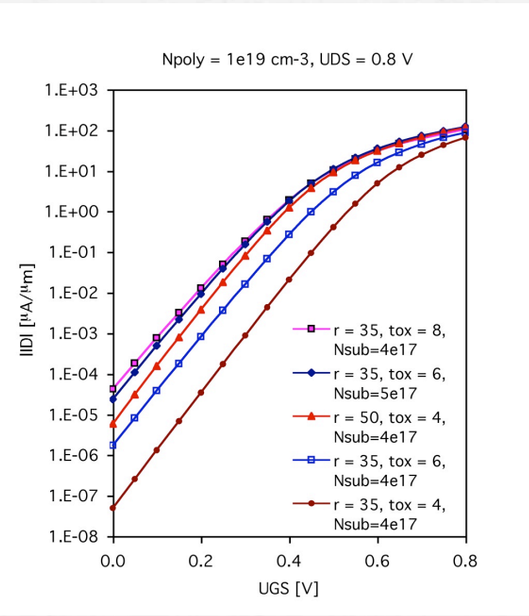


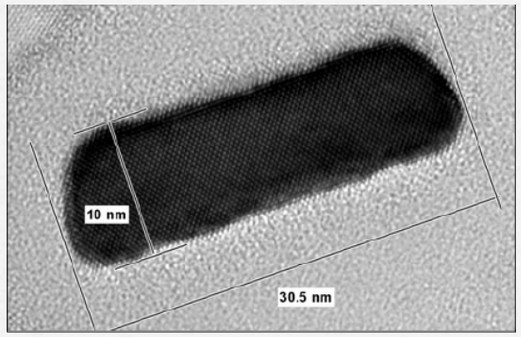
Source: courtesy of A. Pfitzner, Warsaw Univ. of Technology



Experimentally confirmed

Junctionless FET

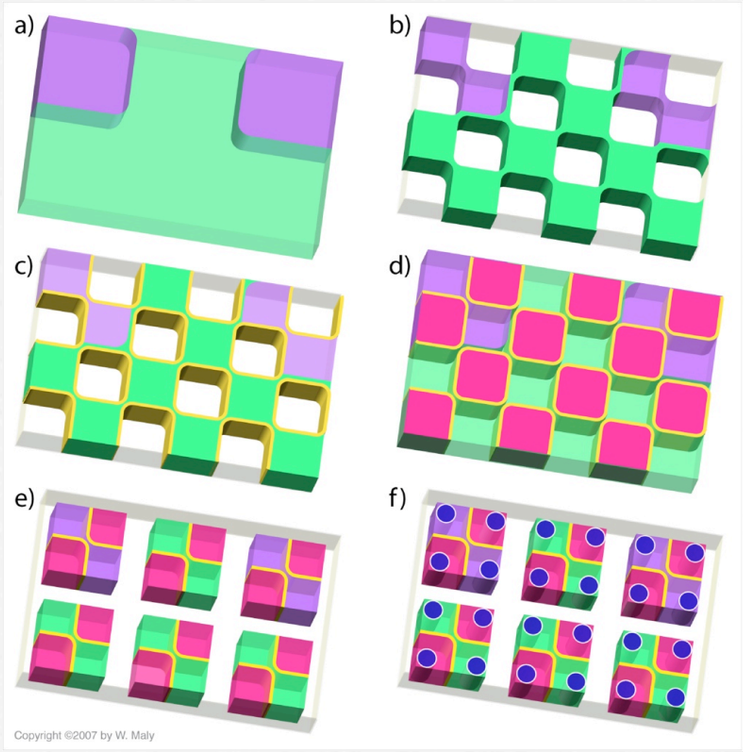
SOI Gated Resistor

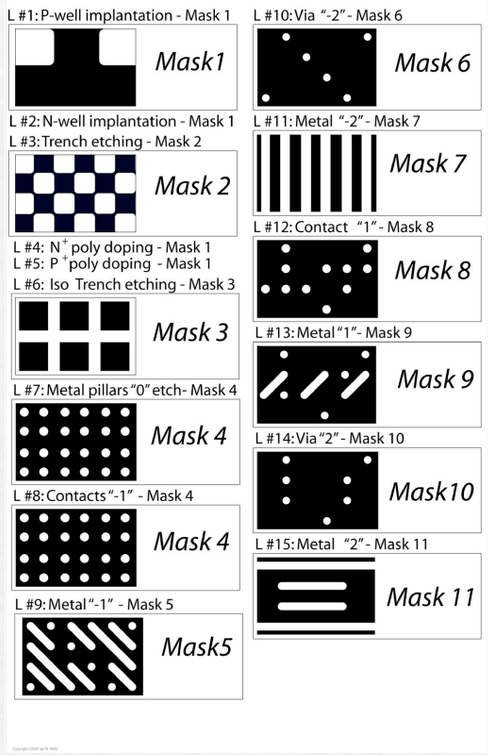


Technology:
Si nanoribbon on SOI

Source: J.P.Colinge et al., conference presentation

Vertical Slit FET





VESTIC technology:
All processes routinely used in CMOS, litho friendly

Source: courtesy of W. Maly

Benchmarking

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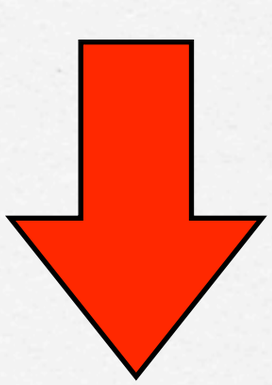

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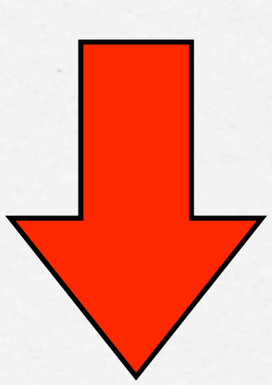

What should be assessed is the circuit performance, not raw device characteristics

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6. Cost per function (…but can we estimate it?)

Benchmarking framework

Tech	Version	Performance	Integrability	Manufacturability	Variability and yield	Design	Cost(?)
Fin FET	…						
	…						
TFET	…						
	…						
Jless FET	…						
	…						
…	…						
	…						

Thank you!

Now it’s YOUR turn:
questions and suggestions, please!