4th Workshop: Elaboration of Recommendations

Wrap-up slides

Clivia M Sotomayor Torres (ICN)

OUTLINE

About NANO-TEC

- Context
- Objectives and partners

ACTIVITIES

- Workshops: summary recommendations from 1st to 3rd workshops
- Panel on Bridging the gap between Technology and Design

RECOMMENDATIONS FROM THE FINAL WORKSHOP

- Charge-based state variables
- Non-charge-based state variables
- New computing paradigms
- Technology Ecosystem.
- Design Panel

CONTEXT

The JU AENEAS covers the whole of nanoelectronics research, ***except*** the Beyond CMOS Domain.

Beyond CMOS research is carried out mainly in academic and research organisations.

Existing consortia cover several domains including Beyond CMOS, which lacks visibility in the ERA and in the EU Framework program.

Given the existence of the JU AENEAS and the room for the EU to fund Beyond CMOS research, a community with long-term research interests in nanoelectronics is needed.

Of key importance is to address the design issues in Beyond CMOS and build a bridge between technologies and design or, better still from novel device concepts through technologies, systemability, to design for applications.

OBJECTIVES AND PARTNERS

To identify the next generation of (emerging) device concepts and technologies for ICT.

To build a joint technology-design community to coordinate research efforts in nano-electronics.

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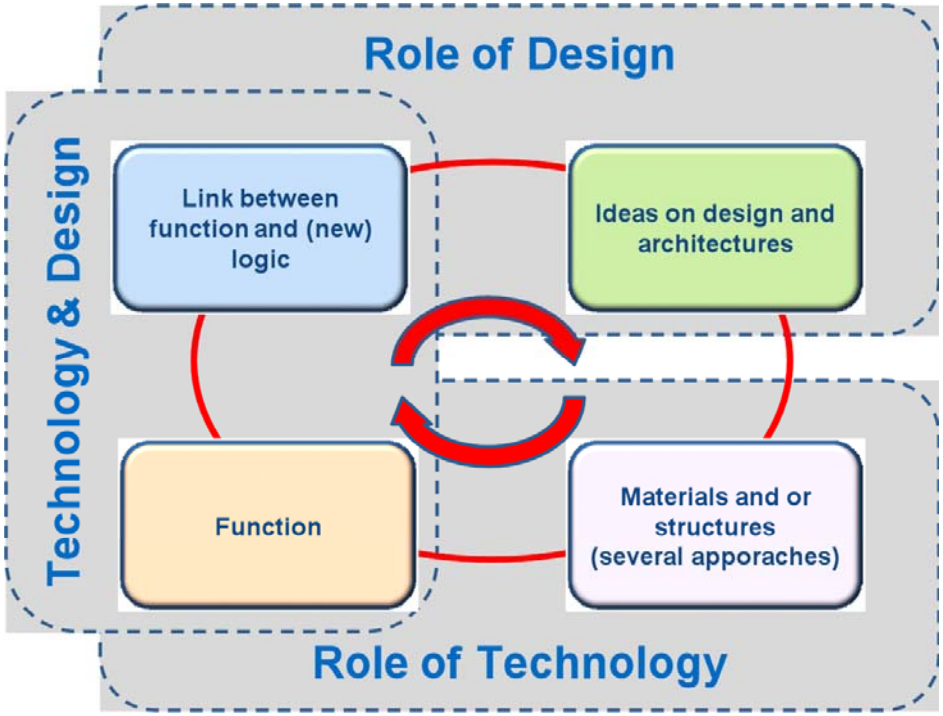
ACTIVITIES



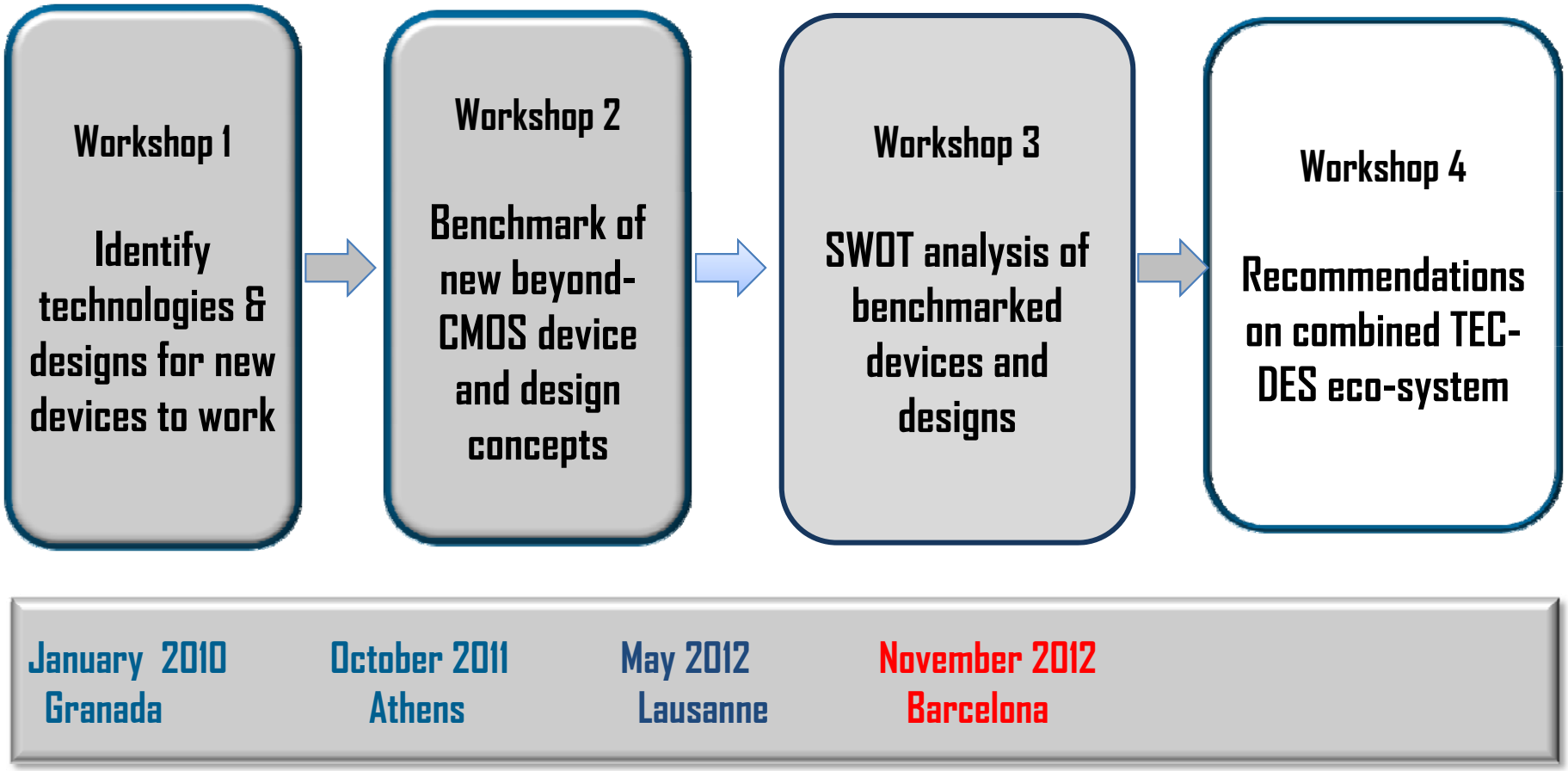
4 workshops with invited experts on Beyond CMOS devices, benchmarking and a SWOT analysis of new devices.

A state-of-the-art web platform for working groups, enabling discussions fora, meetings, communications and access to an information repository.

A report on Emerging Nanoelectronics.

NANO-TEC Workshops timeline

Main mechanism to reach suitable recommendations



WS1 CONCLUSIONS & RECOMMENDATIONS (non-exhaustive)

Address cross-cutting issues:

Power consumption, manufacturability and cost vs. performance.

New technologies issues:

Device functionality at the nanoscale needs to be strengthened
Increasing need for new architectures
Alternative concepts to do computation.

Beyond CMOS design issues:

Variety of nanodevices and materials
Novel circuits and architectures needed to exploit fully nano components.
Mode of operation of such devices?
Multi-scale approach needed in to describe realistic systems.

Some recommendations:

Graphene and molecular electronics need targeted programs.
Spintronics needs a targeted program on architectures and systemability.

WS2 CONCLUSIONS & RECOMMENDATIONS (non-exhaustive)

General recommendation:

- Refine the benchmarking methodology to cover a wider range of Beyond CMOS technologies and design approaches.
- Memory or switching functions of FET-like devices found too restrictive.
- In some cases benchmarking needs to be application-specific.

Common specific recommendation:

- The design component must be built-in from the very beginning.
- Make use of the 3rd dimension, eg, MEMS
- Initially seek to integrate on a Si platform, eg. Quantum computing
- Variability and systemability seen as main challenges.
- Thermal issues and stability need to be addressed.
- Design tools need to incorporate multi-physics and multi-scale approaches.

WS3 CONCLUSIONS & RECOMMENDATIONS (non-exhaustive)

Considering all technologies discussed:

Strengths	Weaknesses
• Application perspectives • Building blocks for innovation in nanoelectronics • European industrial/academic ecosystem	• Physical constraints • Compatibility issues with conventional technology • Reliability, variability
Opportunities	**Threats**
• Design of circuits and systems • 3D integration of multifunctional systems • Industrial/academic cooperation	• Gap to industrial needs? • 'CMOS competition' • Manufacturability

BRIDGING THE GAP BETWEEN TECHNOLOGY & DESIGN

Based on panel discussions and presentations:

- Strands reflect current approaches in the design community
- Material → property → function → application
- Modelling → design
- Device → systemability → system

From modelling to design

We can simulate transport in molecular and semiconducting nanostructures quite reliably, accounting for charging effects, dissipation, screening as long as the molecular systems consist of a sufficiently small number of atoms,

but

the simulation of realistic systems, especially in terms of the contacts and in general the coupling with the external environment is still a problem

Paolo Lugli

OUTLINE

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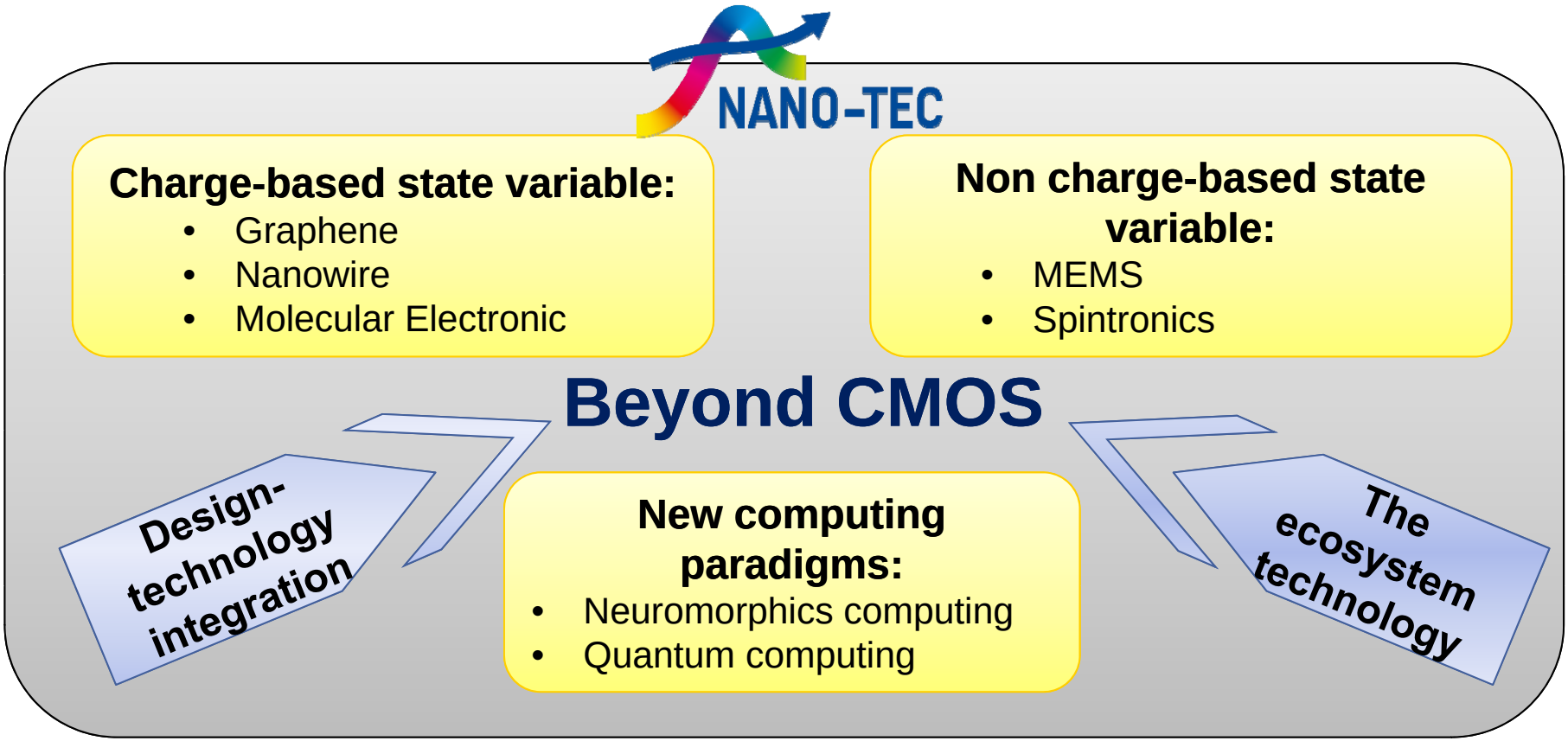
4th Workshop - INPUTS FROM:



4th Workshop: Elaboration of Recommendations

Charge-based State Variable

Rapporteurs:
Guilhem Larrieu (CNRS-LAAS)
Convenior:
Mart Graef (TUDelft) and

INPUTS FROM:

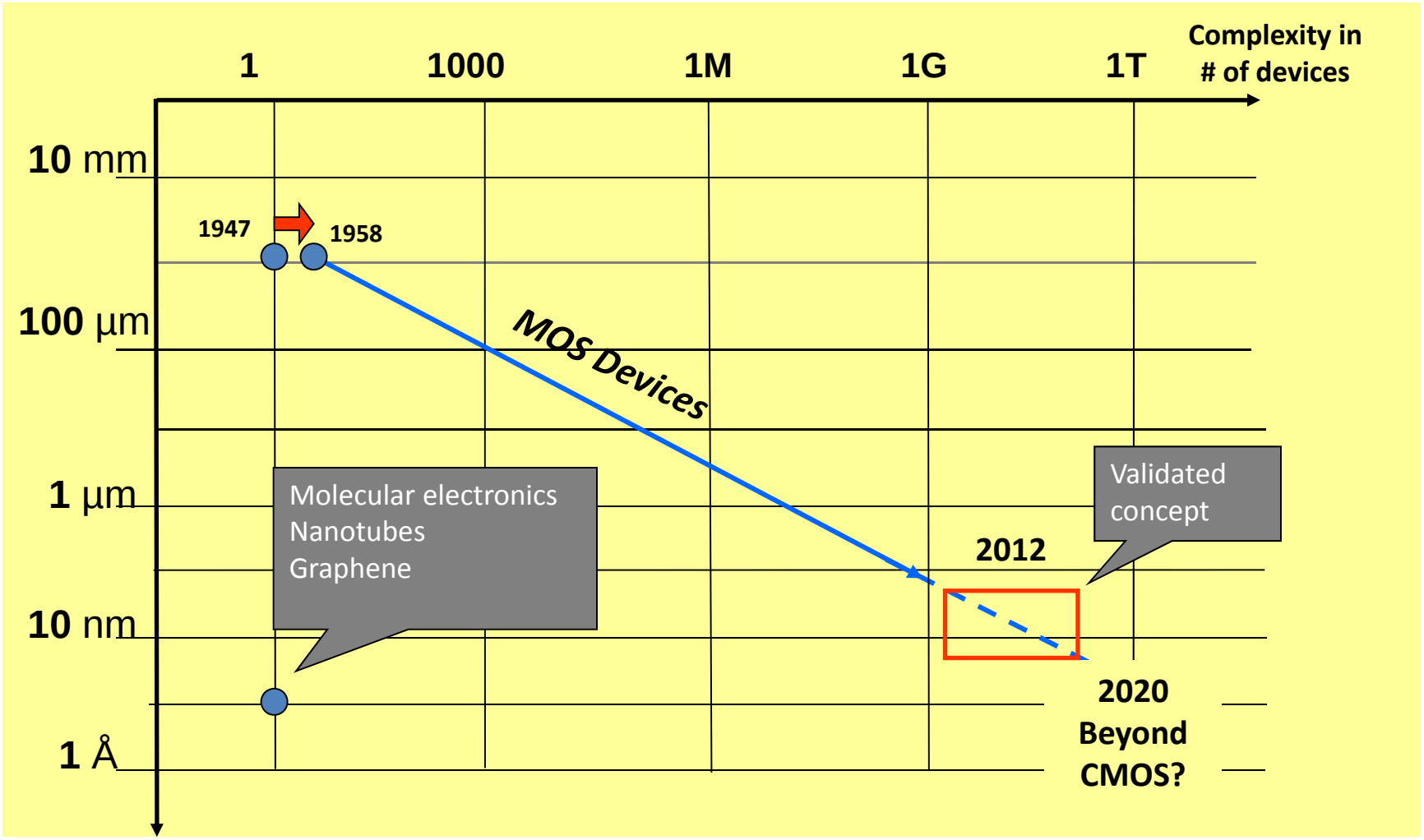
Based on workshop presentations, discussions, working group and rapporteur reports

- **Topic:** Nanowires
  - **WS2 Speaker** Dr. Heike Riel, *IBM Research Zurich*
  - **WS3 Speaker** Dr. Heike Riel, *IBM Research Zurich*

- **Topic:** Graphene
  - **WS1 Speaker** Dr. Jeong-Sun Moon, HRL Laboratories LLC
  - **WS2 Speaker** Dr. Jari Kinaret, *Chalmers Univ Tech*
  - **WS3 Speaker** Dr. Max Lemme, KTH

- **Topic:** Molecular electronics
  - **WS1 Speaker** Prof. Göran Wendin, Chalmers University of Technology
  - **WS2 Speaker** Dr. Dominique Villaume IEMN
  - **WS3 Speaker** Prof. Dr. Sense Jan van der Molen, Leiden University

Reaching dimension/complexity limits



Source: STMicroelectronics

Open Issues

Nanowires

- Physics of nanowires: nanostructures, interfaces
- Process technology aspects: bottom-up vs. top-down
- Modeling & simulation tools

Graphene

- Manufacturability of quality material
- Variability of materials and devices
- Long term stability

Molecular electronics

- Low stability at room temperature
- Low conductance at room temperature
- Low performance compared to Si MOSFET

Design factors

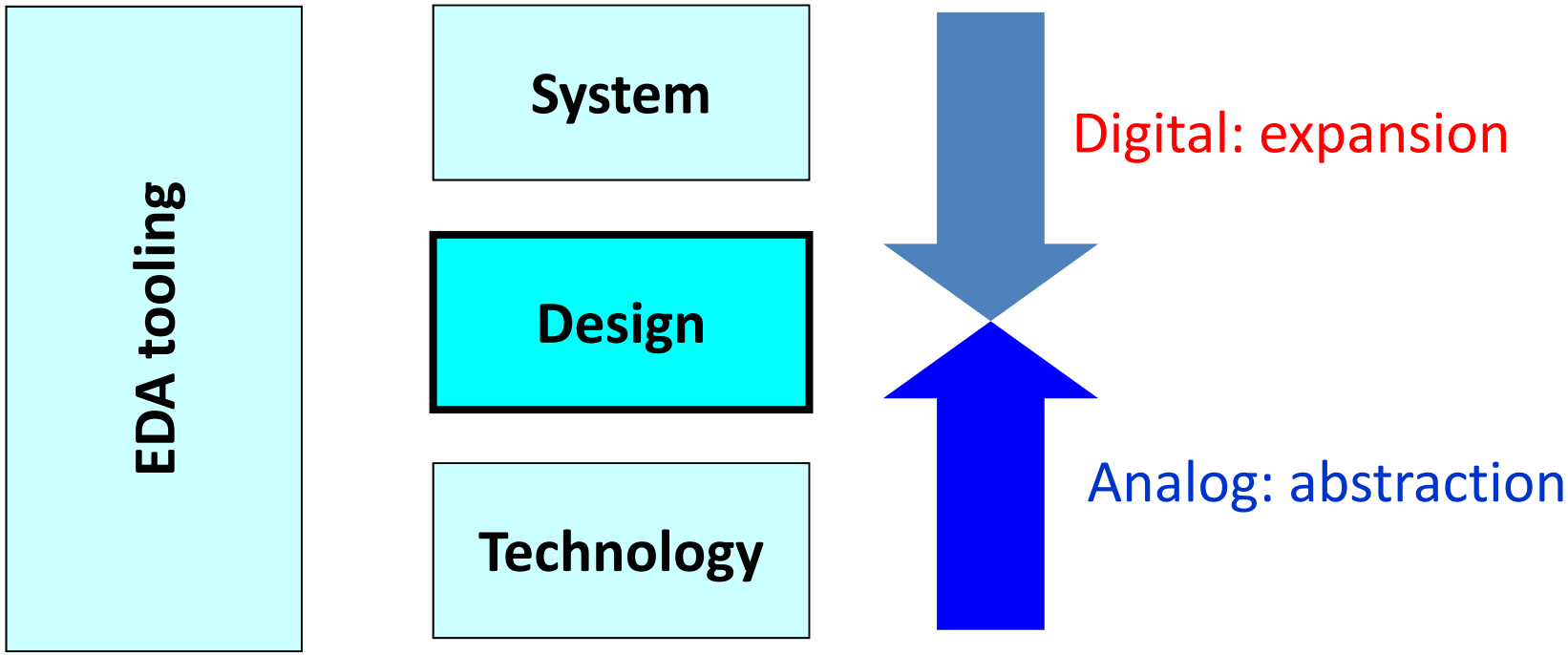
Challenges in design:

Design technologies that enable equivalent scaling (high performance, low power, high reliability, low cost, high design productivity)

- Design for variability
- Low power design (sleep modes, hibernation, clock gating, multi-VDD,...)
- Homogeneous and heterogeneous multicore SoC architectures

Design factors

Design Hierarchy



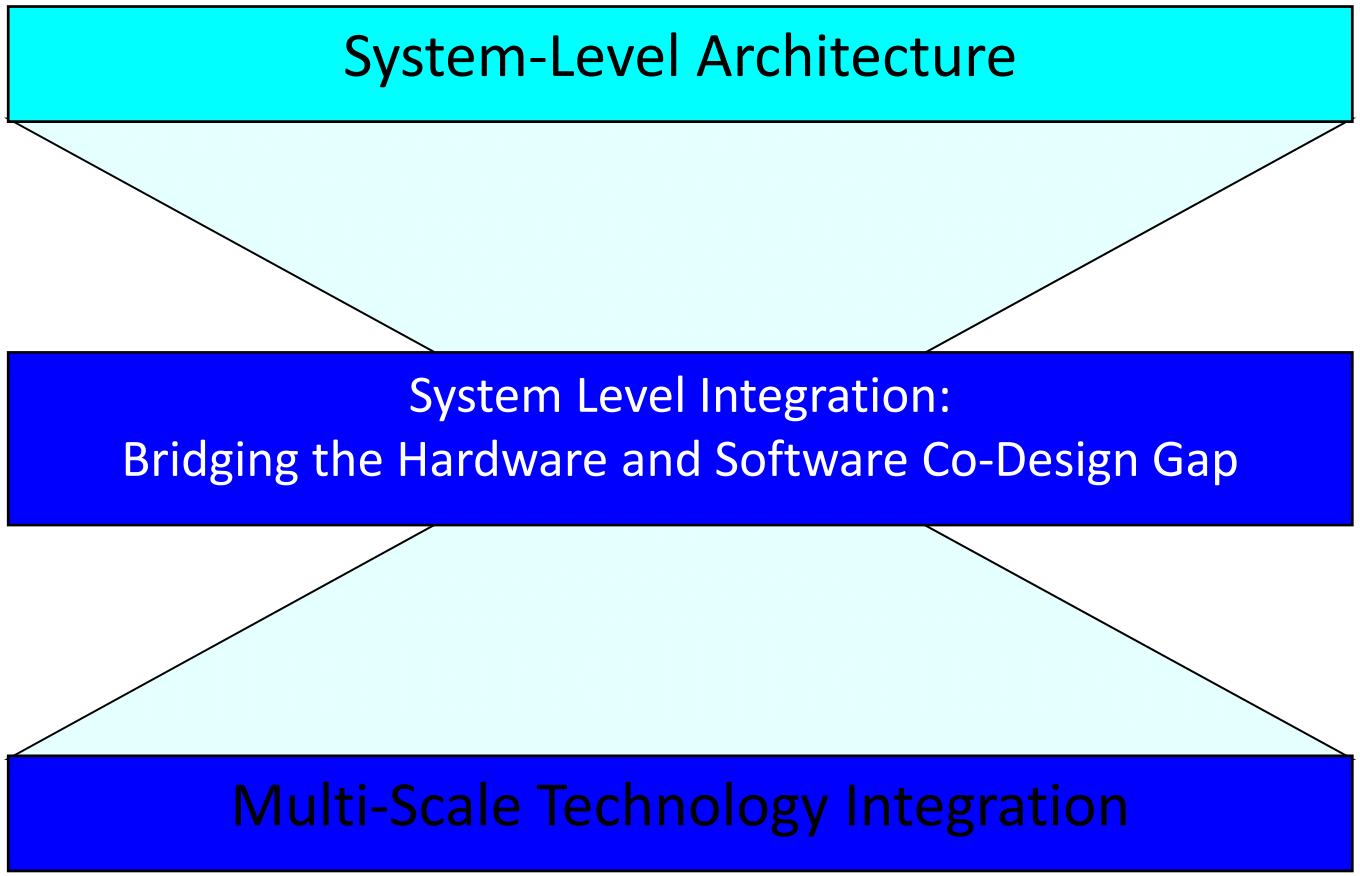
Analog and digital approach design from opposite directions

Mixed-signal: need to “meet in the middle”

Source: Maarten Vertregt, NXP

Design factors

The Co-Design Challenge



Initial Recommendations

Nanowires, graphene, molecular electronics
Pursue programs on:

- Dense circuit integration aspects
- Physical aspects:
  - Electronic structure
  - Carrier transport
  - Variability control
  - Power efficiency
- CMOS compatibility
- Design aspects

- Industrial-academic cooperation

DIscussions:

1. Discussion of several potential cases:

- How to deliver beyond CMOS technologies to designer: Process Design Kit (PDK)
- If graphene based transistor is a reasonable candidate for logic?
  - Need to open the gap -> will reduce the mobility which is the first motivation for graphene.
  - Mobility = high speed is not the 1st requirement for beyond CMOS? The main requirement is to adress the power challenge.
  - Material quality
  - Stability
- 3 issues:
  - Integrability: dense circuit integration.
  - Systemability= design
  - Manusfactability= physical aspect

2. Necessity to have design people close to the development of techno

3. Interconnect possibilities/opportunities should be take into account

WS4 RECOMMENDATIONS

• With respect to nanowires, theoretical understanding of the underlying physics, material science is necessary. The interplay of the physical properties of nanowires (electronic, optical, thermal, mechanical, e.g., strain, interfaces, interface states, surface chemistry, and associated metrology) still require investigation their effect on device operation and on variability, both of which impacting on architectures and integration prospects.

• The combination of nanowires technology with III-V compounds or alternative architecture (TFET) should be regarded as a promising beyond CMOS device, where a particular attention on the CMOS compatibility (for example III-V integration on Si platform) is required.

• Establish a carbon-nanoelectronic program with specific quantitative targets for carbon-based technologies to assess the possibility and test the suitability of fabrication and integration constraints for a combined Si-carbon (graphene) new ICT technology, beyond sensors and single components. Other promising layered materials could be explored as alternatives.

WS4 RECOMMENDATIONS

- With respect to molecular electronics, for information processing of the post CMOS era, more interaction between the design and device communities is required to exploit the full potential of molecules properties. For analog applications, especially sensing, a connection between molecular electronics and flexible electronics may provide new possibilities with a better maturity level.
- Interconnect aspect should be taking into account
- It is essential that strong collaborations are established between the technology and design communities, even during the research stage. Each nanoelectronic project should have a design partner.

4th Workshop: Elaboration of Recommendations

Non-charge-based State Variables

Rapporteurs:
Jouni Ahopelto (VTT) and Piotr Grabiec (ITE)

INPUTS FROM:

Speakers, Discussants, Rapporteurs: Spintronics

Sergio Valenzuela (ICN, Spain), Speaker WS1, Paolo Lugli (TU Munich, Germany) Discussant WS1, Christian Pithan (FZ Jülich, Germany) Rapporteur WS1, Johan Åkerman (U Gothenburg, Sweden) Speaker WS2, Christian Pithan (FZ Jülich, Germany) Discussant WS2, Mart Graef (TU Delft, The Netherlands) Rapporteur WS2, Charles Gould (U Würzburg, Germany) Speaker WS3, Thomas Swahn (Chalmers, Sweden) Discussant WS3, Christian Pithan (FZ Jülich, Germany) Rapporteur WS3

Speakers, Discussants, Rapporteurs: MEMS

Lina Sarro (DIMES, The Netherlands) Speaker WS2, Piotr Grabiec (ITE Warsaw, Poland) Discussant WS2, Danilo de Marchi (POLITO, Italy) Rapporteur WS2, Michael Gaitan (NIST, USA) Speaker WS3, Lars Hedrich (U Frankfurt, Germany) Discussant WS3, Androula Nassiopoulou (NCSR „Democritos" – IMEL, Greece) Rapporteur WS3

WS4 RECOMMENDATIONS

Spintronics Recommendations :

- **Short term, application oriented research:**
  - **RF components:** Increase power output. Demonstration of phase-locking of tens of oscillators needed. Understanding of nonlinearities
  - **Spin Logics:** Material and design developments; improvement of nonlocal devices based on semiconducting and metallic materials. Magnetization switching with pure spin currents. Pure spin currents generation.
  - Spin Transfer Torque (STT) oscillators (STO) offers very interesting perspectives for systematic generation, manipulation and detection of spin waves (magnonics).
  - STT is also able to move domains around – enabling very interesting opportunities for spintronic memristors.

WS4 RECOMMENDATIONS

Spintronics Recommendations :

- **Long term research (more fundamental science based)**
  - **Spin Hall effects and Topological Insulators:** extreme fundamental as well application interest. Focus on materials and device design needed. Spin Hall Effect may generate a pure spin current w/o a charge current which, via STT may generate a spin vawes with very little energy losses.
  - **Spin Thermoelectronics** – Fundamental research needed to understand phenomenology.
  - **Spin Qubits:** Coupling between more than 2 qubits. Limit decoherence from nuclei, molecular spin clusters, quantum control improvement, error correction, Application of new materials.

Issues to be addressed in all above research: interconnects and connecting nanoscale objects, variability, reliability and temperature stability.

WS4 RECOMMENDATIONS

Spintronics Recommendations :

Memories

Already commercial, strong industrial pull for new innovations

Logics

Driving force mmainly academic push, not mature, interesting new physics.

- Advantages for CMOS replacement should be identified. Spintronics offers reduced power dissipation and to large extent could re-use most of existing design architecture, it is also a good candidate to implement a 4-level logic, however a critical fundamental and technology related viabilities have to be clarified:
  - pure spin propagation in wires, without charge propagation
  - spin injectors and spin-sensing transistors (CMOS transistor size)
  - other spintronic architectures? Other carriers - Phonons should also be considered.
- Design investigation for multi-level logic can be studied independently from spintronic feasibility

WS4 RECOMMENDATIONS

MEMS/NEMS Recommendations:

- **MEMS/NEMS** have to be considered more as functionality enablers than as technology for information processing. Nanoelectromechanical devices are expected to be suitable building blocks for creating RF components (oscillators, antennas, interconnects) offering better perfonmance operation, (low RF losses, non-linear operation, opto-mechanical actuation, combination with phonon engineering, etc)

- **Towards Beyond CMOS (MEMS/NEMS switches):** Switches with stable, high performance are necessary for relay-based ICs. The on-state contact resistance should be as low as possible with reliability exceeding 10^{14} on/off cycles.

- An interesting NEMS approach is **conformal changes** of organic molecules. It has been shown that the conductance of small molecules can be swithced by a factor of 1000 by light pulses which drive the molecule to change its shape. The conformal change is reversible and provides a very small NEMS switch.

WS4 RECOMMENDATIONS

MEMS/NEMS recommendations:

- The MEMS/NEMS switches cannot replace CMOS for high density computing, however they can replace CMOS in some interesting and important niche applications e.g. operation in noisy (electromagnetic) enviroment or to simplify technology when logic operations have to be integrated with resonators for RF or sensor applications.
- MEMS/NEMS can introduce additional functionalities on top of CMOS platform.
- New applications using phonons and phonon confinement in nanostructures (e.g. porous Si) are currently investigated with prospective applications including on-chip cooling and thermal devices.

WS4 RECOMMENDATIONS

Technologies not discussed in the Workshop series:

- **Quantum cellular automata (QCA)**: Provides a straightforward method to realise logical functions. Implementation has proven to be difficult, if not impossible. Realisation of single QCA units have been demonstrated at low temperature. Magnetic QCA more promising and simple logic circuits have been demonstrated at room temperature.

- **Thermal computing** is a relatively new approach for non-charge based data processing. Thermal diodes and first three terminal thermal transistors have been demonstrated. More challenging but maybe more promising is the approach in which the phase and polarisation of phonons are used in realisation of logic devices. Thermal computing represents rather long term paradigm, though.

4th Workshop: Elaboration of Recommendations

Technology and Design of new computing paradigms

Rapporteurs:

G Fagas (Tyndall), C M Sotomayor Torres (ICN), G Wendin (Chalmers) and D Winkler (Chalmers)

INPUTS FROM:

Discussant: Göran Wendin (Chalmers)

Rapporteur: Giorgos Fagas (Tyndall)

Attendees: Victor Zhirnov (SRC)
Simon Thorpe (CNRS-Université Toulouse 3)
Sandip Tiwari (Cornell)
Mustafa Badaroglu (imec)
Alain Cappy (CNRS-LAAS)
Paolo Lugli (TU München)
Helena Theander (Chalmers)

WS4 RECOMMENDATIONS

- **Transversal coherent research project (super "IP")** aiming at integration of unconventional computing paradigms (e.g., quantum information processing, neuromorphic information processing, chemical/molecular information processing) with digital environments via digital-analogue hardware and software interfaces, in order to create useful hybrid systems.

  - Do not get locked on specific devices from the start. Analyze, benchmark and develop application areas where solutions to computationally hard problems may be possible.
  - Bridge the gap theory-design-systems-applications.
  Develop embedded-systems approaches for promising hardware components and circuits

WS4 RECOMMENDATIONS

- **Research areas should focus on mathematical problems and/or applications that unconventional computing can solve or give an answer more efficiently** (see beating a chess masters with less resources than Deep Blue)
  For example, image recognition (characterised by complexity of image, time and energy required for it), data-mining of complex big data (combinatorial efficiency of quantum computing or associative learning of neuromorphic computing), finding repeated patterns in sequence of events (e.g., in monitoring internet activity), creating meaningful outputs from input sequences

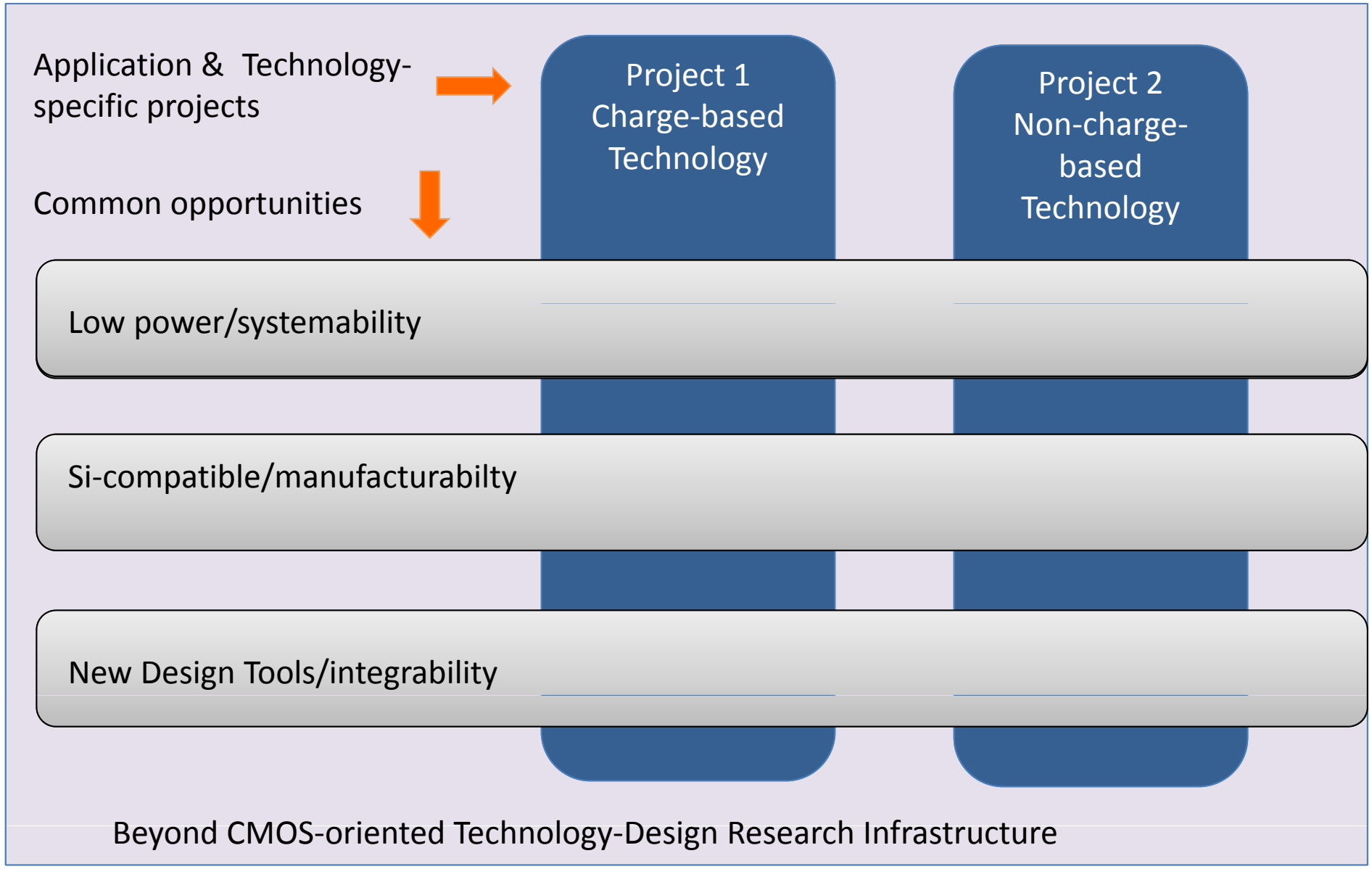
- Research topics should focus on hardware (e.g., solid-state qubits, memristive components) and software enablers for unconventional computing, aiming at integrated solutions and addressing adaptive learning by a system in relation to interaction with human users

A BOLD SUGGESTION (1/2)

An “experiment”:

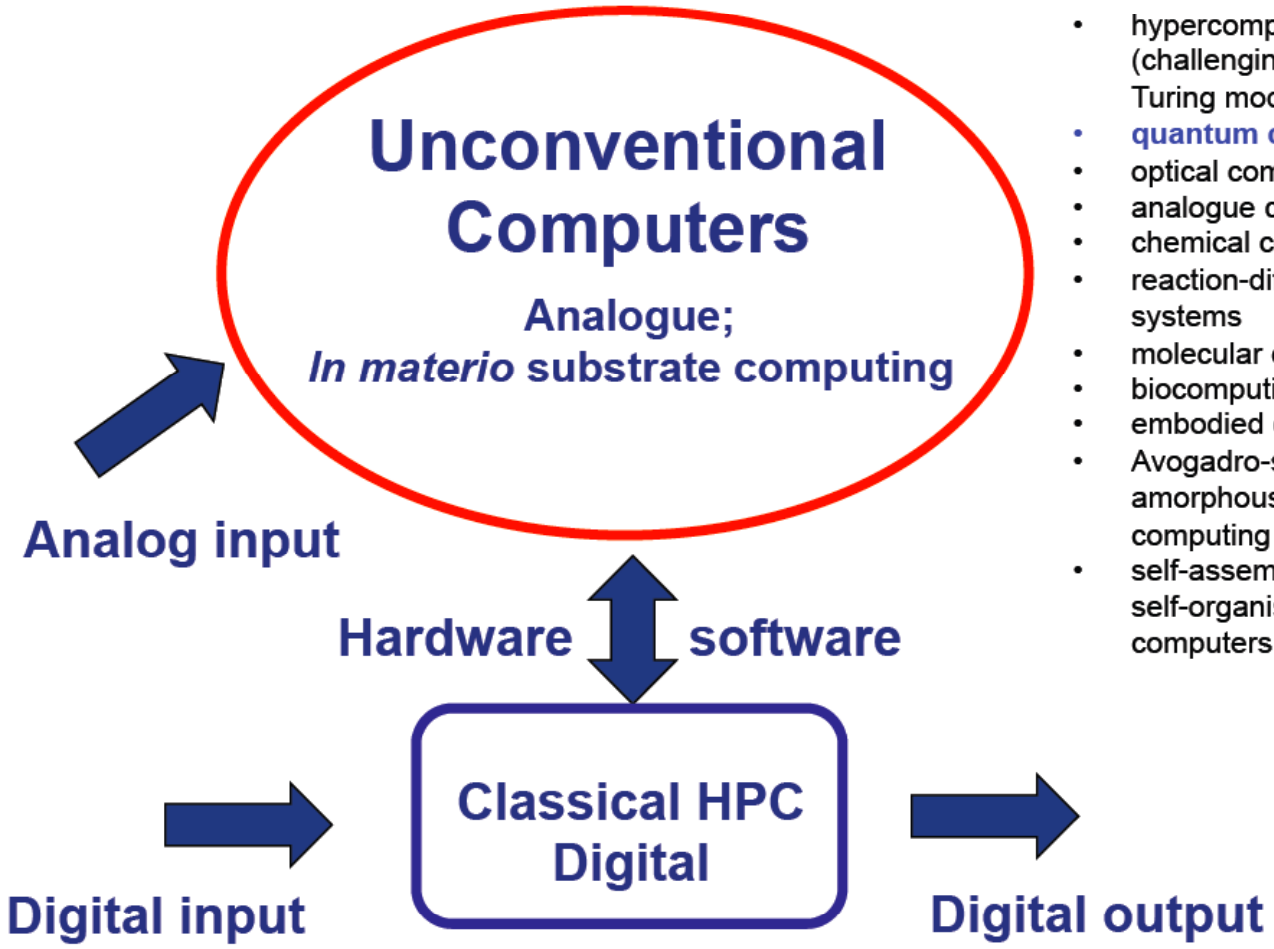
- Develop methods to ensure the technology gap is bridged
- Cluster two pilot Integrated Projects project in Beyond CMOS technology-design
- One on charge-based and one on non-charge. They will be at different stages in the TRL.
- These should be ideally supported by a pilot distributed technology-design research infrastructure
- Facilitate a super IP on Unconventional Computing Paradigms:
    - Super-IP or collection of IPs
    - 10-20 MEuro/year and 5 + 5 years
    - Clear Objectives and work plan
    - Concrete milestones
    - But adaptive and reconfigurable

A BOLD SUGGESTION (2/3)



Beyond CMOS-oriented Technology-Design Research Infrastructure

A BOLD SUGGESTION (3/3)



- hypercomputation (challenging the Turing model)
- quantum computing
- optical computing
- analogue computing
- chemical computing
- reaction-diffusion systems
- molecular computing
- biocomputing,
- embodied computing
- Avogadro-scale and amorphous computing
- self-assembling and self-organising computers

A dedicated European large-scale program/project on high-performance computing unifying digital and unconventional paradigms.

Not a Flagship – a fleet, a strike force.

4th Workshop: Elaboration of Recommendations

The ecosystem technology in beyond CMOS in Europe

Rapporteurs:

Alain Cappy (CNRS) and Thomas Swahn (Chalmers)

WHICH ECOSYSTEM ?

Our scope: “Beyond CMOS”

Information processing, memory, **communications**

Our input comes from:

<u>all beyond-CMOS conclusions from NANO-TEC</u>

+ known activities in Europe

+ electronics survey

+ the NANO-TEC projects recommendations for the future

CONTEXT

- A critical issue in beyond CMOS research is the availability of advanced technology.
- The ecosystem technology has many players
- A clear definition of the roles of the respective players is needed in order to avoid non-constructive competition and waste of resources

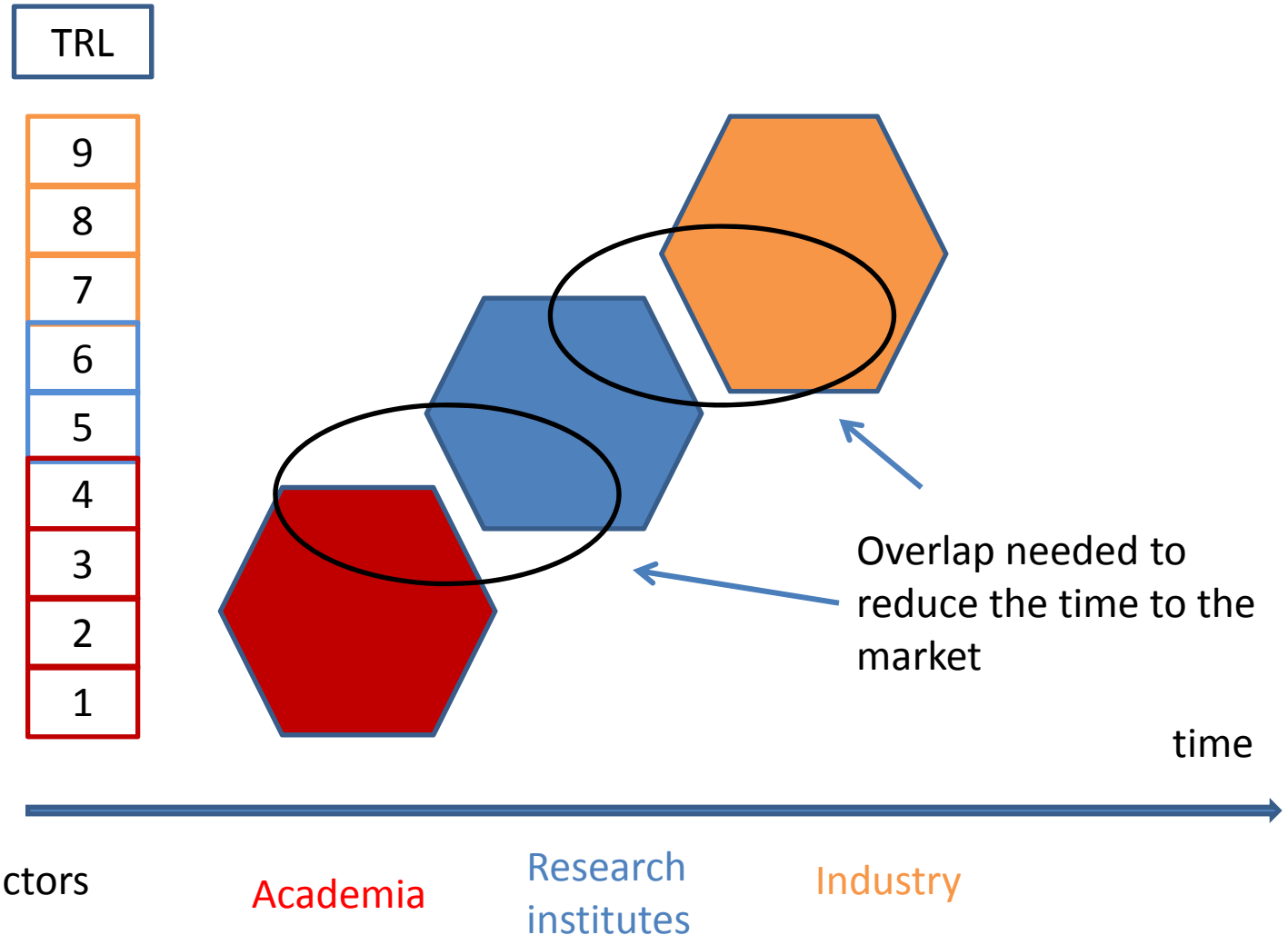
CONTEXT

The ecosystem technology has three main players with different access status

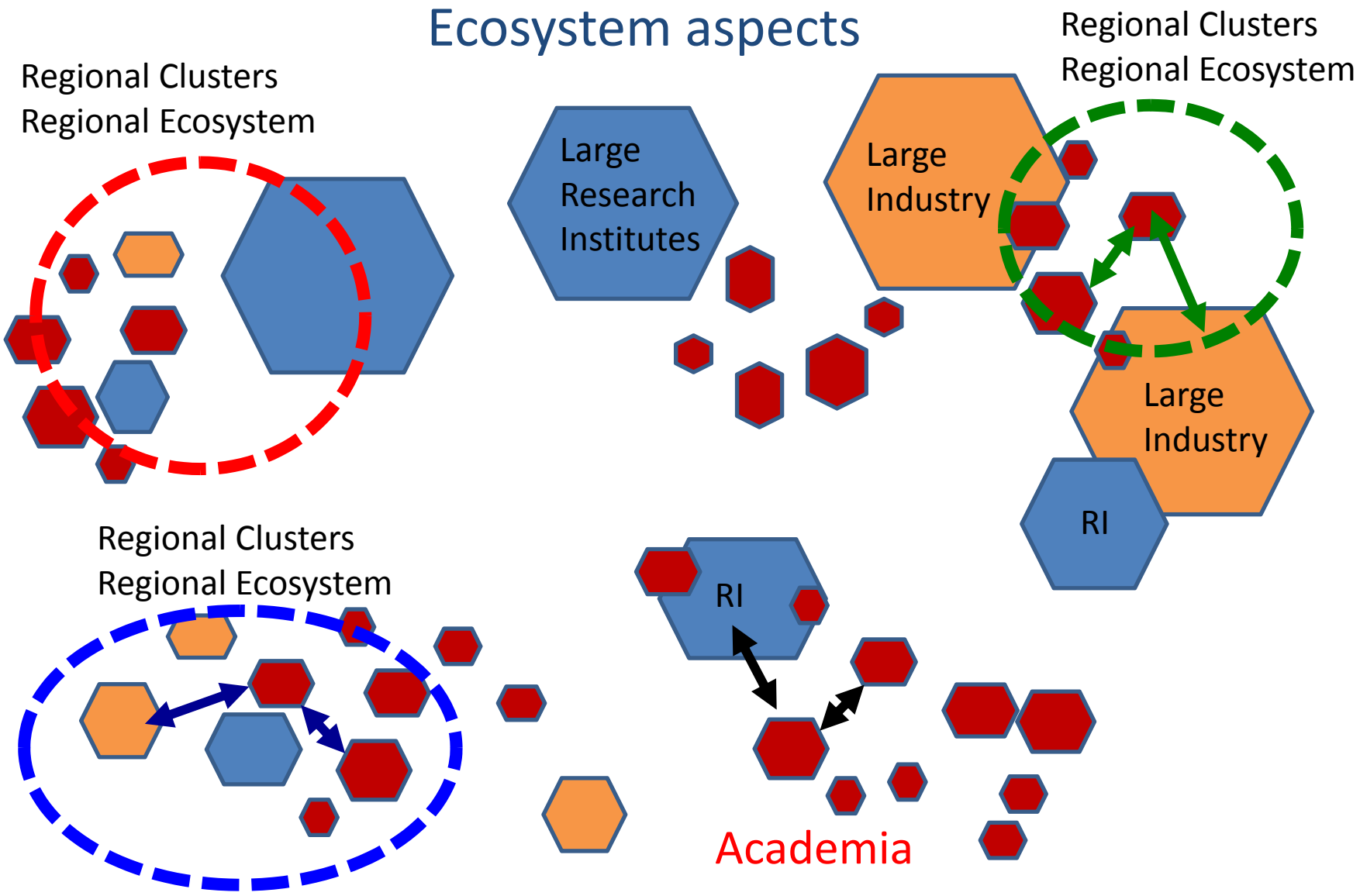
- **Academia** (with an R&D horizon > 6 years, TRL 1-4) – *basic understanding, test and validation of innovative architectures, materials and processes for future ICT.*
- **Research Institutes** (RTOs, Integration Centres with R&D horizon 3–6 years, TRL 3-7) – *Technology implementation and the assessment towards Production Equipment; development of high performance components.*
- **Industry** (with R&D horizon < 3 years, TRL 6-9) – *Technology research, innovation and exploitation; Process introduction and continuous improvement with innovative approaches (yield, reliability,…).*

CONTEXT

TRL metrics



CONTEXT


Ecosystem aspects
Regional Clusters
Regional Ecosystem
Large
Research
Institutes
Large
Industry
Regional Clusters
Regional Ecosystem
Large
Industry
RI
Regional Clusters
Regional Ecosystem
RI
Academia

BEYOND CMOS TECHNOLOGY ECOSYSTEM

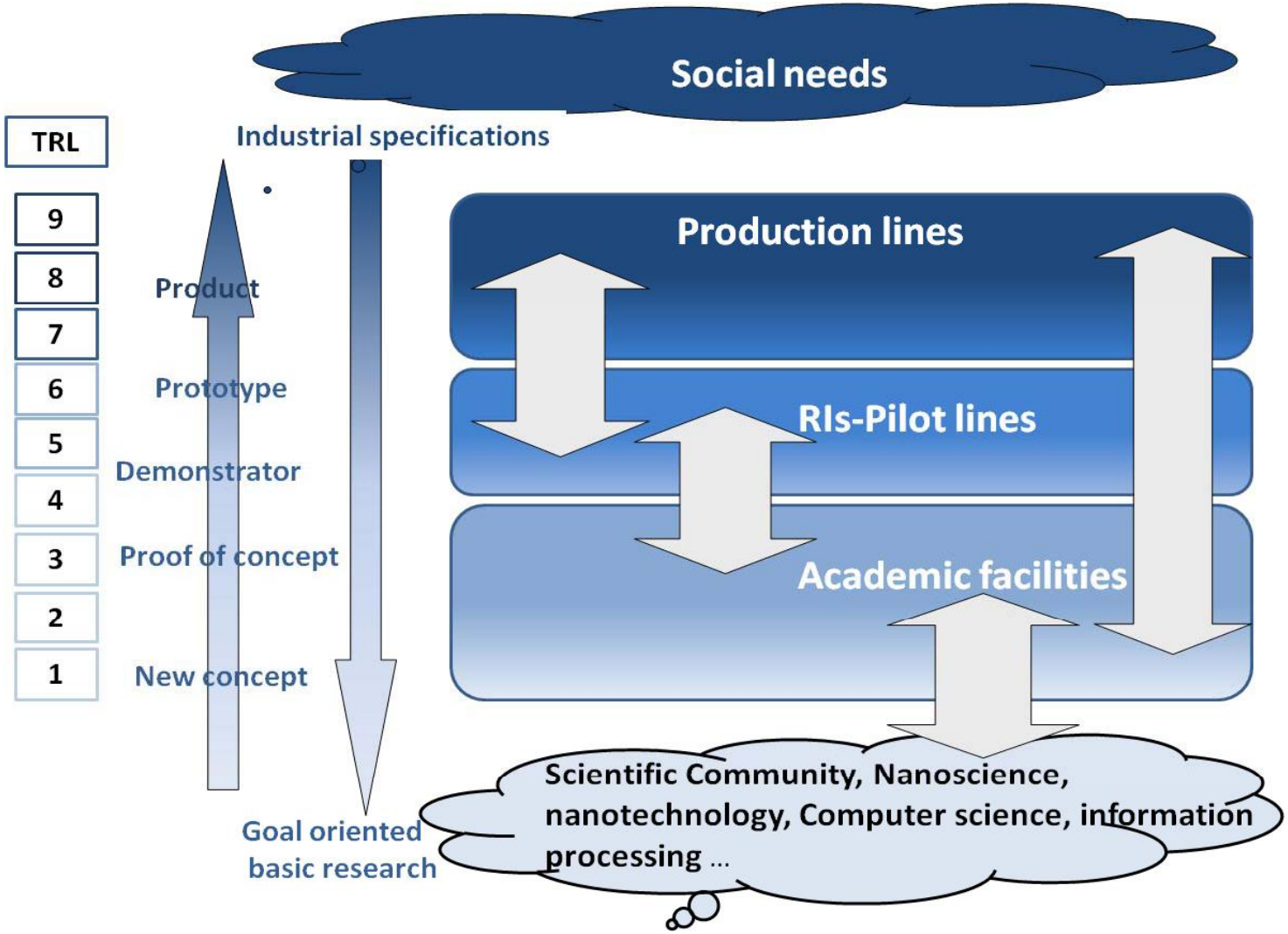
Beyond CMOS address medium/long term technologies: the main players are academia and large research institutes. BUT the active role of Industry is mandatory:

- to contribute to the identification of relevant long-term fundamental research topics needed in the value chain,

- to define expectations for ultimate CMOS technology, applications, and services (> 2015),

- to provide critical feedback to research institutes and academia.

BEYOND CMOS TECHNOLOGY ECOSYSTEM



BEYOND CMOS DEVICE TECHNOLOGIES?

- Using the three device categories chosen for workshop 4, we can describe a little bit the technology state of the art and the needs to push the technology forward.

- Digital with charge as state variable (New semiconductor transistor (TFET,i-MOS, III-V, nanowire…but also nanomechanical switch). Generally , the demonstration is carried out for a single device or low complexity circuits. To demonstrate better performance than CMOS (at least for one or two parameters), manufacturability is a key question. So the main difficulty is the access to large scale infrastructures (LSI) at reasonable cost. Design is not a problem if the new device can simply replace CMOS

BEYOND CMOS DEVICE TECHNOLOGIES?

- Digital with state variable other than charge (Spin, molecular state….) For this domain, the objective is mainly to demonstrate the possibility to use of a new two state device to make digital circuits. Manufacturability on a semiconductor process line is a key question.

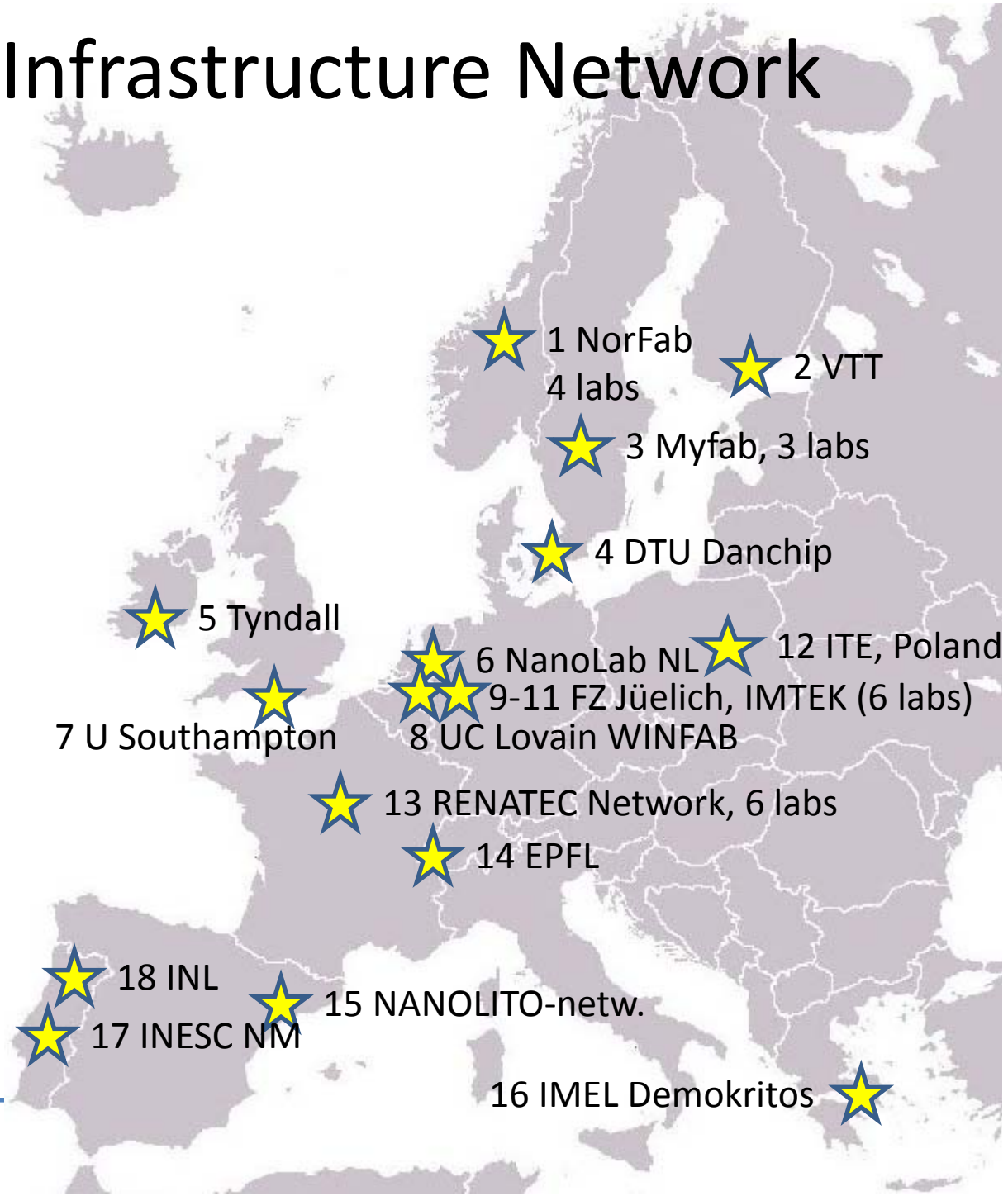
- Non digital (quantum, neuromorphic). For this domain, the notion of device is not relevant. Completely new technology (self assembly ….) can be proposed for which the technology ecosystem is not clear.

Bottom-up infrastructure networking and mapping

- A grass-root mapping approach to European infrastructures >≈ 500 m^2
- to connect small ecosystems (typically small RI, regional networks) to large institutes and industry
- Bottom-up and open access approach: several coordinated proposals submitted (Myfab, NorFab, RENATECH, TRAIN^2-network etc.) to the EU-open consultation (22 October).
- Not the complete picture – but the NANO-TEC map of our extended infrastructure network (inclusive approach)
- Additional input to the final report wanted!

European Infrastructure Network

1 NorFab, Norway, (4 labs)
2 Finland, VTT, Finland
3 Myfab, Sweden (3 labs)
4 Danchip, Denmark
5 Tyndall, Ireland
6 NanoLabNL, Holland
7 Twente, The Netherlands
8 U. Southampton, England
9 UC Lovain, Belgium
10 FZ Jüelich, Germany
11 IMTEK/HSG-IMIT Germany
12 ITE, Poland
13 RENATEC, France (6 labs)
14 EPFL, Switzerland
15 NANOLOTO, Spain (x labs)
16 IMEL Demokritos, Greece
17 INESC NM, Portugal
18 INL, Portugal



NANO-TEC

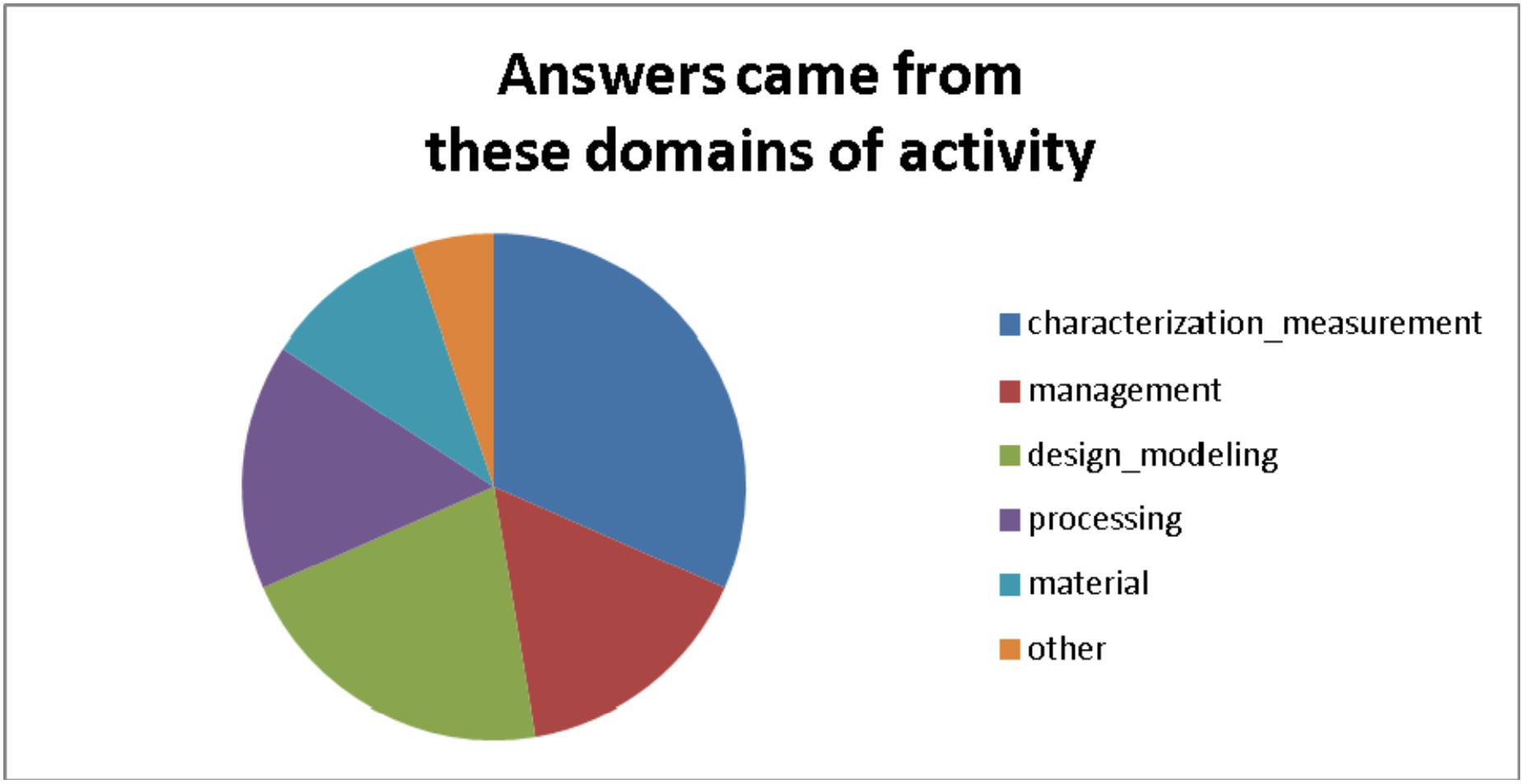
HOW TO IMPROVE THE BEYOND CMOS TECHNOLOGY ECOSYSTEM ?

What is the opinions of the players?

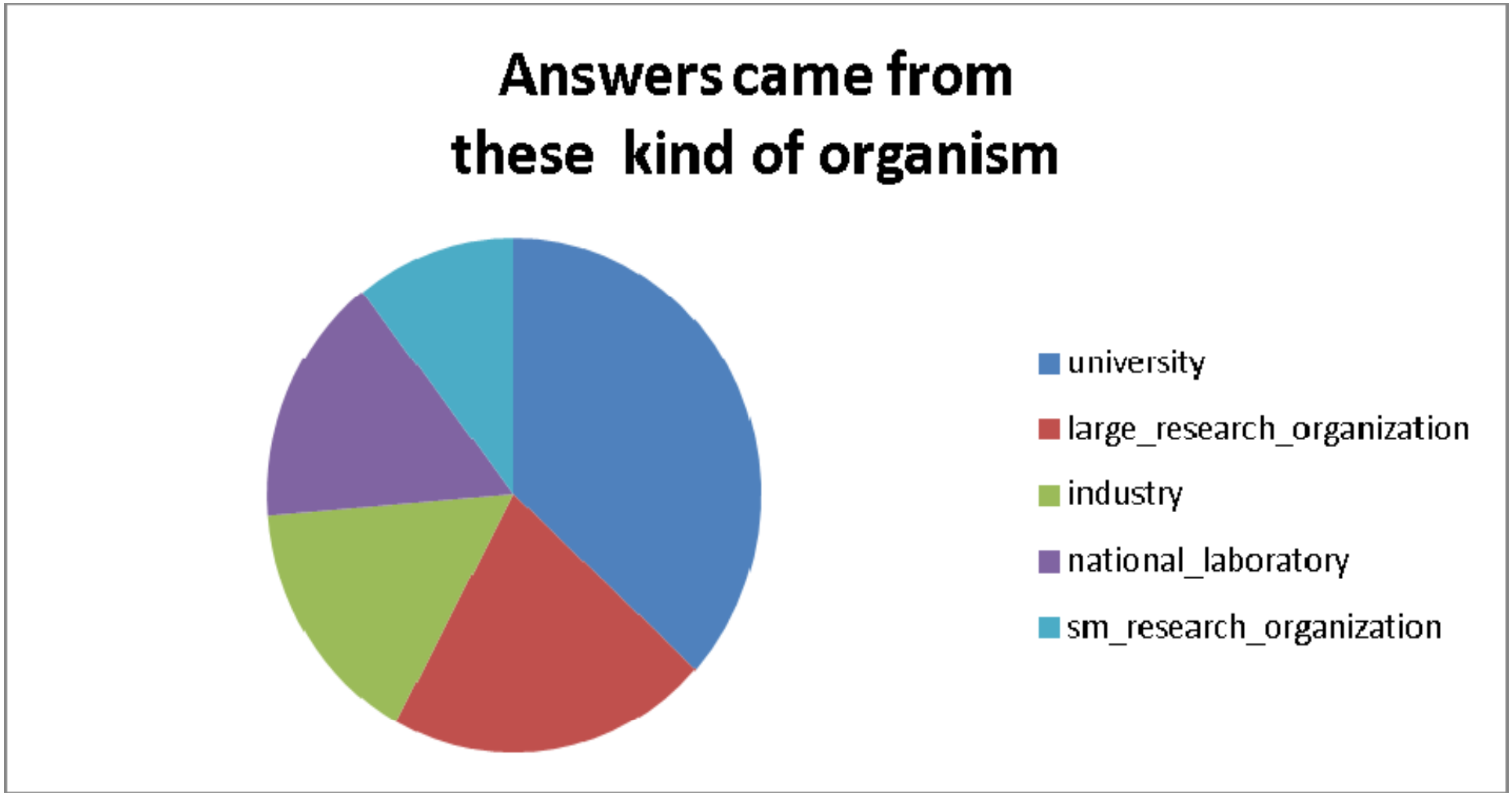
The NANOTEC electronic poll:

- Posted in the NANO-TEC website July – August 2012
- Invitations sent to experts within the extended NANO-TEC network
- 19 replies registered

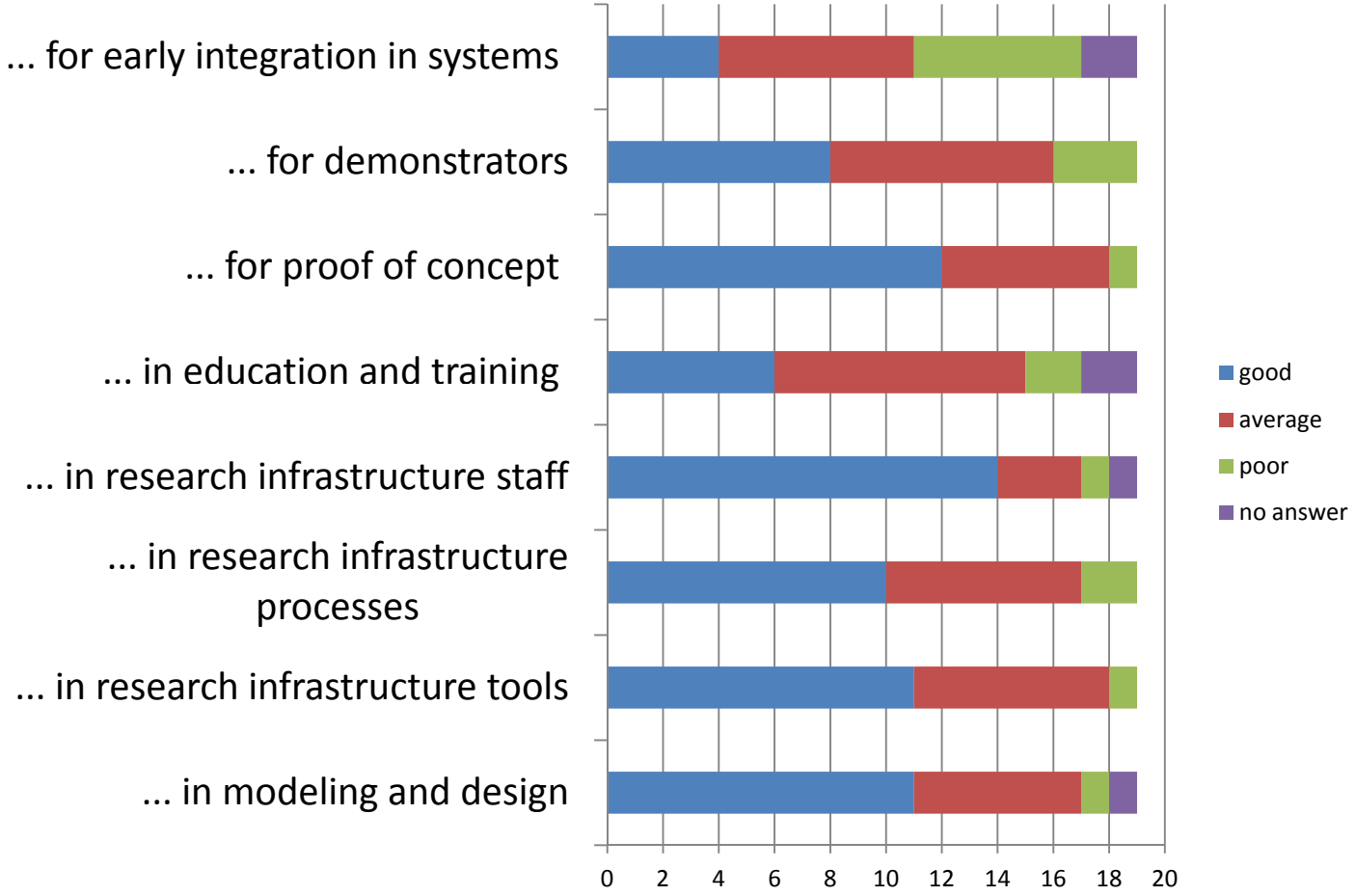
3. STATUS OF THE RESPONDENT?



3. STATUS OF THE RESPONDENT?

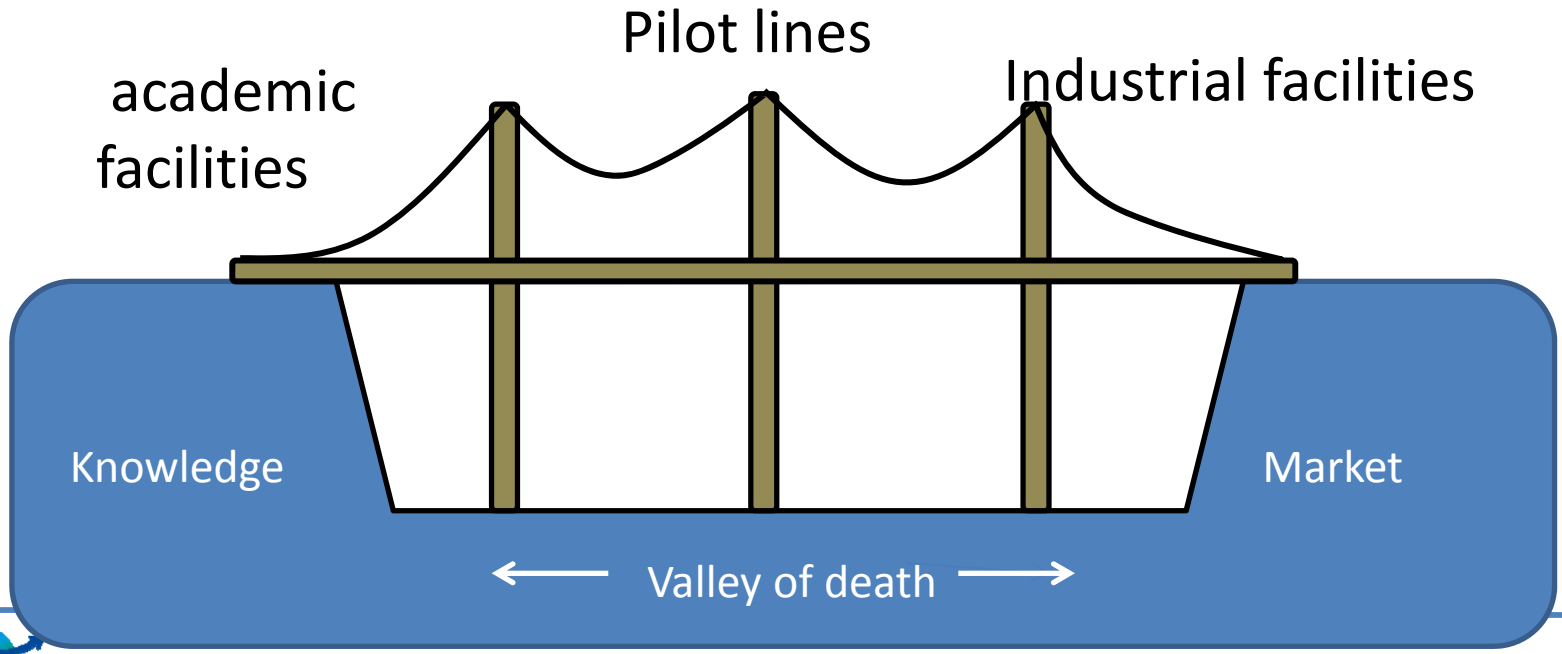


Opinion on the general ”beyond CMOS” European capabilities …



HOW TO IMPROVE THE BEYOND CMOS TECHNOLOGY ECOSYSTEM ?

- European research is strong in beyond CMOS technologies, but the transition from ideas arising from basic research to competitive product is a weak link in European nanoelectronics value chains
- The gap between basic knowledge generation and the subsequent commercialisation of this knowledge in marketable products is known as the "valley of death" issue.



HOW TO IMPROVE THE BEYOND CMOS TECHNOLOGY ECOSYSTEM ?

Make a better connection between the three pillars

The first pillar, "academic facilities" consists of taking best advantage of European scientific excellence in transforming the ideas arising from fundamental research into technologies competitive at world level. Proofs of concept and patents

The second pillar, "Pilot lines" consists of putting in place pilot lines having technology prototyping facilities to enable the fabrication of innovative prototypes.

The third pillar, "Industrial facilities" starting from product prototypes duly validated during the demonstration phase to create and maintain in Europe attractive economic

HOW TO IMPROVE THE BEYOND CMOS TECHNOLOGY ECOSYSTEM ?

- Many structures already exist (CATRENE, prins, ENIAC, AENAS, SINANO, ENI2, Silicon Europe, …) gathering the same communities.

DO NOT create a new one

- How to improve the ecosystem without increased complexity ??

WS4 RECOMMENDATIONS

The first recommendation:

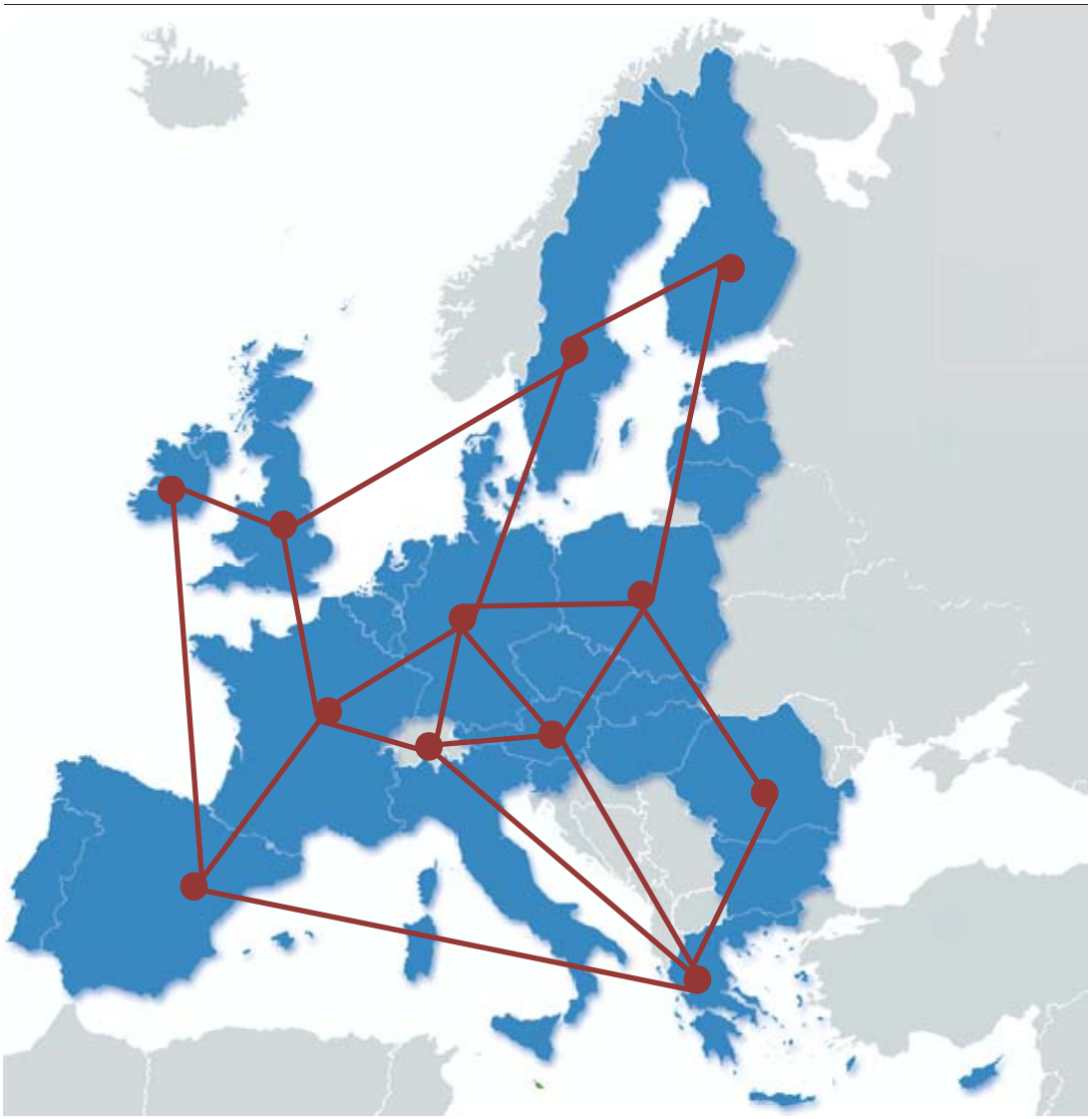
Academic networking

- We propose that Europe organize all the advanced academic technological facilities having a significant activity in beyond CMOS research in a European network with one and only one entry point in each country, each entry point having mission to represent/structure its national facilities

Do not make the picture more complicated!

- In order to avoid a new structure, it should be useful that this network could be managed by an existing initiative. This network will be complementary to the facilities of the RTO and tightly link to them in order to allow a smooth crossing of the 'valley of death'.

WS4 RECOMMENDATIONS



Academic facility
European network

WS4 RECOMMENDATIONS

The second recommendation:

Beyond CMOS education

We propose that Europe should create a multidisciplinary 'Beyond CMOS ' Erasmus Mundus programme to educate a new generation of student to future information processing concepts: theory of information, binary and non binary information processing, quantum computing, neuromophic computing.

Feedback from Industry

The low level of feedback from industry is also a weakness in Europe. It is recommended that industry will define more clearly the expectations for ultimate current technology, future needs and roadmaps of long-term research. This feedback would increase the manpower on research on subjects that are considered as strategic by industry for the long term and avoid dispersion on subjects of minor importance.

Workshop 4

Summary and Recommendations on the Technology-Design Ecosystem for Nanoelectronics

Panel Discussion:

Design Tools for Beyond CMOS technologies

CONTRIBUTORS

Panelists:

- Prof. Dr. Wolfgang Rosenstiel, edacentrum and University of Tübingen;
- Prof. Dr. Paolo Lugli, Technical University of Munich;
- Prof. Mustafa Badaroglu, imec;
- Prof. Dr. Sandip Tiwari, Cornell University, Ithaca, N.Y.

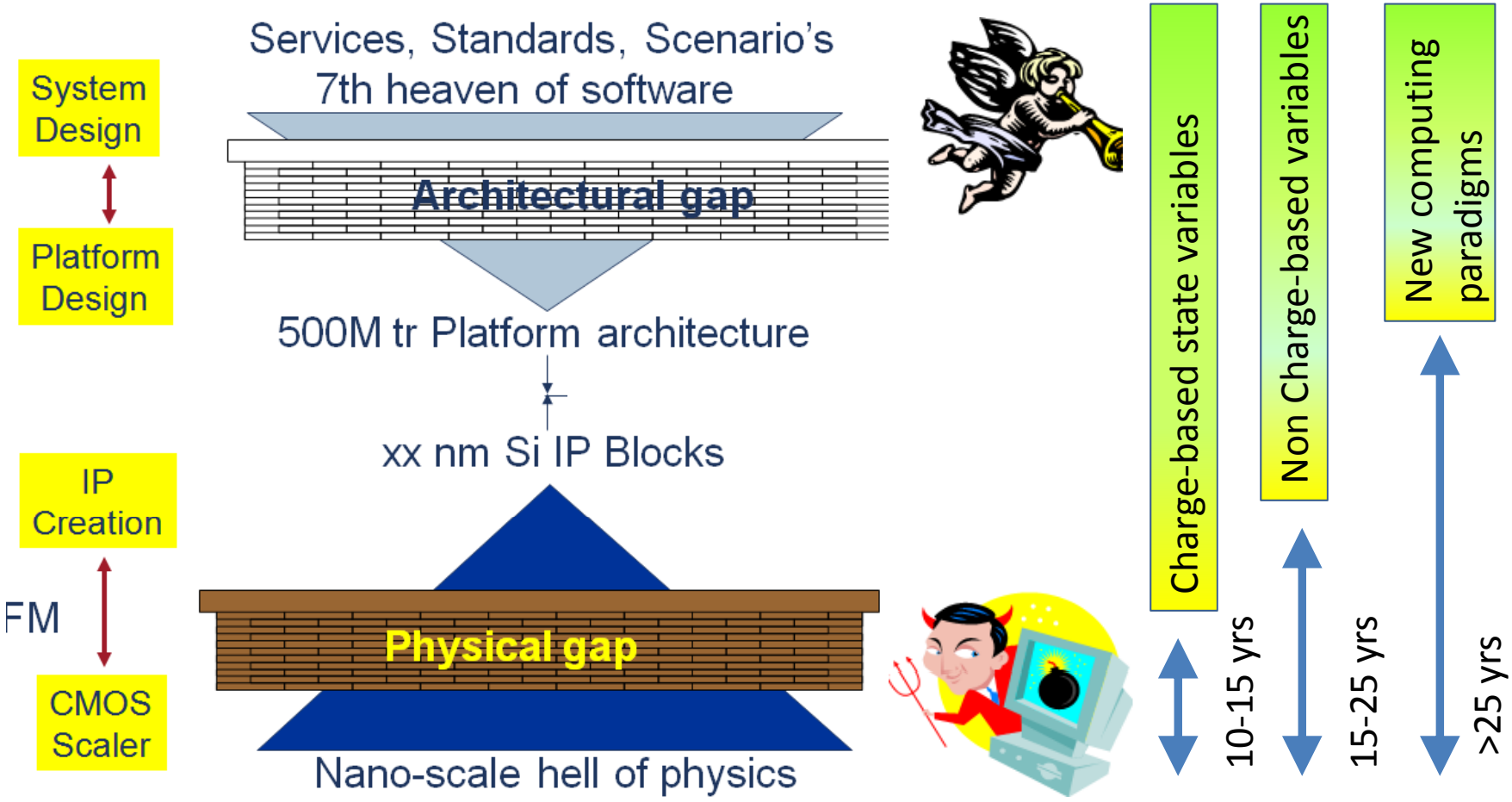
Chair:

- Dr. Livio Baldi, Micron Semiconductors Italia, Agrate Brianza

SETTING THE STAGE

- Non CMOS technologies can complement CMOS in several applications (nice to have).
- Must have is More Moore continuation beyond CMOS scaling limits (must have) for logic or memories.
- But Moore's Law is **NOT** about transistor size but about device complexity.
- Are we sure that CMOS size is the critical parameter?
  - In logic technology half-pitch is usually much larger than transistor length
  - A sizable percentage of transistors is there just for signal buffering.

WHAT CAN BE SAVED?



KEY QUESTIONS

- Are design tools the main bottleneck for Beyond CMOS?
- Can a new technology solve the limitations of current tools?
- If new tools/architectures become available, will we really need a new technology?
- What can trigger the investment needed for new technology/tools?

Panel Session
Design Tools for 'Beyond CMOS' Technologies

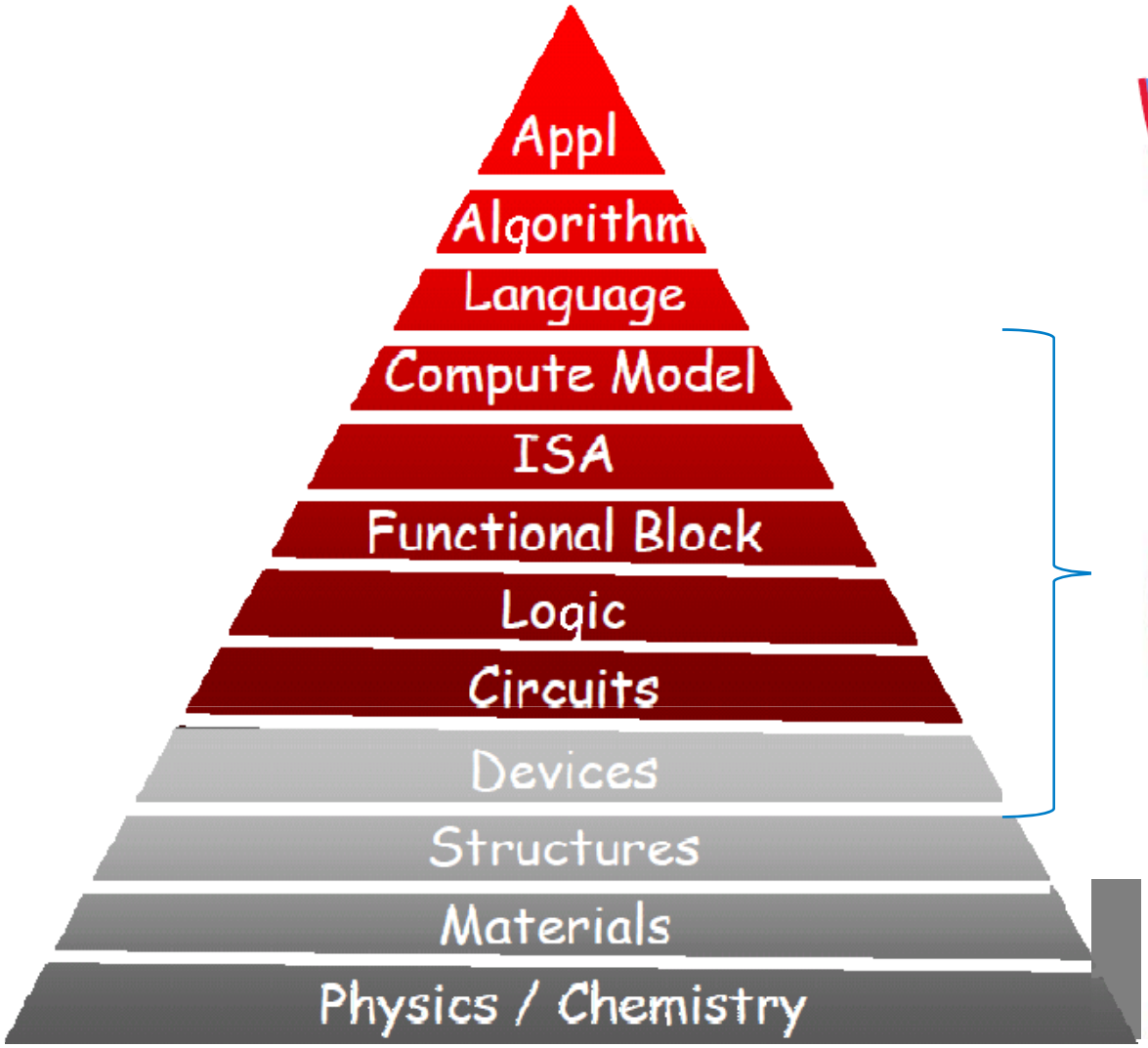
Statement

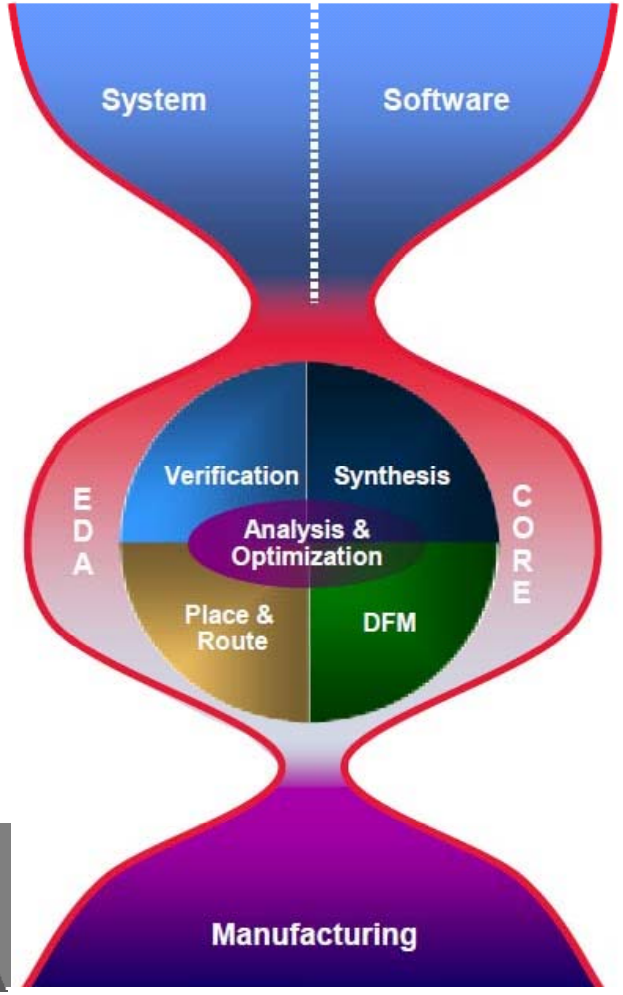
Wolfgang Rosenstiel

U Tübingen, edacentrum

Editor's note: these are selected slides-full presentation in project web site.

Design Tools Exist Mainly for CMOS





Today's design facilities in ‚Beyond CMOS'

(i) A variety of nanodevices can be reliably fabricated using various materials, technologies and processes.

(ii) Several open questions still exist concerning the mode of operation of such devices.

(iii) Modeling and simulation is necessary for better understanding of these devices.

(iv) A multi-scale approach is needed in order to describe real systems.

(v) Novel circuits, architectures and design methodologies are needed for a full exploitation of nanodevices.

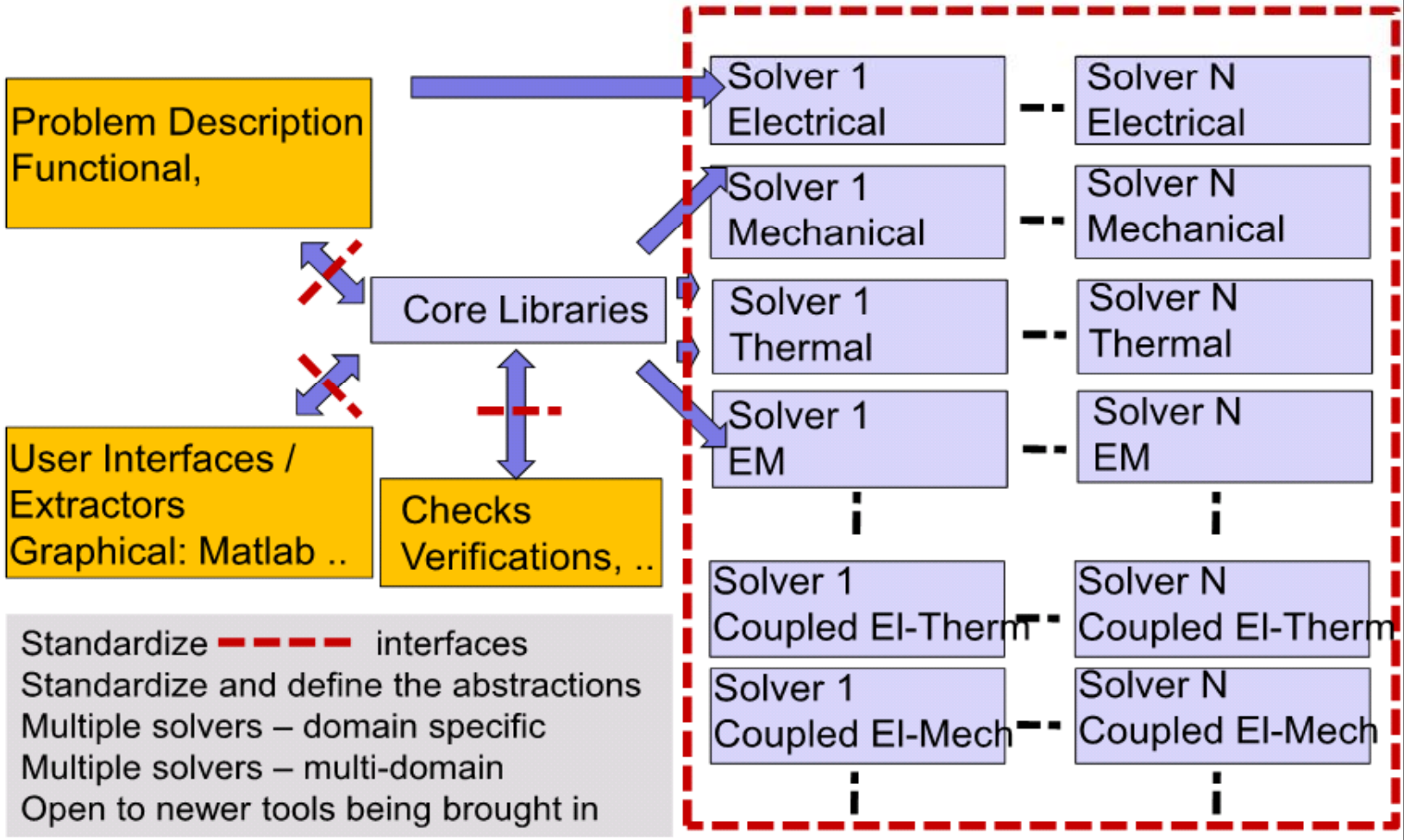
(vi) Education is far away from teaching a new generation of designers who know about nanodevices and related technology.

… But not many tools for Beyond CMOS…

A POSSIBLE TECHNOLOGY & DESIGN INFRASTRUCTURE

Build A New Open Infrastructure

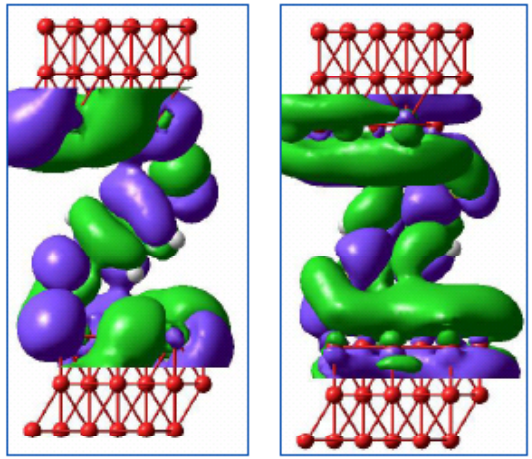
S Tiwari



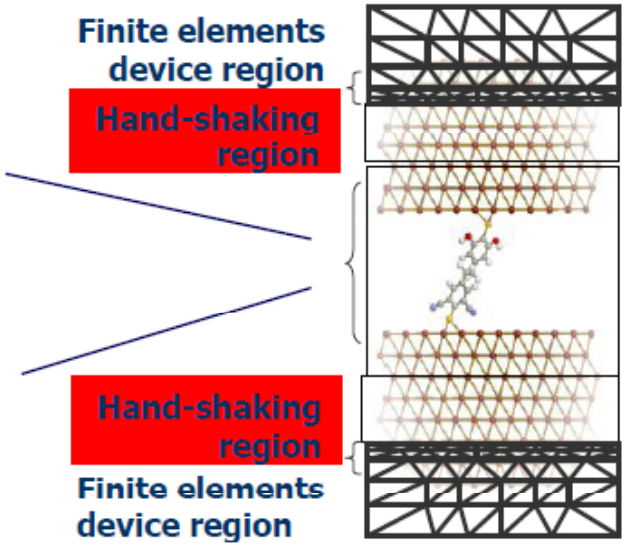
Standardize - - - - interfaces
Standardize and define the abstractions
Multiple solvers – domain specific
Multiple solvers – multi-domain
Open to newer tools being brought in

Multiscale modeling

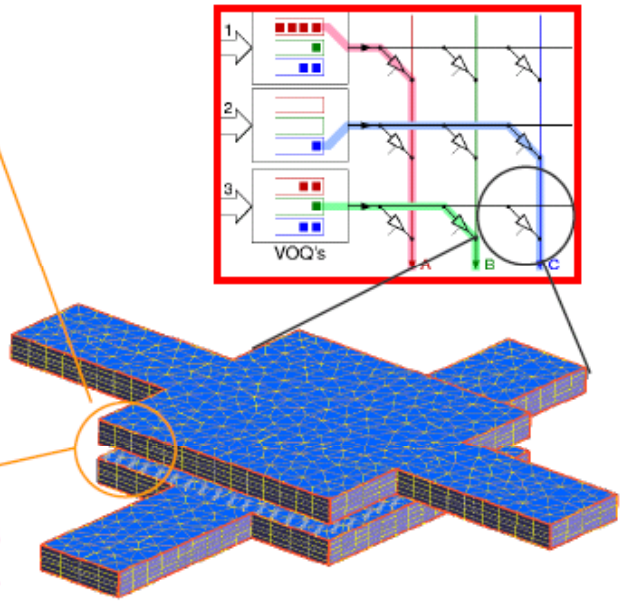
Paolo Lugli



DFTB + quantum-transport approaches using Non-equlibrium Green Functions.



Well-established drift diffusion simulator codes are used to simulate contacts and devices surrounding the molecules.



Circuit level

nanometer region | submicron to micron region | Micron to millimeter regions

Ab initio models | **Quantum-classical interfaces** | **Continuum-based and circuit models**

Physics ⟷ Engineering

WS4 Conclusions and recommendations

There is …

1) … a need to rethink design processes of ‘Beyond CMOS’
2) … a need of a new open infrastructure for the development of ‘Beyond CMOS’ design

Tasks:

- Motivation and support to facilitate communication and cooperation between design and technology actors from academia and industry
- Modeling and simulation of ‘Beyond CMOS’ devices and circuits have to be developed to gain sustainable knowledge.
- From the resulting exchange of knowledge, the “systemability” of ‘Beyond CMOS’ devices has to be proven.
- In addition “integratability” (with CMOS), manufacturability of novel technology and reliability are key factors.
- **→ to bridge the design – technology gap we have to concentrate and focus on the most promising Beyond CMOS technologies and work on the complete value chain**

Panel Session
Design Tools for 'Beyond CMOS' Technologies

Statement

Sandip Tiwari

Cornell University, USA

Editor's note: these are selected slides-full presentation in project web site.

My View by Sandip Tiwari, Cornell Univ.

1. Greatest new technologies find entirely new applications of their own.
   NP complete, robust decision making in the midst of uncertainty in devices, information input, incomplete description of the problem.

2. For new technologies, design systems are certainly very important, but robust design systems will nearly always be insufficient for the purpose of comparing to an entrenched 50 year technology infrastructure. (bipolar, nmos, cmos, …). It finds an application – digital watch for CMOS – to slowly penetrate and evolve.

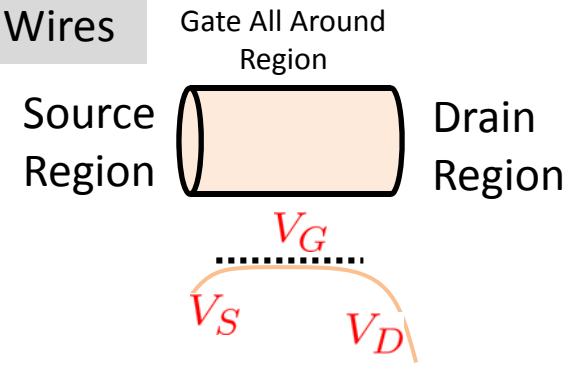
3. But, it is possible to make reasonable judgment *when some characteristic is truly inappropriate for a replacement task*.

4. If we really want to have the freedom to explore architectures, new devices in some design context, functions, …, it must be open so different expertise can come together. This needs interfaces and all the necessary attributes specified in a defined format that are required by fiat. Robustness, variabilities, functional description, … all need to be part of the framework's design.

Example: Characteristics Charge

Problem of today:
Variability(Control), Off-state current, Turn-on sharpness, Drive Current

Wires



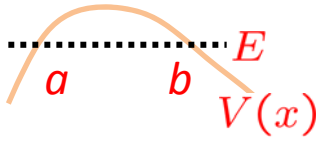
$$\frac{1}{r}\frac{\partial}{\partial r}r\frac{\partial \psi}{\partial r}+\frac{\partial^2 \psi}{\partial y^2}=0$$

Scaling: $r'=\lambda r, y'=\lambda y$

$$\frac{1}{r'}\frac{\partial}{\partial r'}r'\frac{\partial \psi}{\partial r'}+\frac{\partial^2 \psi}{\partial y'^2}=0$$

If aspect ratio retained (scaling), potential profile invariant

How small? Tunneling – off-state in traditional, on-state in tunnel FETs



$$I \propto T \approx \frac{\exp(-2\Gamma_{ba})}{\left[1+\frac{1}{4}\exp(-2\Gamma_{ba})\right]^2} \approx \exp(-2\Gamma_{ba}) = \exp\left[-2\int_a^b \gamma(y)dy\right]$$

$$\exp\left(-\int\sqrt{\frac{2m^*}{\hbar^2}}[V(y)-E]dy\right) \approx \exp\left[-2\sqrt{\frac{2m^*}{\hbar^2}}\left(\sqrt{V}L-\frac{EL}{2\sqrt{V}}+\cdots\right)\right]$$

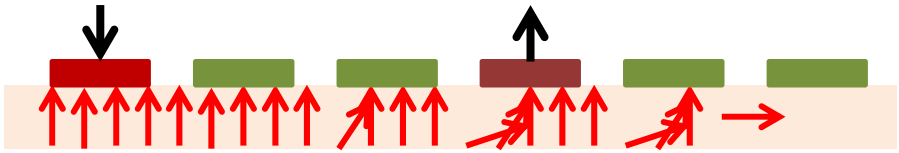
1st order term:

Current proportional to square root of potentials in barrier. Slow swing
Variance inversely proportional to length scale – tunneling.

Problem is law of large numbers in its Poisson limit. Problems of graphene, nanotubes, are much worse because of additional size, energy and its line width effects .

Example: Characteristics Spin

Magnetization switching with spin current, spin qubits, …, spin-torque flipping limits



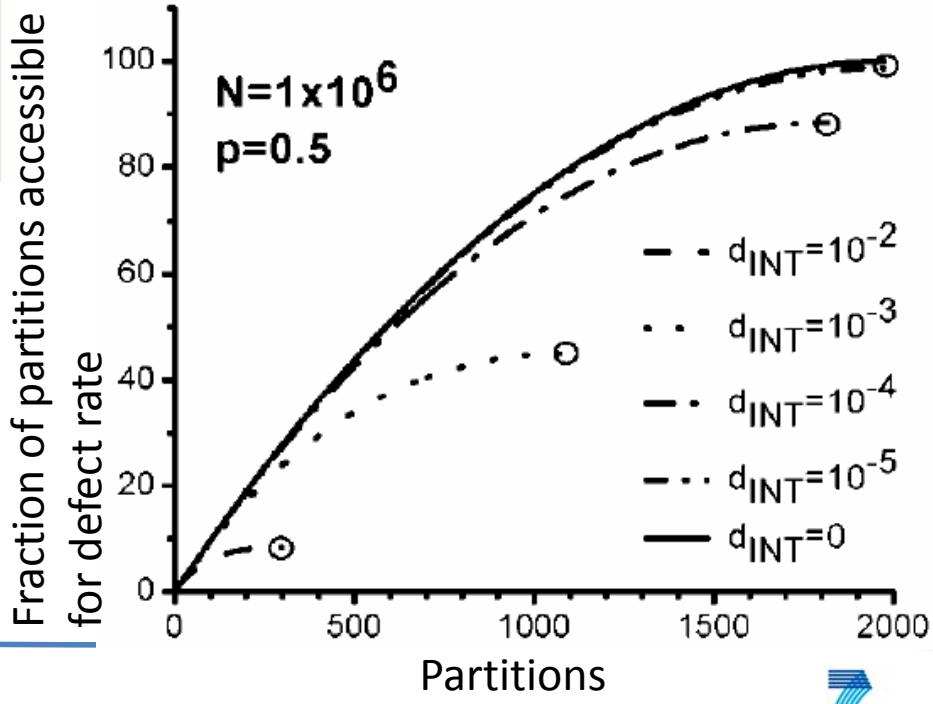
Spin transport, Signal loss⇔failure rate

$$q = 1 - \exp\left(-\frac{\ell}{\lambda_c}\right)$$

for $q = .001$ $\ell = 0.001\lambda_c$
if $\lambda_c = 100\ \mu m, \Rightarrow \ell = 100\ nm$

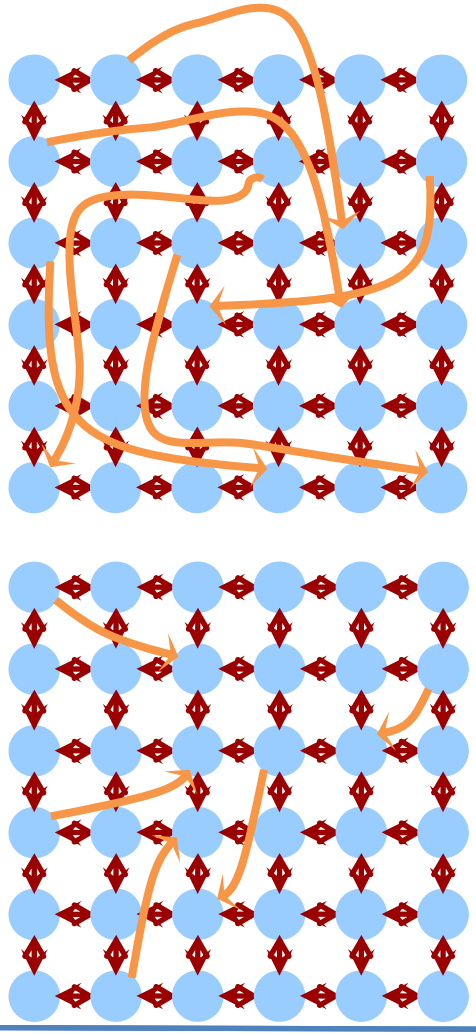
For normal distribution of errors, fraction of usability.
This in turn raises power for error correction, and devices that cannot be used.

Signal recoverable up to q of ½. If $\lambda_c/2 = 50\ \mu m,$ energy of $\approx 1\ V \times 10\ \mu A = 10\ \mu W$ needed per recovery, or $400\ mW/cm^2$+ area. I think these are quite optimistic numbers.

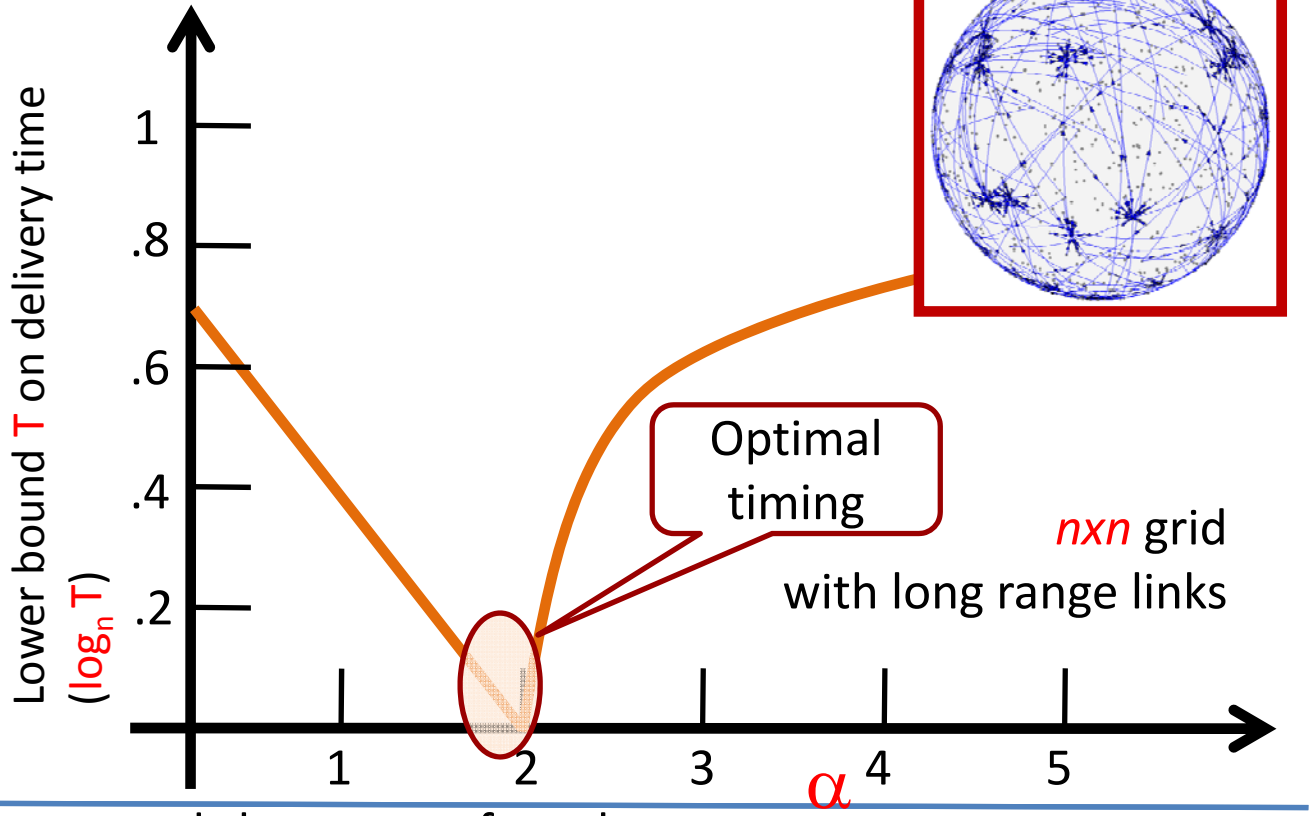


An Important Issue We Forget: Networks – Timing in Large Integration

Small World Network: A class of networks with orderly local structure and small diameter
Watts-Strogatz (1998)



Long range percolation model: For each node *v*, add directed link to random node *w* with probability proportional to $p(v,w)^{-\alpha}$ where $p(v,w)$ is the lattice distance from *v* to *w*.



Build a mixture of long range and short range for robustness

NANO-TEC

SEVENTH FRAMEWORK PROGRAMME

Bayesian Engines

Machine learning models – hidden Markov, neural nets, … Bayesian/Belief networks
Such Bayesian probabilistic networks for AI, signal processing, data mining, …. in dedicated hardware.

Acyclic Graphs:

$$p(X_1, \cdots, X_n) = \prod_{i=1}^{n} p[X_i | Parent_i]$$

Outgoing: Sum-product normalized
Incoming: Max-sum normalized

Basic Computational Blocks

Dedicated evolving networked hardware using suitable electronic devices. High FI, High FO

Probabilistic gates of Inexact approaches

This opens up thinking about new devices in an entirely new way.

Panel Session
Design Tools for 'Beyond CMOS' Technologies

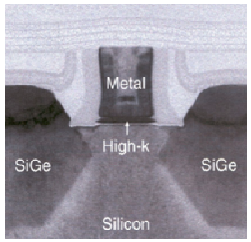
Statement

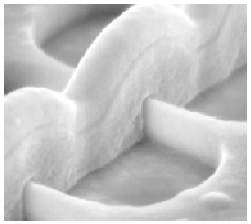
Mustafa Badaroglu
IMEC, Leuven, Belgium
badar@imec.be

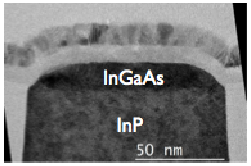
Editor's note: these are selected slides-full presentation in project web site.

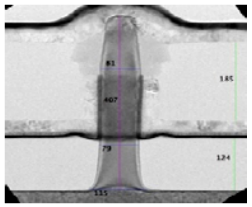
TECHNOLOGY ROADMAP & CHALLENGES

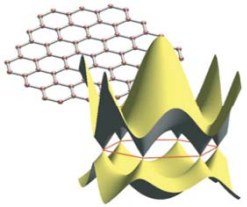
V_{dd}	1.0/1.1V	0.9/1.0V	0.8/0.9V	0.7/0.8V	0.6/0.7V	0.5/0.6V	< 0.5V
Process-induced Strain Engineering	Advanced Gate Stack Engineering		Fully-depleted Channel Electrostatics		Band-Engineered Channel for Enhanced Transport		New Transport & Extreme Channel Electrostatics
SD/stressors	Metal Gate +High-k		Multigate FETs		III/V & Ge channels	Nanowires Tunnel FETs	2D Quantum Materials + Spintronics



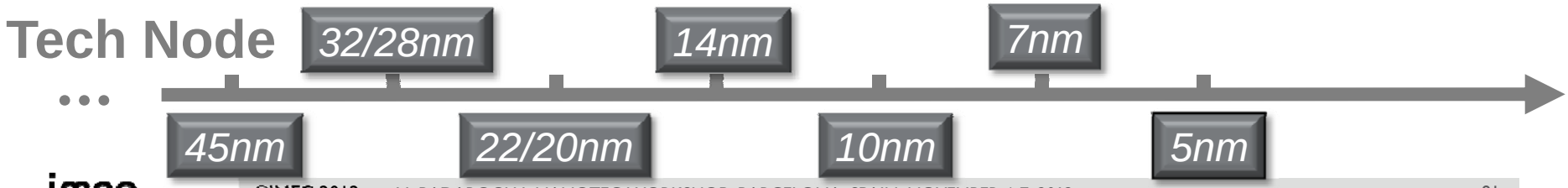








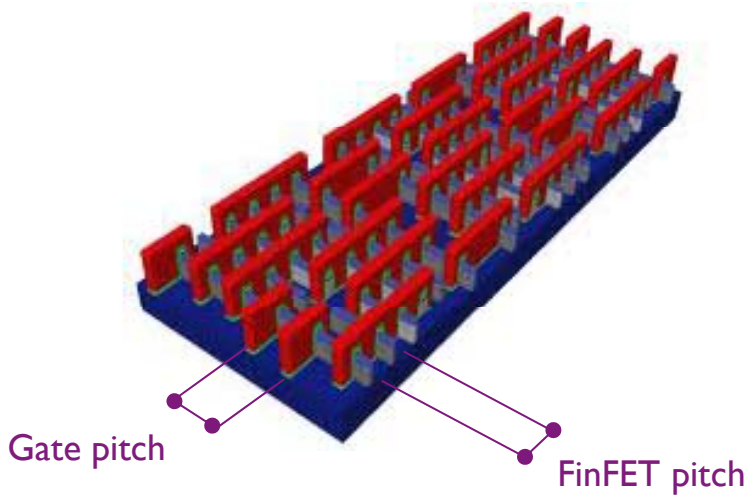
Device	Gate leakage	SCE	Ion/Ioff: Leakage	Variability	Weak drive
Interconnect	Capacitance	Resistance	EM	Congestion	Advanced transport
Patterning	Restrictions	Multiple patterning		EUV/DSA/X-ray	



DEVICE SCALING TARGETS UNDER CONSTRAINTS

- >50% area downscaling node-to-node
- >30% more fmax node-to-node at constant power
- >20% more fmax at constant leakage
- >35% more fmax at constant energy
- <15% process cost

Pitch scaling to ensure 50% area downscaling

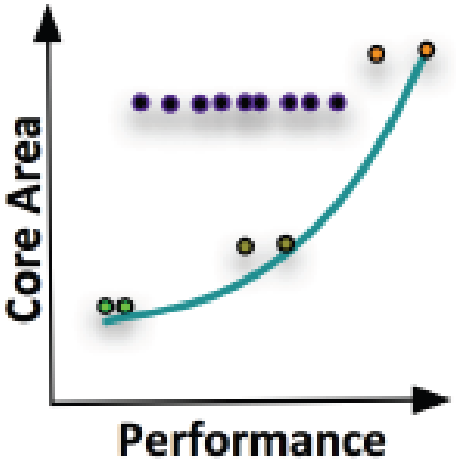


	28	20	14	10	7	5
Poly pitch - [nm]	110	82	58	40	29	20
Metal pitch - [nm]	90	64	44	30	22	15
L - [nm]	30	24	20	14	10	7
fin pitch - [nm]	0	0	42	30	21	15
fin Width - [nm]	0	0	10	7	5	3.5
fin Height - [nm]	0	0	30	23	16	10.5

PARETO FRONTIERS FOR SYSTEM SCALING

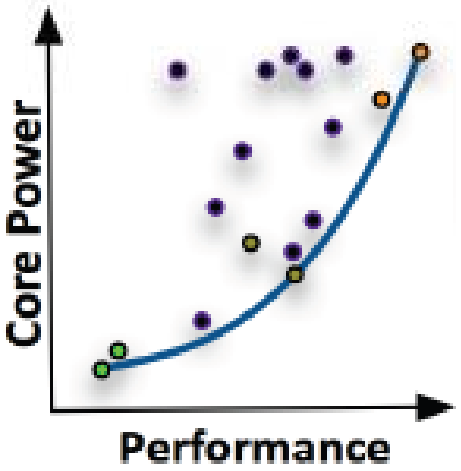
Parallelism Limits

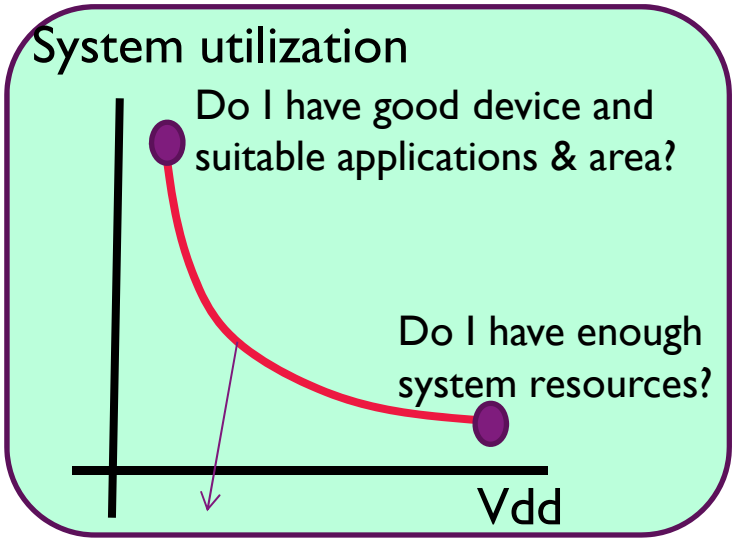
$, Yield, Skew, Interconnect, Leakage



Power Limits

Thermal, Battery, Skew, Variability, Reliability



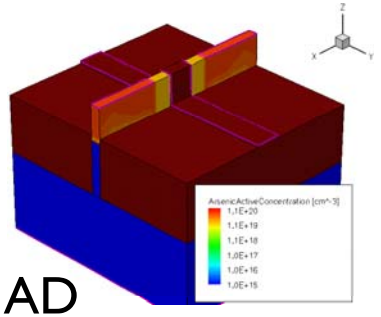


USE AS MUCH AS POSSIBLE EXISTING INFRASTRUCTURE WITH NEW PHYSICS

Determine what you need from device for your architecture

Know your implementation/manufacturability constraints

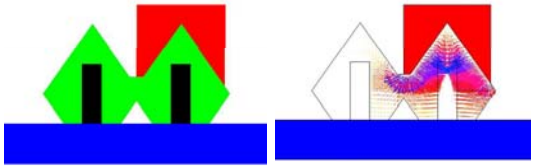
Implement models that designers could use



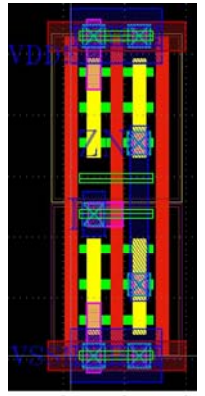
TCAD

- Physical modeling (e.g. TCAD, Matlab for what-if analysis, Magnetics simulator, thermomechanical simulator, quantum simulator)
- Multi-physics compact model (e.g. VerilogA, VHDL-AMS): fitting model, equation-based, no solvers
- Convert multi-physics to electrical

Layout basic cells (stdcell, memory cell)



EXTRINSIC PARASITICS



CELL

- Patterning
- Extrinsic parasitics

Circuit-level (e.g. RO, datapath) multi-physics transient simulation

Implement simple modules – (synthesis, P&R, backannotation)

CONCLUDING REMARKS

System (top-to-bottom) and device (bottom-to-top) must meet in the middle before brute-force design

Compact models must connect multi-physics to transient electrical properties

Interconnect (e.g. transport, parasitics) must always be included in design flow

4th Workshop: Elaboration of Recommendations

WRAP-UP

Clivia M Sotomayor Torres (ICN)
Wladek Grabinski (EPFL)

TIMELINE

RECOMMENDATIONS

Team works to produce an updated version soon after it.
Expects to upload public version by end of November for wide use and dissemination .
Please send inputs comments to rapporteurs by end of this week.

DISSEMINATION

Project will distribute to the Commission, NCPs, funding agencies, learned societies, networks and interest groups

- **Project ends 28th February 2013**

OBJECTIVES - TAKING STOCK

Have we contributed to establishing the joint design-technology community?

- Made a good start
- Found methodological issues
- Participation of the community at large could have been stronger.

How to advance further?

- A follow up CA?
- Practical implementation of our own recommendations?
- One or more projects?

How useful can our recommendations be?

- As much as we disseminate and persuade
  → lobbying

Have we been sufficiently adventurous?

- TI, new paradigms, 12 -25 year time scales.

THANKS to all who are contributing to this exercise.