Workshop 4

Summary and Recommendations on the Technology-Design Ecosystem for Nanoelectronics

Panel Discussion:

Design Tools for Beyond CMOS technologies

NANO-TEC

SEVENTH FRAMEWORK PROGRAMME

Panelists:

- Prof. Dr. Wolfgang Rosenstiel, edacentrum and University of Tübingen;
- Prof. Dr. Paolo Lugli, Technical University of Munich;
- Prof. Mustafa Badaroglu, imec;
- Prof. Dr. Sandip Tiwari, Cornell University, Ithaca, N.Y.

Chair:

- Dr. Livio Baldi, Micron Semiconductors Italia, Agrate Brianza

NANO-TEC

SEVENTH FRAMEWORK PROGRAMME

Setting the stage

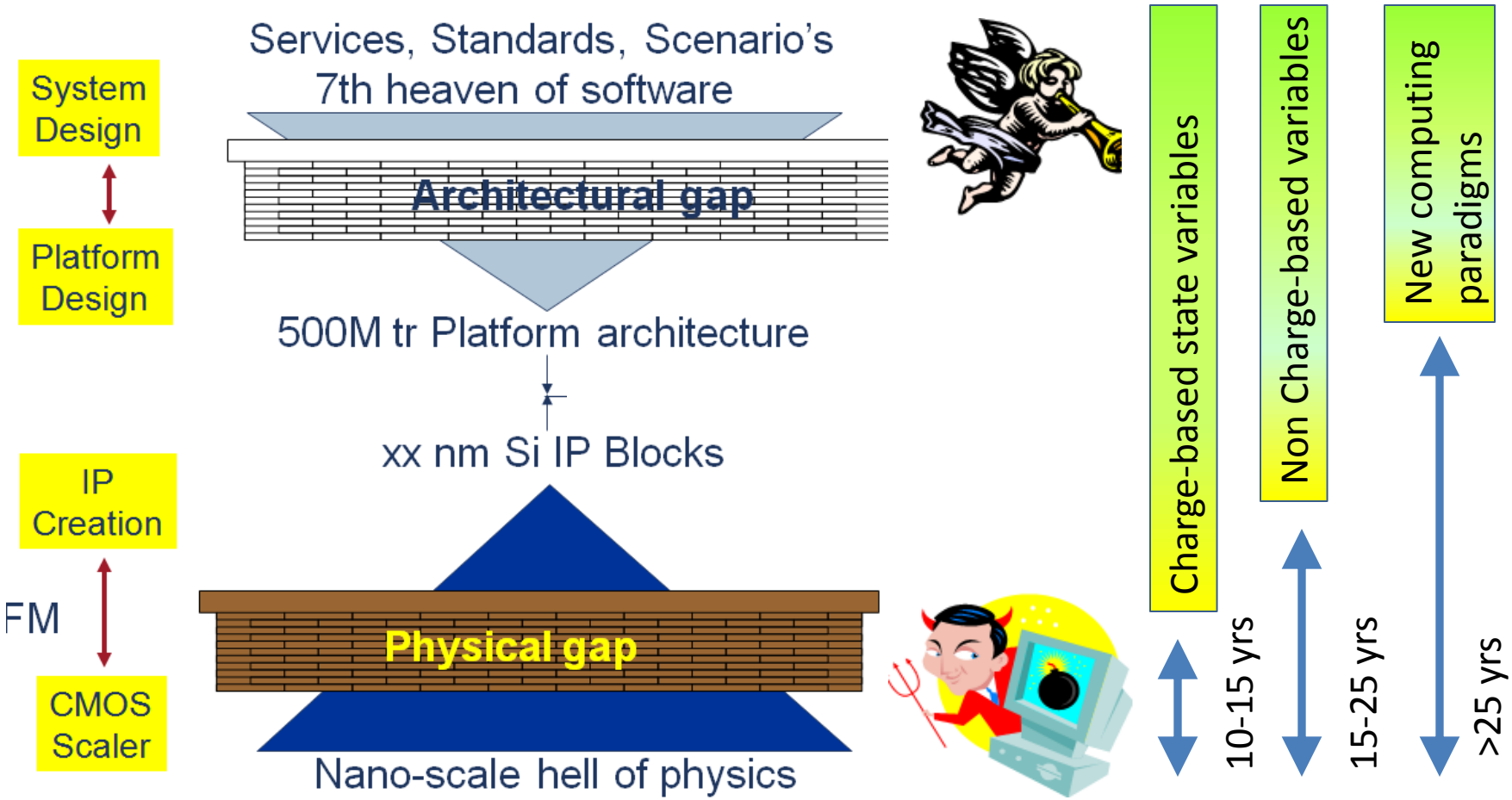
- Non CMOS technologies can complement CMOS in several applications (nice to have).
- Must have is More Moore continuation beyond CMOS scaling limits (must have) for logic or memories.
- But Moore's Law is **NOT** about transistor size but about device complexity.
- Are we sure that CMOS size is the critical parameter?
  - In logic technology half-pitch is usually much larger than transistor length
  - A sizable percentage of transistors is there just for signal buffering.

A less known prediction by Moore

NANO-TEC

SEVENTH FRAMEWORK PROGRAMME

What can be saved?



NANO-TEC

SEVENTH FRAMEWORK PROGRAMME

Key Questions

- Are design tools the main bottleneck for Beyond CMOS?
- Can a new technology solve the limitations of current tools?
- If new tools/architectures become available, will we really need a new technology?
- What can trigger the investment needed for new technology/tools?

Panelists:

- Prof. Dr. Wolfgang Rosenstiel,
  edacentrum and University of Tübingen;
- Prof. Dr. Paolo Lugli,
  Technical University of Munich;
- Prof. Mustafa Badaroglu,
  imec;
- Prof. Dr. Sandip Tiwari,
  Cornell University, Ithaca, N.Y.

Chair:

- Dr. Livio Baldi,
  Micron Semiconductors Italia, Agrate Brianza

NANO-TEC

SEVENTH FRAMEWORK PROGRAMME