



4th Workshop: Elaboration of Recommendations

The ecosystem technology in beyond CMOS in Europe

Rapporteurs:

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WHICH ECOSYSTEM ?

Our scope: “Beyond CMOS”

Information processing, memory, communications

Our input comes from:

all beyond-CMOS conclusions from NANO-TEC

+ known activities in Europe

+ electronics survey

+ the NANO-TEC projects recommendations for the future

CONTEXT

- A critical issue in beyond CMOS research is the availability of advanced technology.
- The ecosystem technology has many players
- A clear definition of the roles of the respective players is needed in order to avoid non-constructive competition and waste of resources

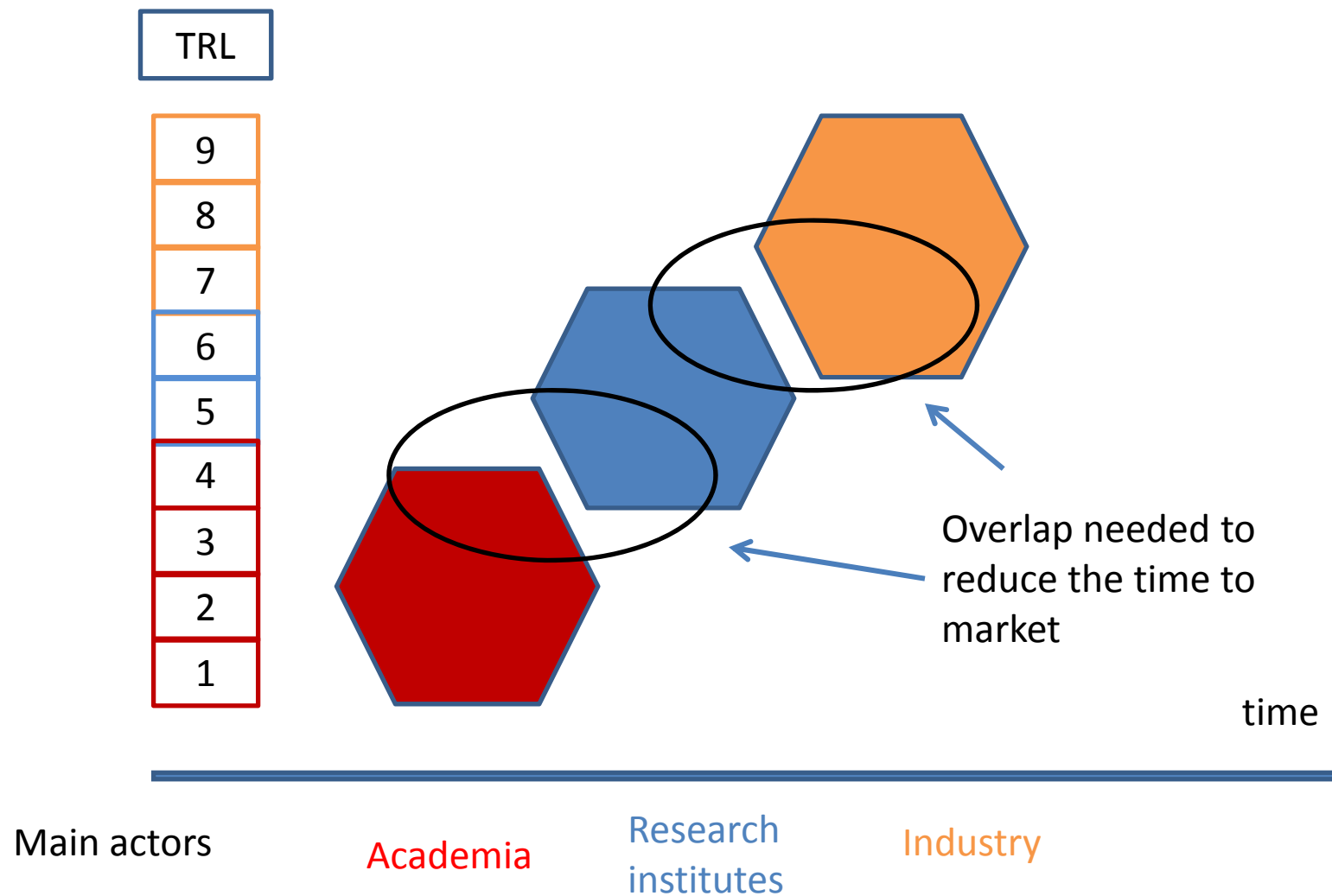
CONTEXT

The ecosystem technology has three main players with different access status

- **Academia** (with an R&D horizon > 6 years, TRL 1-4) – *basic understanding, test and validation of innovative architectures, materials and processes for future ICT.*
- **Research Institutes** (RTOs, Integration Centres with R&D horizon 3–6 years, TRL 3-7) – *Technology implementation and the assessment towards Production Equipment; development of high performance components.*
- **Industry** (with R&D horizon < 3 years, TRL 6-9) – *Technology research, innovation and exploitation; Process introduction and continuous improvement with innovative approaches (yield, reliability,...).*

CONTEXT

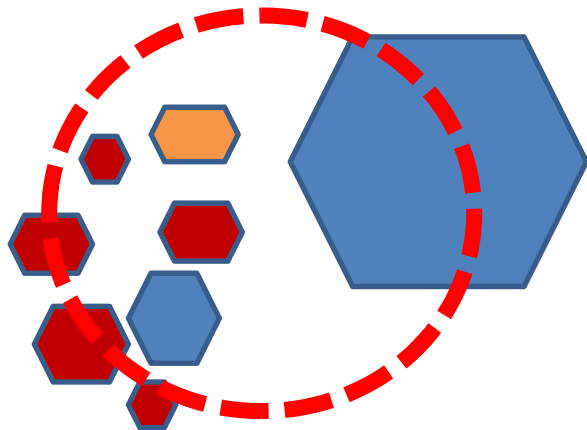
TRL metrics



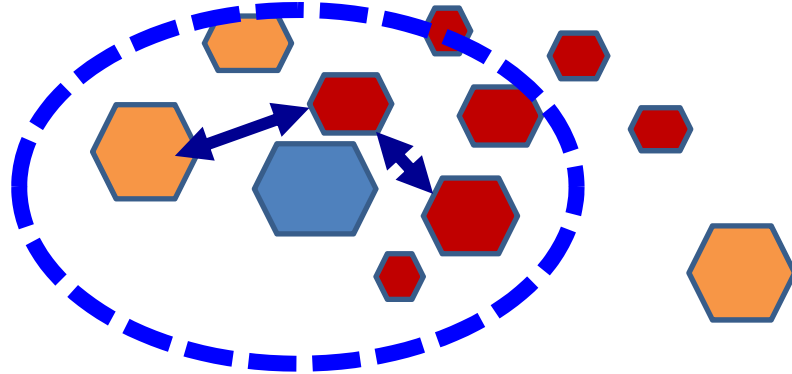
CONTEXT

Ecosystem aspects

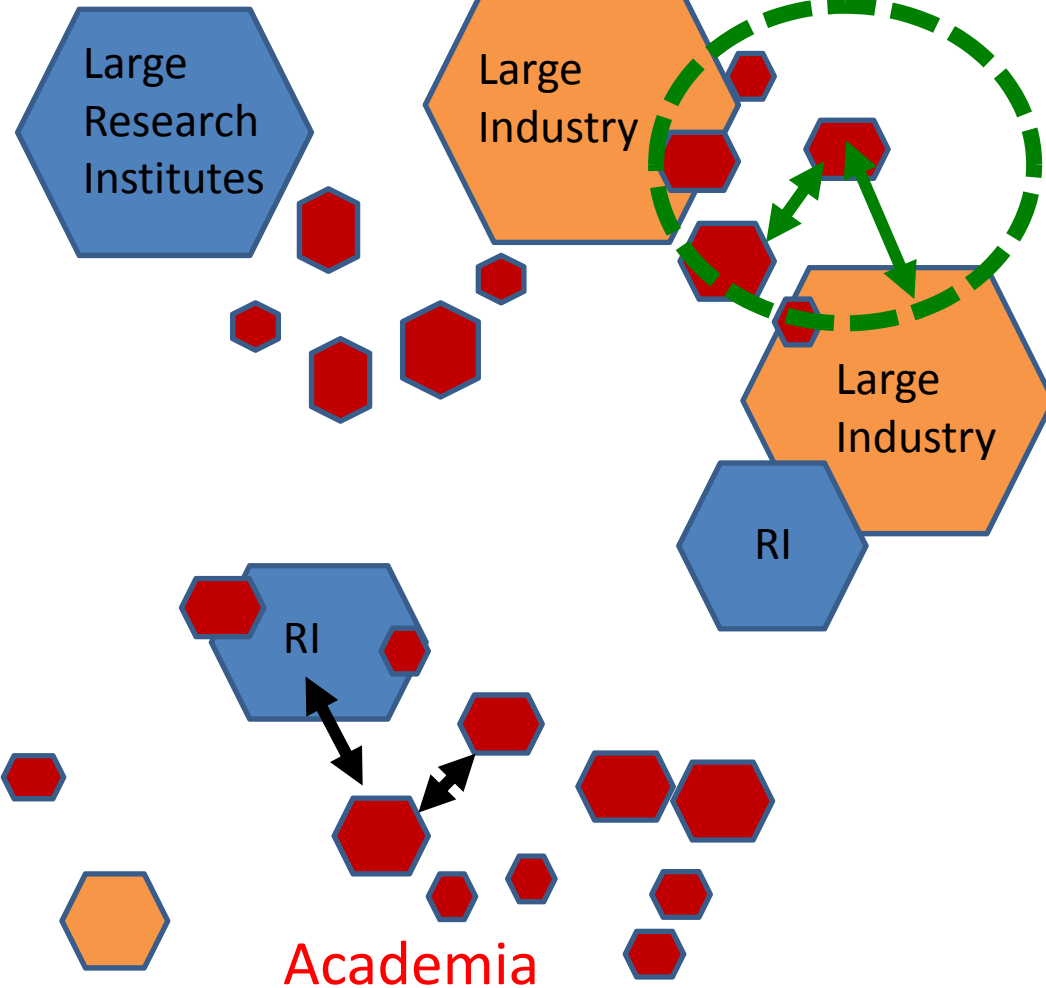
Regional Clusters
Regional Ecosystem



Regional Clusters
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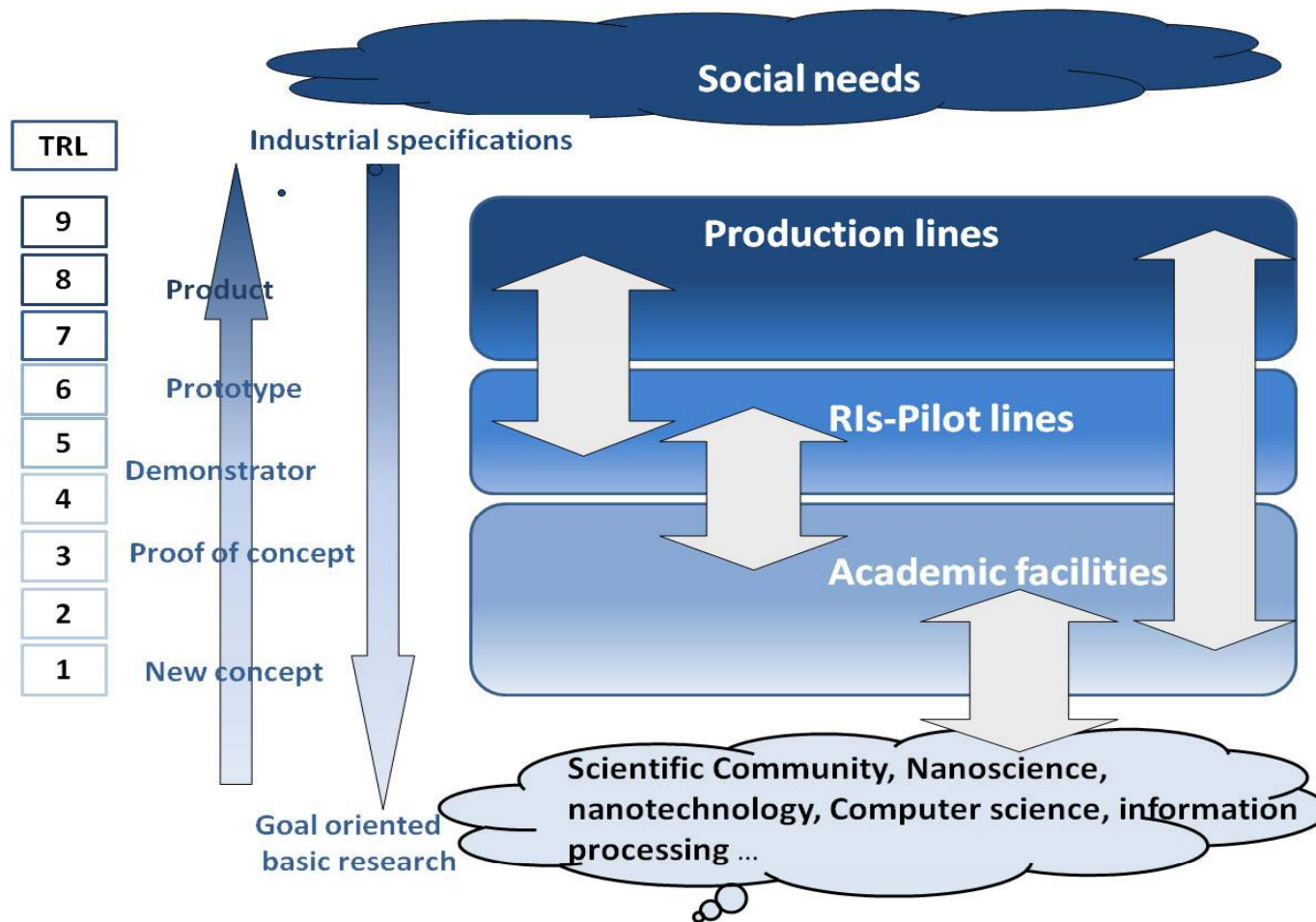


BEYOND CMOS TECHNOLOGY ECOSYSTEM

Beyond CMOS address medium/long term technologies: the main players are academia and large research institutes. BUT the active role of Industry is mandatory:

- to contribute to the identification of relevant long-term fundamental research topics needed in the value chain,
- to define expectations for ultimate CMOS technology, applications, and services (> 2015),
- to provide critical feedback to research institutes and academia.

BEYOND CMOS TECHNOLOGY ECOSYSTEM



BEYOND CMOS DEVICE TECHNOLOGIES?

- Using the three device categories chosen for workshop 4, we can describe a little bit the technology state of the art and the needs to push the technology forward.
- Digital with charge as state variable (New semiconductor transistor (TFET,i-MOS, III-V, nanowire...but also nanomechanical switch). Generally , the demonstration is carried out for a single device or low complexity circuits. To demonstrate better performance than CMOS (at least for one or two parameters), manufacturability is a key question. So the main difficulty is the access to large scale infrastructures (LSI) at reasonable cost. Design is not a problem if the new device can simply replace CMOS

BEYOND CMOS DEVICE TECHNOLOGIES?

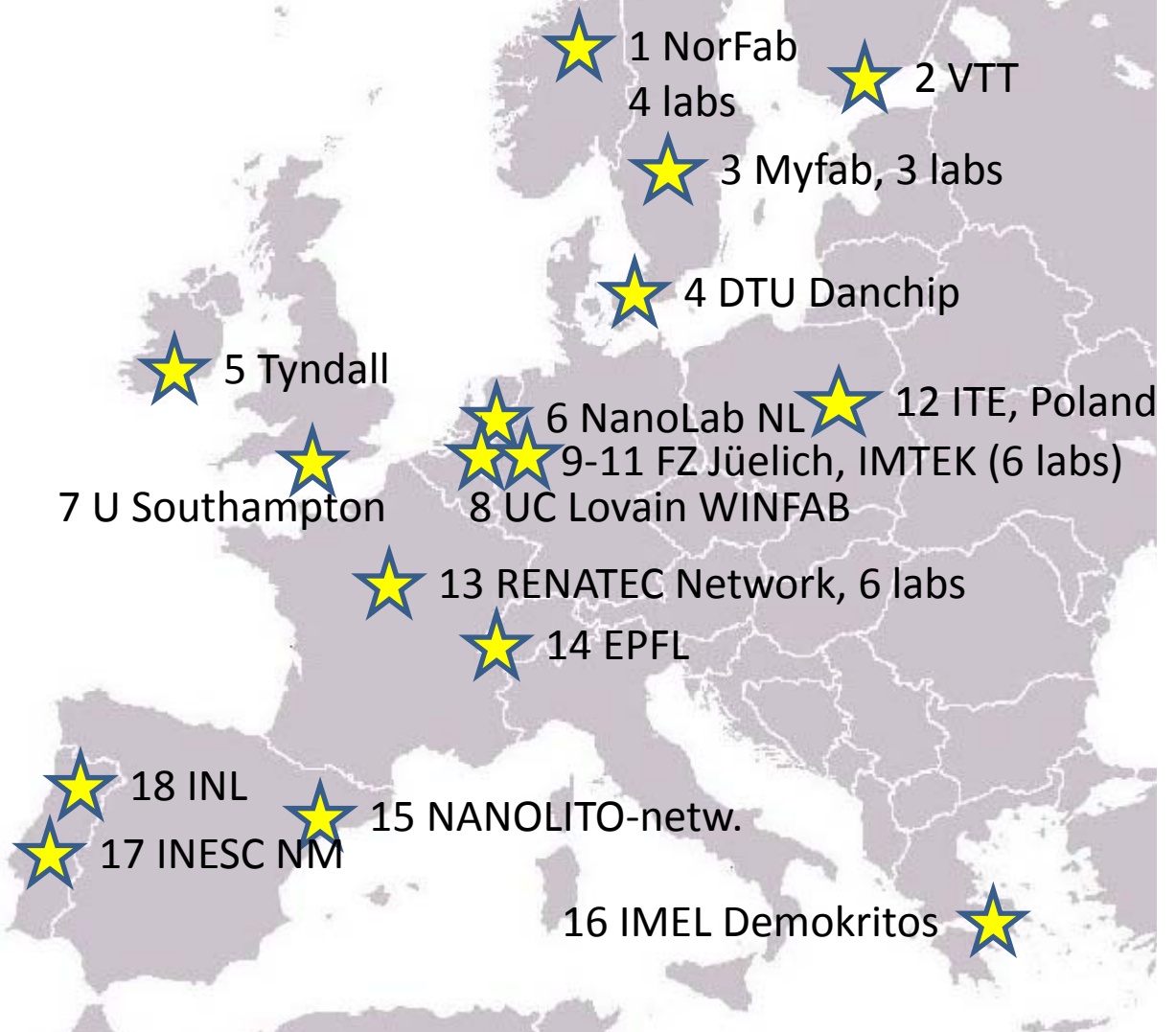
- Digital with state variable other than charge (Spin, molecular state....) For this domain, the objective is mainly to demonstrate the possibility to use of a new two state device to make digital circuits. Manufacturability on a semiconductor process line is a key question.
- Non digital (quantum, neuromorphic). For this domain, the notion of device is not relevant. Completely new technology (self assembly) can be proposed for which the technology ecosystem is not clear.

Bottom-up infrastructure networking and mapping

- A grass-root mapping approach to European infrastructures $>\approx 500 \text{ m}^2$
- to connect small ecosystems (typically small RI, regional networks) to large institutes and industry
- Bottom-up and open access approach: several coordinated proposals submitted (Myfab, NorFab, RENATECH, TRAIN²-network etc.) to the EU-open consultation (22 October).
- Not the complete picture – but the NANO-TEC map of our extended infrastructure network (inclusive approach)
- Additional input to the final report wanted!

European Infrastructure Network

- 1 NorFab, Norway, (4 labs)
- 2 Finland, VTT, Finland
- 3 Myfab, Sweden (3 labs)
- 4 Danchip, Denmark
- 5 Tyndall, Ireland
- 6 NanoLabNL, Holland
- 7 Twente, The Netherlands
- 8 U. Southampton, England
- 9 UC Lovain, Belgium
- 10 FZ Jülich, Germany
- 11 IMTEK/HSG-IMIT Germany
- 12 ITE, Poland
- 13 RENATEC, France (6 labs)
- 14 EPFL, Switzerland
- 15 NANOLOTO, Spain (x labs)
- 16 IMEL Demokritos, Greece
- 17 INESC NM, Portugal
- 18 INL, Portugal



BEYOND CMOS TECHNOLOGY PLAYERS: MEDIUM SCALE FACILITIES

1. Austrian Institute of Technology (AIT, www.ait.ac.at/), Austria
2. Catalan Institute of Nanotechnology (www.icn.cat), Spain
3. Cavendish Laboratory, University of Cambridge (www.phy.cam.ac.uk/), England
4. Danchip/DTU (www.danchip.dtu.dk/English.aspx), Denmark
5. EPFL NanoLab (nanolab.epfl.ch/), Switzerland
6. Forschungszentrum Jülich (FZ-Jülich, www.fz-juelich.de), Germany
7. IMB-CNM (www.imb-cnm.csic.es/), Spain
8. IMEL/NCSR Demokritos (imel.demokritos.gr/index.shtml), Greece
9. Institute of Electron Technology (www.ite.waw.pl/en/), Poland
10. Myfab, the Swedish Research Infrastructure for Micro and Nano Fabrication (www.myfab.se)
11. NorFab (www.norfab.no/), Norway

BEYOND CMOS TECHNOLOGY PLAYERS: MEDIUM SCALE FACILITIES

12. Reykjavik University, Iceland, (en.ru.is/)
13. Royal Institute of technology (KTH) (www.kth.se/en), Sweden
14. RWTH Aachen, (www.fh-aachen.de) Germany
15. SINTEF (www.sintef.no/home/), Norway
16. TNO (www.tno.nl), The Netherlands
17. TU Delft (<http://www.dimes.tudelft.nl/>), The Netherlands
18. Tyndall (www.tyndall.ie) Ireland,
19. UCL (www.uclouvain.be), Belgium
20. University of Glasgow (www.gla.ac.uk), UK
21. University of Twente, MESA+ (www.utwente.nl/mesaplus), The Netherlands
22. VTT (www.vtt.fi), Finland

BEYOND CMOS TECHNOLOGY PLAYERS: LARGE SCALE FACILITIES

- LETI (<http://www-leti.cea.fr/>) *France , Olivier Peyret*
- IMEC (www.imec.be) Belgium,
- Nanocenter Dresden (incl. 2 Fraunhofer Institutes: IPMS, IZFP) (www.nanodresden.de), Germany

YOUR OPINION ON THE GENERAL 'BEYOND CMOS' EUROPEAN CAPABILITIES

	good	average	poor	no answer
... in modeling and design: *	11	6	1	1
... in research infrastructure tools: *	11	7	1	0
... in research infrastructure processes: *	10	7	2	0
... in research infrastructure staff: *	14	3	1	1
... in education and training : *	6	9	2	2
... for proof of concept : *	12	6	1	0
... for demonstrators: *	8	8	3	0
... for early integration in systems : *	4	7	6	2

2. Specific questions about the NANOTEC topics

2b. Your opinion on the European capabilities in spintronics concerning ...

	good	average	poor	no answer
... modeling and design in spintronics: *	10	2	0	7
... device and circuit processing in spintronics: *	8	3	1	7

2. Specific questions about the NANOTEC topics

2c. Your opinion on the European capabilities in nanowires concerning ...

	good	average	poor	no answer
... modeling and design in nanowires: *	12	2	2	3
... device and circuit processing in nanowires: *	9	5	2	3

2. Specific questions about the NANOTEC topics

2d. Your opinion on the European capabilities in graphene concerning ...

	good	average	poor	no answer
... modeling and design in graphene: *	11	3	0	5
... device and circuit processing in graphene: *	8	3	3	5

2. Specific questions about the NANOTEC topics

2e. Your opinion on the European capabilities in MEMS concerning ...

	good	average	poor	no answer
... modeling and design in MEMS: *	11	2	1	5
... device and circuit processing in MEMS: *	11	1	2	5

2. Specific questions about the NANOTEC topics

2f. Your opinion on the European capabilities in solid state quantum computing concerning ...

	good	average	poor	no answer
... modeling and design in solid state quantum computing: *	5	4	2	8
... device and circuit processing in solid state quantum computing: *	4	2	5	8

2. Specific questions about the NANOTEC topics

2g. Your opinion on the European capabilities in neuromorphic computing concerning ...

	good	average	poor	no answer
... modeling and design in neuromorphic computing: *	8	3	1	7
... device and circuit processing in neuromorphic computing: *	7	4	1	7

3. STATUS OF THE RESPONDENT?

Domain of activity: *

Organism: *

Are you partner of a FP7 project (IP, STREP, NoE...) in nanoelectronics?:

Are you partner of a FP7 project (IP, STREP, NoE...) in nanoelectronics? If yes, please tell us the name and type.

Additional information concerning European capabilities regarding Technology-Design of the benchmarked technologies:

1. In general Europe has good competence in design even in advanced technology and in new design tools, covering areas that are neglected by major EDA companies. Unfortunately it is the area where the market is limited or uncertain. Only MEMS and SiP design present a large growth potential.
2. Restricted access from universities to 'silicon' or to data from companies remains a huge barrier. This hinders innovation in modelling and design -- where I feel typically advantages of Europe would be.
3. Europe should launch an integrated effort combining math to cs to ee to process technologists to create a design framework whose interfaces are open and regulated so that an infrastructure can exist for taking advantage of disparate advances in materials, devices, circuits, etc. and applied to systems. Else, the ground work will not finds its way easily to society.

HOW TO IMPROVE THE BEYOND CMOS TECHNOLOGY ECOSYSTEM ?

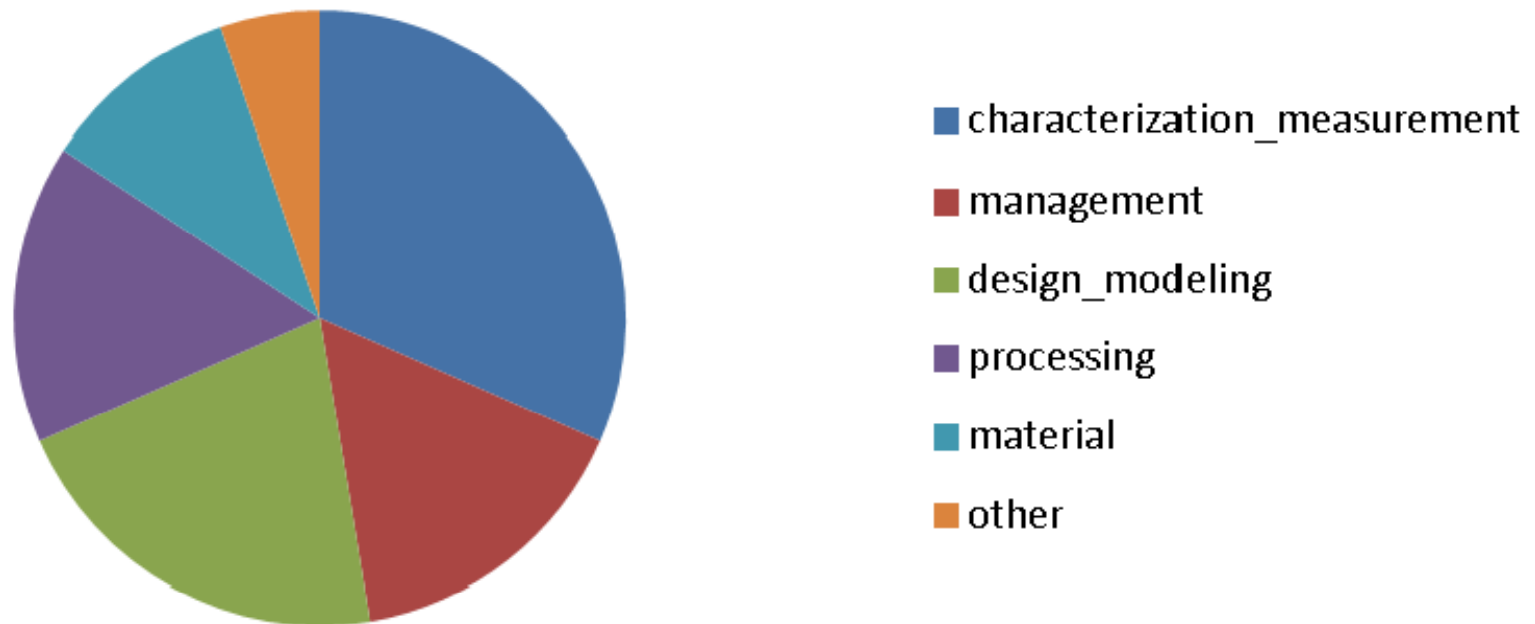
What is the opinions of the players?

The NANOTECH electronic poll:

- Posted in the NANO-TEC website July – August 2012
- Invitations sent to experts within the extended NANO-TEC network
- 19 replies registered

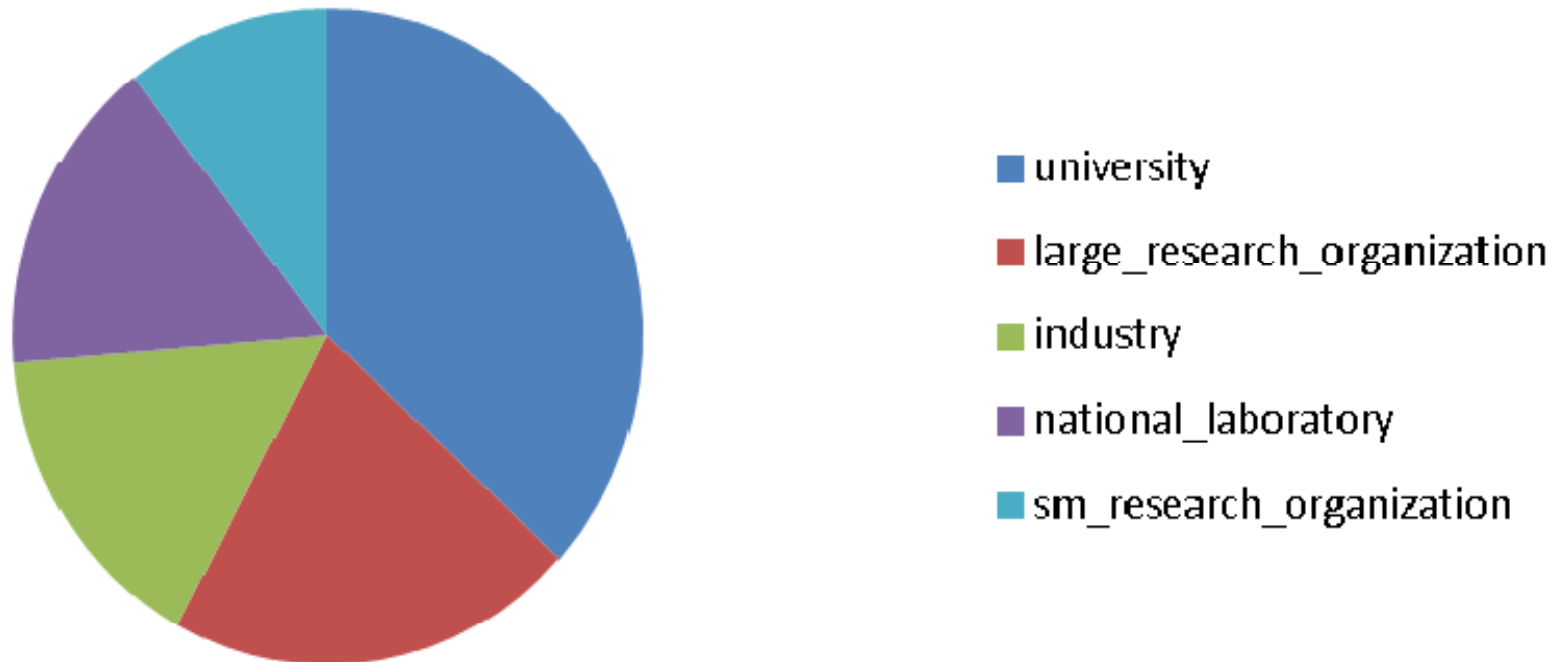
3. STATUS OF THE RESPONDENT?

**Answers came from
these domains of activity**

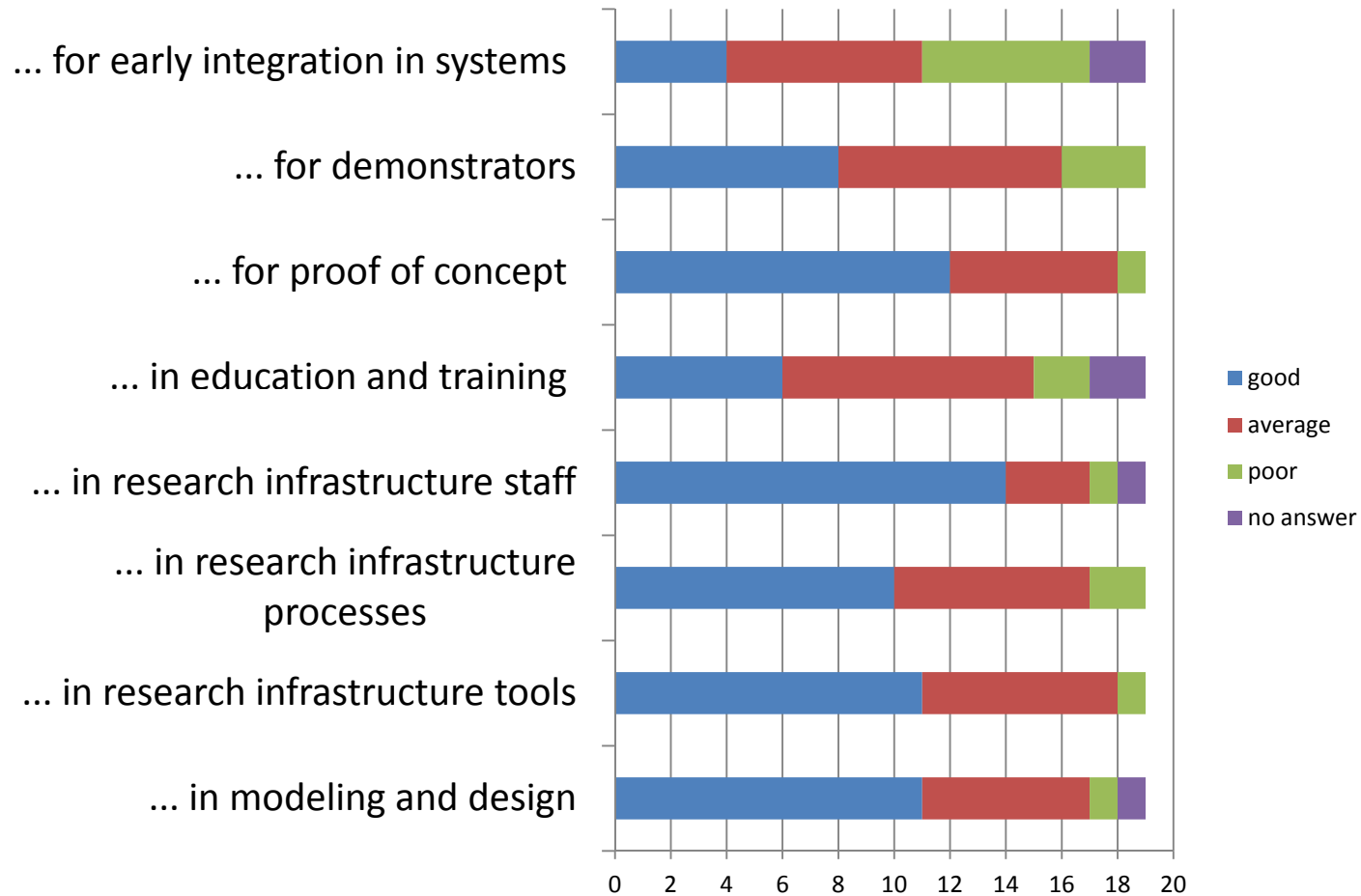


3. STATUS OF THE RESPONDENT?

Answers came from
these kind of organism

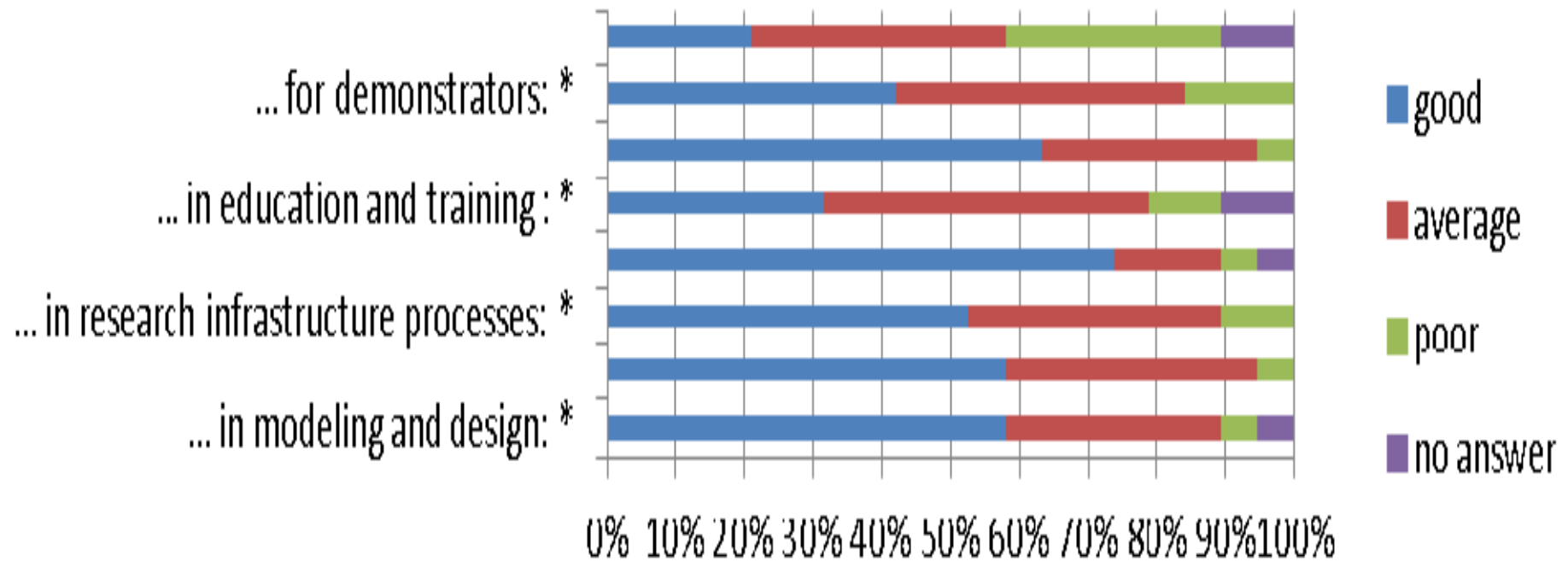


Opinion on the general "beyond CMOS" European capabilities ...



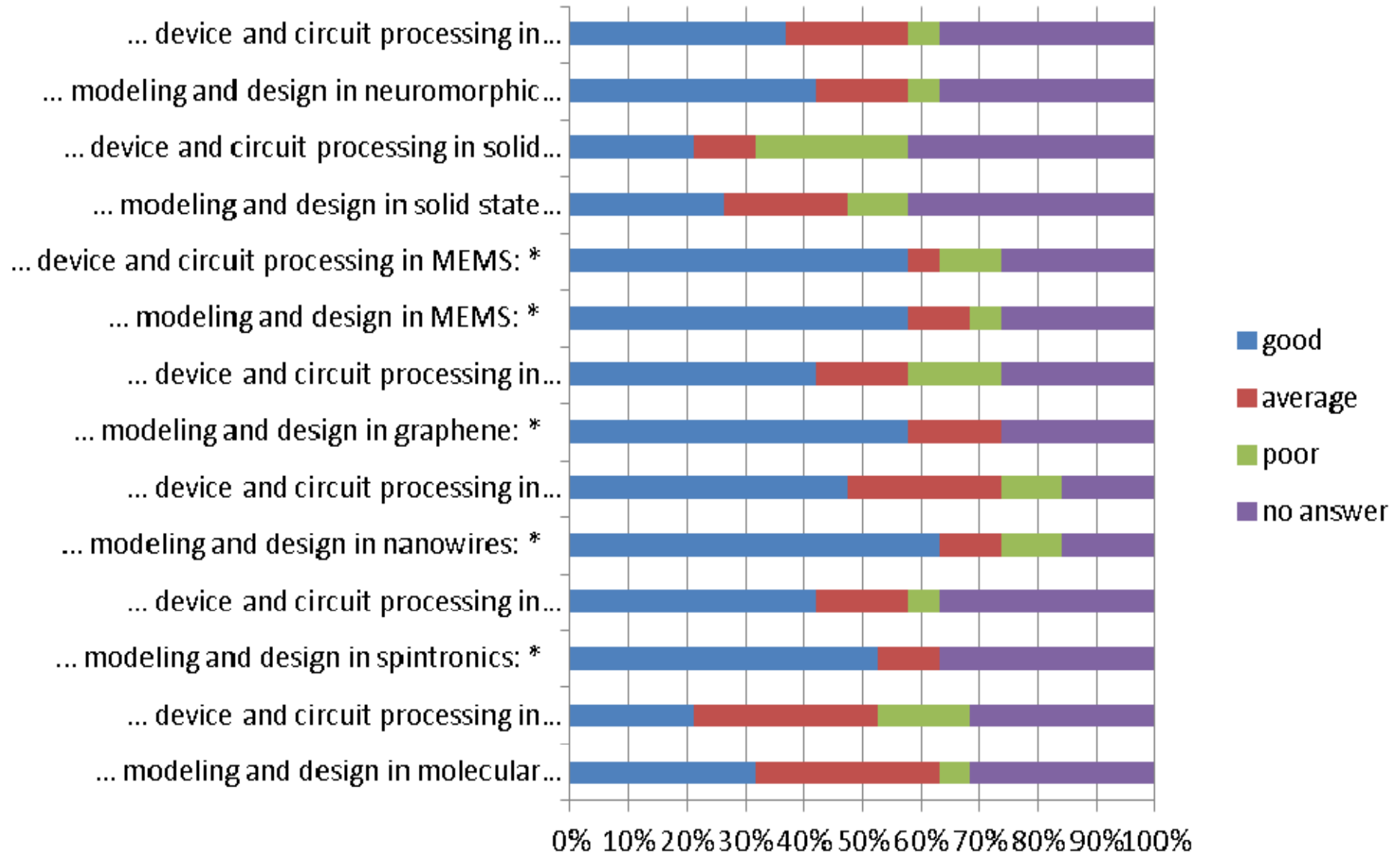
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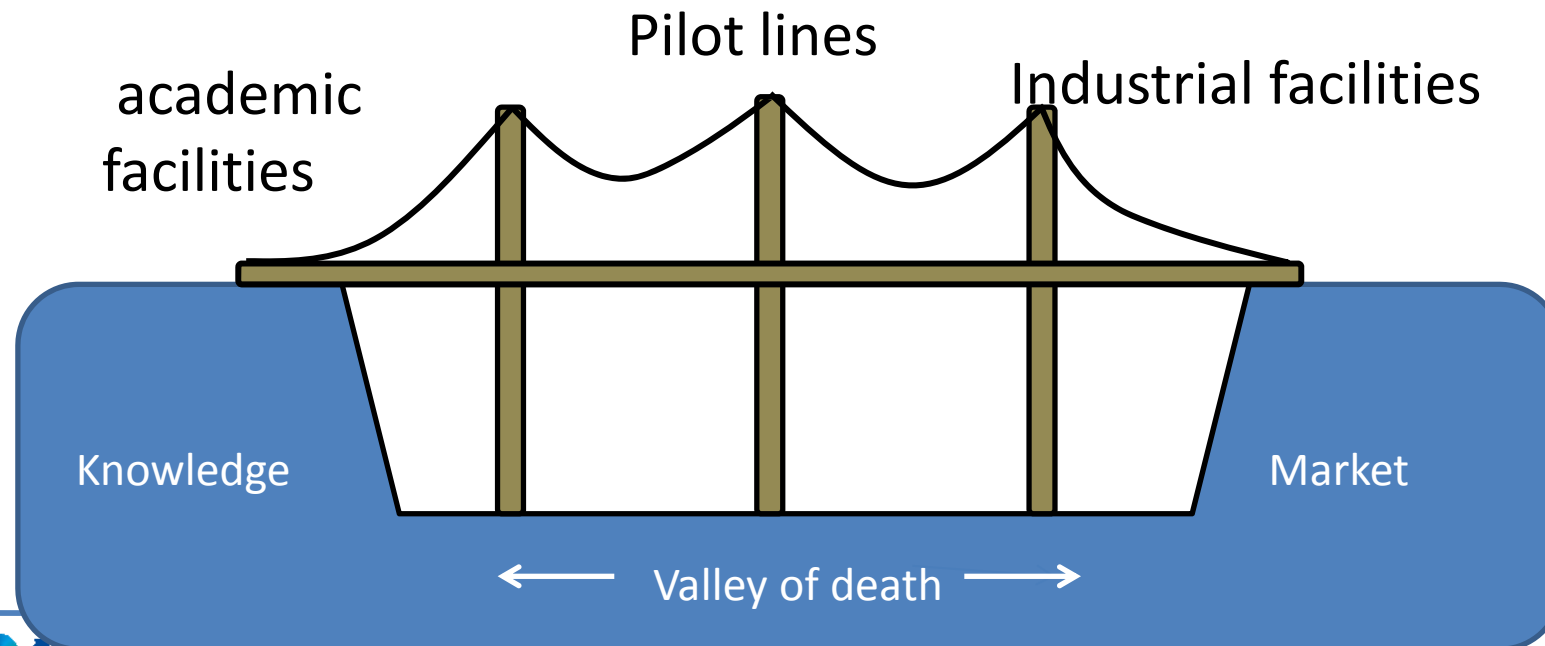
Opinion on the European capabilities concerning

...



HOW TO IMPROVE THE BEYOND CMOS TECHNOLOGY ECOSYSTEM ?

- European research is strong in beyond CMOS technologies, but the transition from ideas arising from basic research to competitive product is a weak link in European nanoelectronics value chains
- The gap between basic knowledge generation and the subsequent commercialisation of this knowledge in marketable products is known as the "valley of death" issue.



HOW TO IMPROVE THE BEYOND CMOS TECHNOLOGY ECOSYSTEM ?

Make a better connection between the three pillars

The first pillar, “academic facilities” consists of taking best advantage of European scientific excellence in transforming the ideas arising from fundamental research into technologies competitive at world level.
Proofs of concept and patents

The second pillar, “Pilot lines” consists of putting in place pilot lines having technology prototyping facilities to enable the fabrication of innovative prototypes.

The third pillar, “Industrial facilities” starting from product prototypes duly validated during the demonstration phase to create and maintain in Europe attractive economic

HOW TO IMPROVE THE BEYOND CMOS TECHNOLOGY ECOSYSTEM ?

- Many structures already exist (CATRENE, prins, ENIAC, AENAS, SINANO, ENI2, Silicon Europe, ...) gathering the same communities.

DO NOT create a new one

- How to improve the ecosystem without increased complexity ??

RECOMMENDATIONS

The first recommendation:

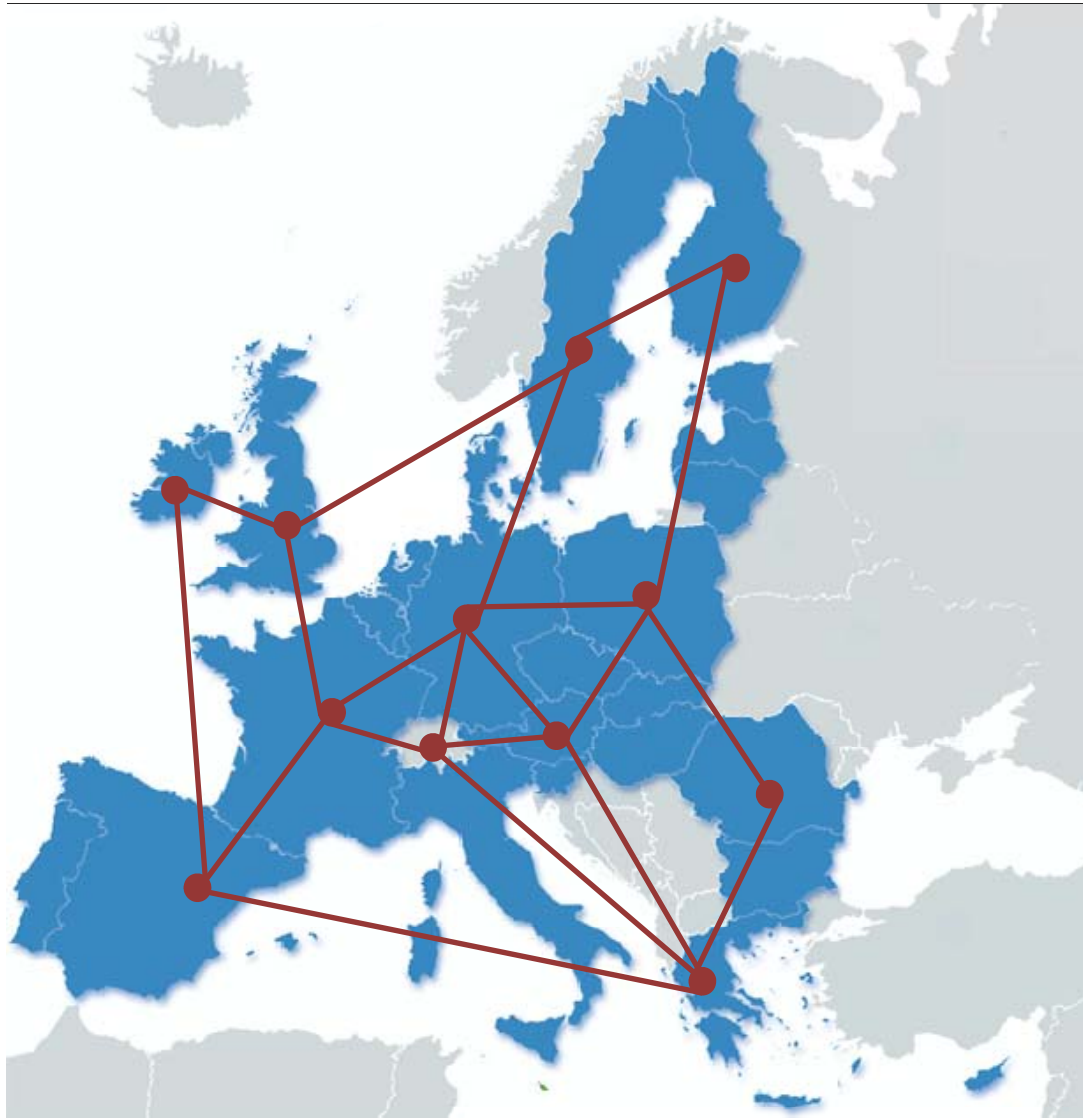
Academic networking

- We propose that Europe organize all the advanced academic technological facilities having a significant activity in beyond CMOS research in a European network with one and only one entry point in each country, each entry point having mission to represent/structure its national facilities

Do not make the picture more complicated!

- In order to avoid a new structure, it should be useful that this network could be managed by an existing initiative. This network will be complementary to the facilities of the RTO and tightly link to them in order to allow a smooth crossing of the 'valley of death'.

RECOMMENDATIONS



Academic facility
European network

RECOMMENDATIONS

The second recommendation:

Beyond CMOS education

We propose that Europe should create a multidisciplinary ‘Beyond CMOS ‘ Erasmus Mundus programme to educate a new generation of student to future information processing concepts: theory of information, binary and non binary information processing, quantum computing, neuromorphic computing.

Feedback from Industry

The low level of feedback from industry is also a weakness in Europe. It is recommended that industry will define more clearly the expectations for ultimate current technology, future needs and roadmaps of long-term research. This feedback would increase the manpower on research on subjects that are considered as strategic by industry for the long term and avoid dispersion on subjects of minor importance.