Semiconductor Research Corporation

Pioneers in Collaborative Research®

Beyond Moore's Law: SRC Views on Nanoelectronics

Victor V. Zhirnov and Ralph K. Cavin

NANO-TEC Workshop, Barcelona, Spain, November 6-7, 2012

Outline

- Industrial Collaborative Research
  - 30 Years of Semiconductor Research Corporation
- Perspectives on Moore's Law
- Moore Physics
- Beyond Moore: An Intro
- Way Beyond Moore: Hints from Nature
- Summary

Semiconductor Research Corporation

- The Semiconductor Research Corporation (SRC) was established in 1982 as a consortium of semiconductor companies to manage high priority university research
  - Concept of “pre-competitive research” defined
    - Shared resource
  - Enhanced interaction with government agencies to focus basic research
  - Model for global collaboration ultimately leading to:
    - National Technology Roadmap for Semiconductors
    - **International Technology Roadmap for Semiconductors**
    - **ITRS Emerging Research Devices Chapter provides Potential/Risk assessments for beyond- CMOS solutions**

SRC’s Charter

Objectives:

- Define relevant research directions
- Explore potentially important new technologies (**<u>and transfer results to industry</u>**)
- Generate a pool of experienced faculty & relevantly educated students

SRC’s “Founding Fathers”

Erich Bloch

Robert Noyce

Jack Kilby

Current Technical Directions of SRC Program Entities

- Global Research Collaboration (GRC):
  - Addressing CMOS scaling and scaling independent challenges collectively aimed toward continuing the viability of the current industry.

- Focus Center Research Program (FCRP):
  - Addressing technical barriers faced by semiconductor industry to enable execution of ultimate-CMOS while developing linkages to beyond-CMOS.

- Nanoelectronic Research Initiative (NRI):
  - Addressing identification of the next “switch” or “information element” enabling revolutionary new approaches that significantly increase functionality and expand system application space.

Founding SRC Companies

IBM

AMD

intel

CONTROL DATA

MOTOROLA

Honeywell

National Semiconductor

HARRIS

SILICON SYSTEMS

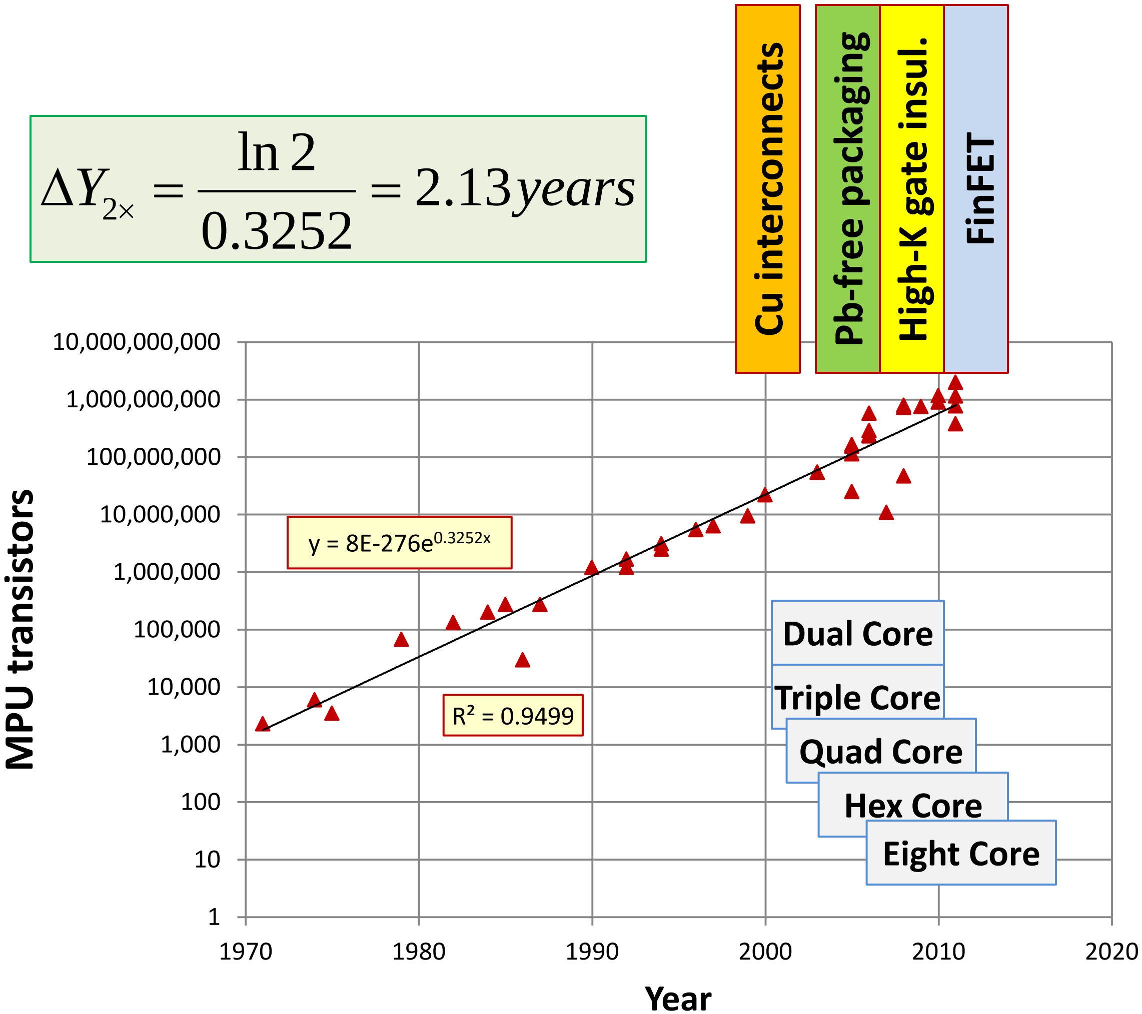
digital

GENERAL INSTRUMENT

Current SRC Member Companies

Moore's Law: 1971-2011

$$\Delta Y_{2\times} = \frac{\ln 2}{0.3252} = 2.13 years$$



Company	Model	Year
Intel	4004	1971
Intel	8080	1974
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AMD	8150	2011

The Copper Revolution

Research Start: 1989

~10 years

Cornell, Berkeley, RPI, SUNY Albany

Commercialization: 1998-2002

Need:

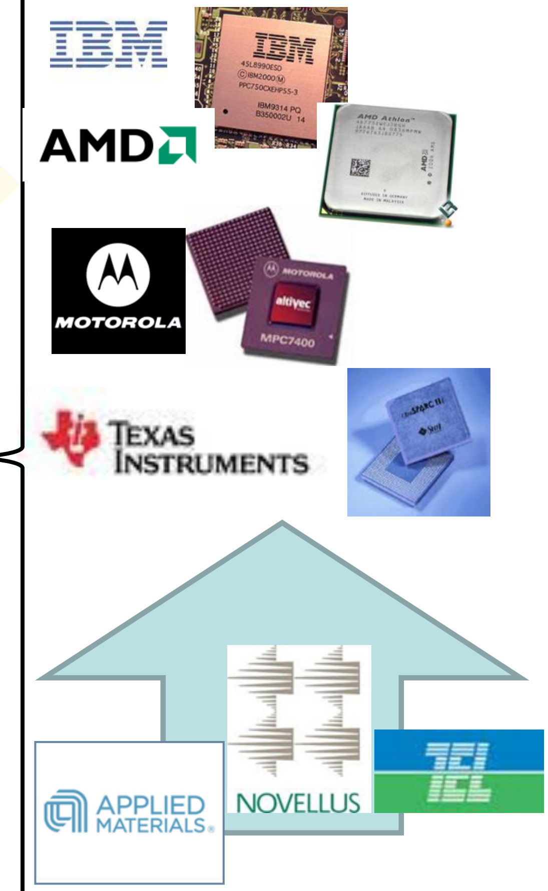
Interconnects to:

1) break the **1GHz** barrier

2) reduce power

Challenge: Replace Al with Cu

- New deposition process
- Reliability (e.g. Cu diffusion and electromigration)



15 SRC-supported influential publications

- **Early (1993) SRC papers on Cu interconnects:**

  Y. Shacham-Diamand et al, "**Copper Transport in Thermal SiO_2**", J. Electrochem Soc. 140 (1993) 2427

  124 citations; 33% by industry

  - S. P. Murarka et al, "**Advanced multilayer metallization schemes with copper as interconnection metal**", Thin Solid Films 236 (1993) 257

  197citations; 26% by industry

The high-K Breakthrough

Research Start: 1997

~11 years

Commercialization: 2008-2012

UT Austin, NCSU, U N-Texas, U S-Florida…

Need:

to address the “Running out of Atoms” crisis

Challenge:

Replacing SiO2 with high-K gate materials

- New deposition process
- Gate metal etc.

IBM, AMD, intel, Texas Instruments, freescale, GLOBALFOUNDRIES

- Innovation of high-K gate dielectrics for use 45nm and beyond technology
- Successful transfer of high-K technology to industry.
- **18** SRC-supported influential publications (>100 citations)

Paper Title	Authors	Total Citations	Industry Percentage
High-k gate dielectrics: Current status and materials properties considerations, JAP 89 (**2001**) 5243	Wilk / Agere, Wallace /U. N Texas, Anthony/ U. S Florida	**3288**	**27%**
High quality ultra thin CVD HfO2 gate stack with poly-Si gate electrode, IEDM **2000**, 31-34	Dim Lee Kwong et al. /UT Austin	**126**	**34%**
Alternative dielectrics to silicon dioxide for memory and logic devices, Nature 406 (**2000**) 1032	Angus Kingon et al. / NCSU	**663**	**24%**

‘Green’ Flip-Chip Packages

Research Start: 1993

12 years

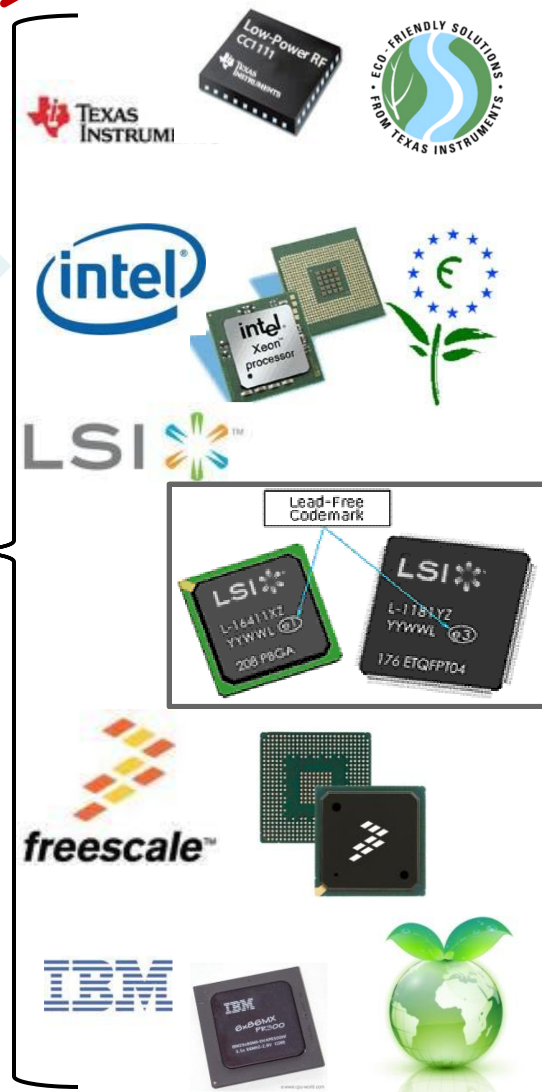
Commercialization: ~2005

Prof. King-Ning Tu / UCLA

Discussion of a ban within the EU on products sold containing Pb to begin in 2006

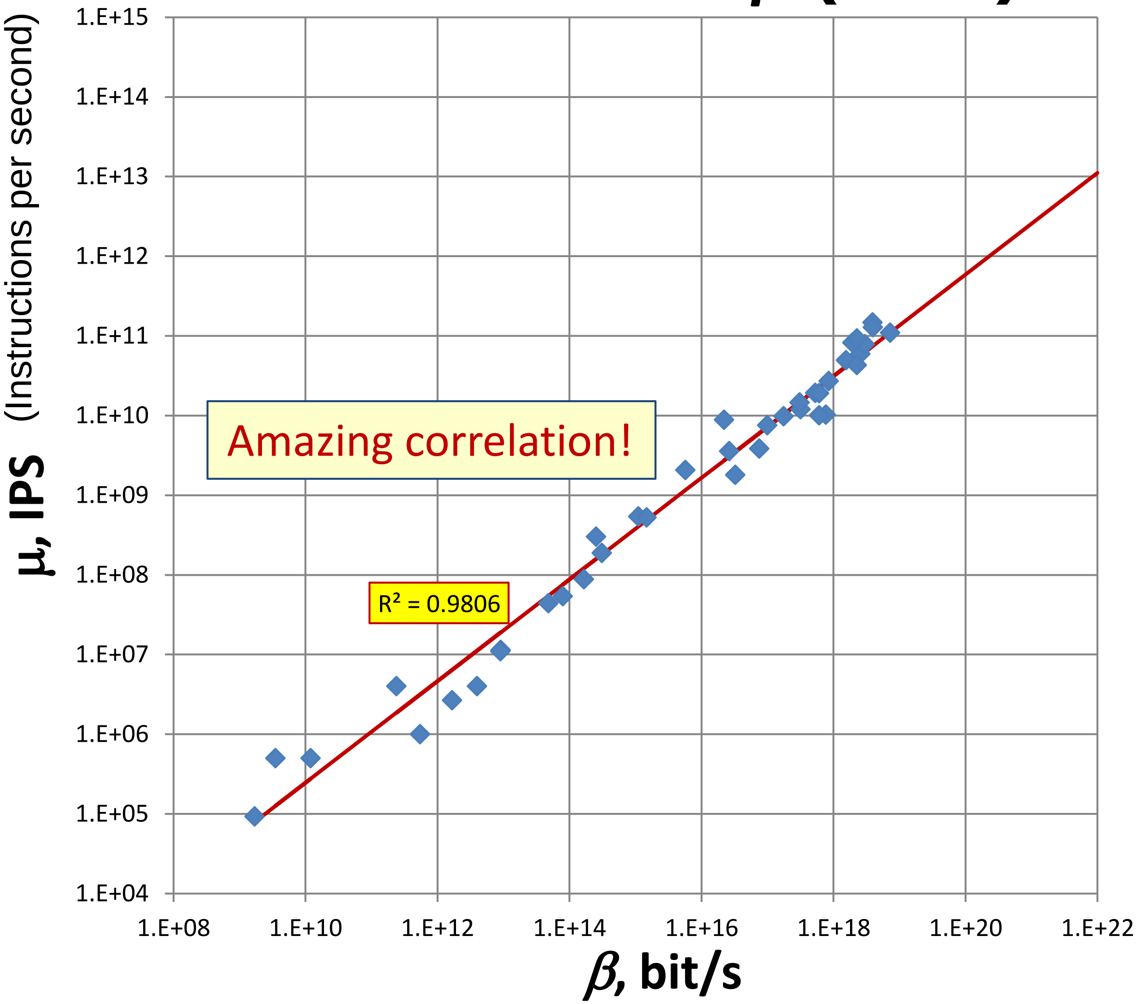
Replacing the Tin-Lead alloy within Flip Chip Packaging

- Pb-free solders
- Reliability (e.g. Whisker Growth)



- Innovation of a “Green” flip chip for use in consumer electronics applications.
- Successful transfer of Pb-free packaging to industry.
- 9 SRC-supported influential publications (>100 citations)
- **World-record # of citations for paper on packaging:**
    - K. Zeng and K. N. Tu, "Six cases of reliability study of Pb-free solder joints in electronic packaging technology", MATERIALS SCIENCE & ENGINEERING 38 (2002) 55-105
- ***578 citations; ~20% by industry***

Benchmark capability μ (IPS) as a function of β (bit/s)



$$\beta = N_{tr} \cdot f$$

aggregate indicator of technology capability

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Moore Physics

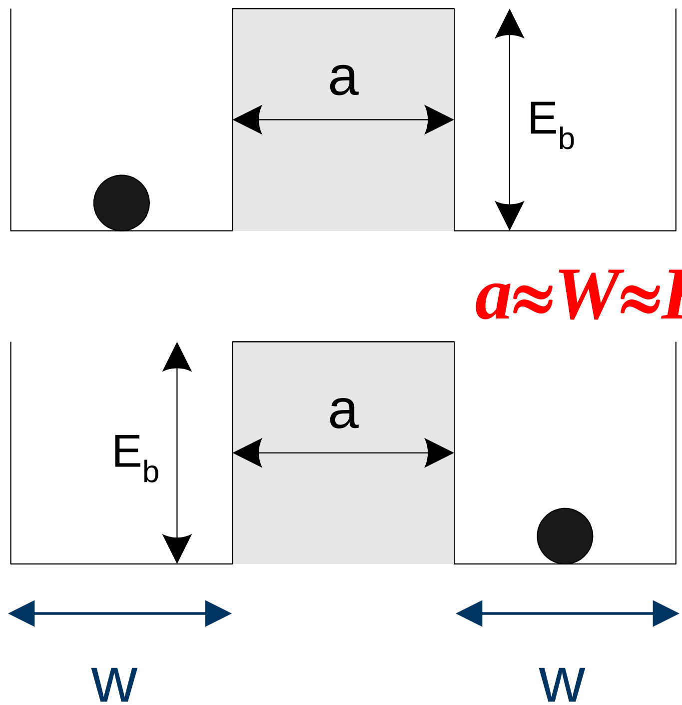
1) Barrier and tiling abstractions for device and interconnect models
2) Electron-based switch: A little Field Effect Transistor Physics
3) Electron-based nonvolatile memory: Scaling limits for Flash
4) 'Ultimate CMOS': A Summary

R. K. Cavin, P. Lugli and V. V. Zhirnov, "Science and Engineering Beyond Moore's Law", *Proc. IEEE* 100 (2012) 1720-1749

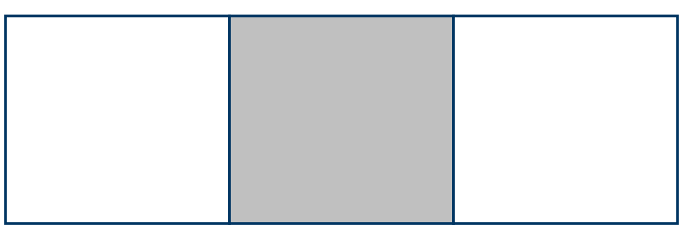
In collaboration with Technische Universität München

Two-well bit – **Universal Device Model**

Controllable energy barrier

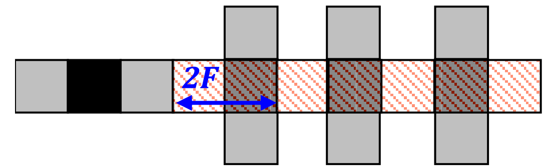


$a \approx W \approx F$



Generic Floorplan of a binary switch (tiling)

Tiling framework for limiting digital circuit analysis



$$\langle L \rangle = 6F$$

At the limits of scaling, the energy per tile is nearly the same for both devices and interconnect tiles

$$\boxed{E_{bit}(k) = \frac{1}{2} k \cdot E_{sw}}$$

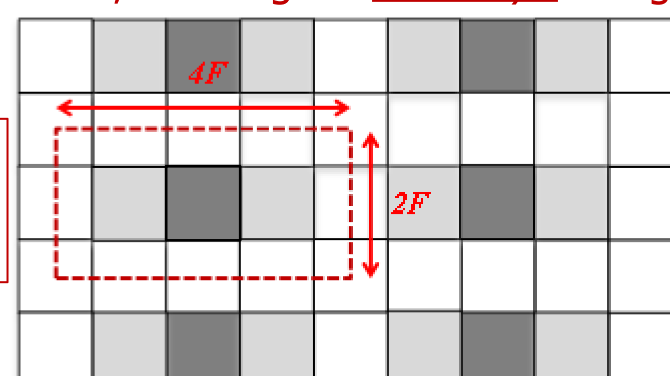
k - number of tiles per switch

k=3+6=9

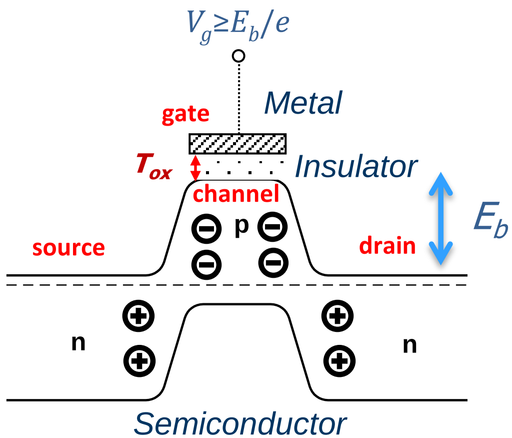
$$\boxed{E_{bit} = \frac{9}{2} E_{sw}}$$

Densest possible floorplan (*isolated* devices, allowing for *arbitrary* wiring

$$\boxed{n_{2D} = \frac{1}{8F^2}}$$



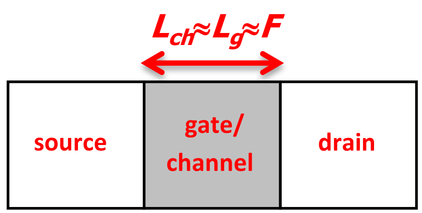
Electron-based Switch: A Little Field Effect Transistor Physics



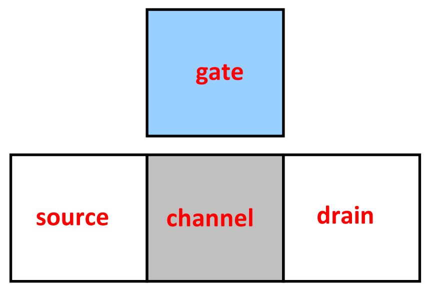
Optimized FET structure

$$\boxed{\frac{T_{ox}}{L_{ch}} \sim \frac{1}{30}}$$

Barrier tunneling renders FET feature sizes below about 5nm problematical



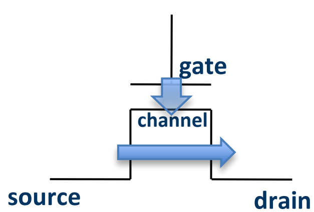
plan view



side view

L_g, nm	EOT, nm	J_{gate}, A/cm^2	V_{dd}	E_{sw}
10	0.60	2000	0.8	$3.36 \cdot 10^{-18}$
9	0.55	2220	0.8	$2.92 \cdot 10^{-18}$
8	0.55	2500	0.7	$1.89 \cdot 10^{-18}$
7	0.55	2860	0.7	$1.57 \cdot 10^{-18}$
6	0.50	3330	0.7	$1.21 \cdot 10^{-18}$
5.5	0.50	3640	0.65	$9.09 \cdot 10^{-19}$
5	0.50	4000	0.65	$7.65 \cdot 10^{-19}$
4.5	0.50	4440	0.65	$6.50 \cdot 10^{-19}$

ITRS FET performance goals below 10nm



$$\Delta x \Delta p \geq h$$

$$L \cdot \sqrt{2m^* E_b} \geq h$$

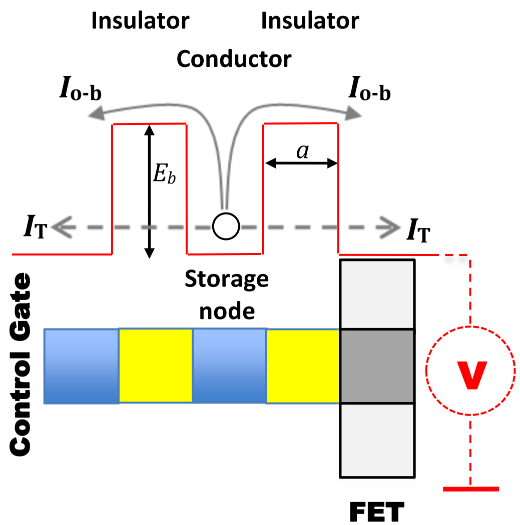
$m^* = 0.19 m_0$

$E_b = 0.5eV$

$$L_{crit} \sim \frac{h}{\sqrt{2m^* E_b}} \sim 4nm$$

Electron-based Nonvolatile Memory (Flash)

1. Basic Concept



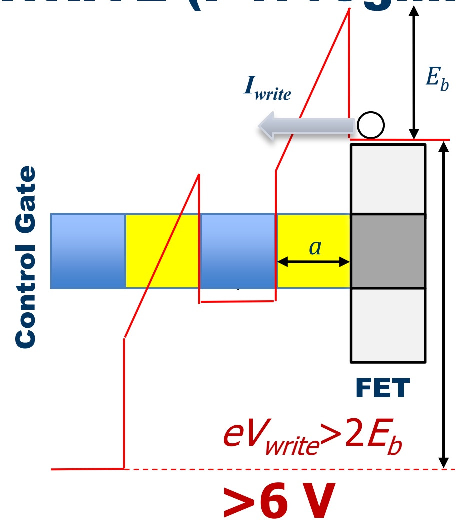
E_{bmin} >1.7 eV (>10 y retention)

$E_{b\,SiO2}$=3.1 eV

a_{min}~5 nm

$$L_{crit} \sim \frac{h}{\sqrt{2m^* E_b}}$$

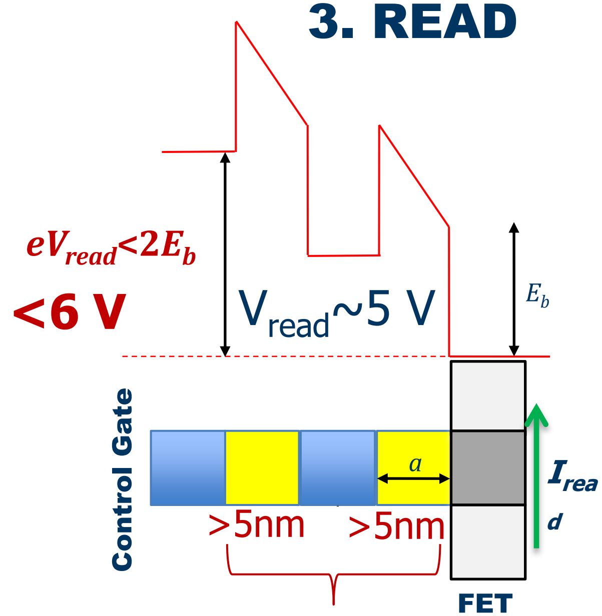
2. WRITE (F-N regime)



$V_{write\ min}$> 6-7 Volt (very slow)

V_{write} >**10-15 Volt** (ms-μs)

3. READ

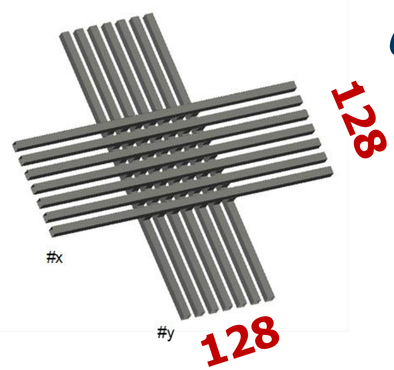


T_{ox}>10nm

$$\boxed{\frac{T_{ox}}{L_{ch}} \sim 1}$$

F_{min}>10nm

4. Array



C_{line}~ 10^{-14} F

$$E \sim C_{line} V^2 \sim 2.5 \cdot 10^{-13}\, J$$

‘Ultimate CMOS’: A Summary

- The reliance of CMOS and many other proposed information technologies on electron charge to support their operations places them at risk as features scale downward into the few nanometer regime
  - tunneling becomes detrimental to performance

- Heavier particle mass could, in principle, allow for further scaling

$$L_{crit} \sim \frac{h}{\sqrt{2m^* E_b}}$$

An Example:
Minimal Memory Element

What is the smallest volume of matter needed for a memory cell?

Al Fazio, Intel Fellow (ITRS ERD meeting, Barza, April 2010)

$$L_{crit} \sim \frac{h}{\sqrt{2m^* E_b}}$$

Information carriers

Flash

Electrons — $V_{min} \sim 10^3\ nm^3$

Atoms — $V_{min} < 10\ nm^3$

ReRAM

V. V. Zhirnov, R. K. Cavin, S. Menzel, E. Linn, S. Schmelzer, D. Bräuhaus, C. Schindler and R. Waser, "**Memory Devices: Energy-Space-Time Trade-offs**", *Proc. IEEE* 98 (Dec. 2010) 2185

In collaboration with RWTH Aachen Univ / Jülich Res. Ctr.

V. V. Zhirnov, R. Meade, R. K. Cavin, S. Menzel, and G. Sandhu, "**Scaling Limits of Resistive Memories**", *Nanotechnology* 22 (June 2011) 254027

In collaboration with Micron Technology, Inc.

Space-Action Principle for Memory

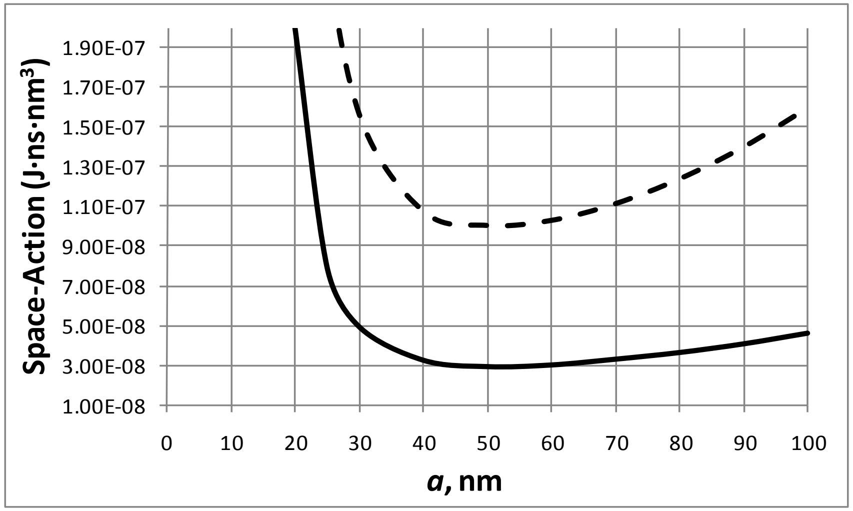
$$Energy \times time \times Volume = \min$$

$$E \cdot t \cdot V = \min \qquad E \cdot t \cdot L = \min \qquad E \cdot t \cdot N_{at} = \min$$

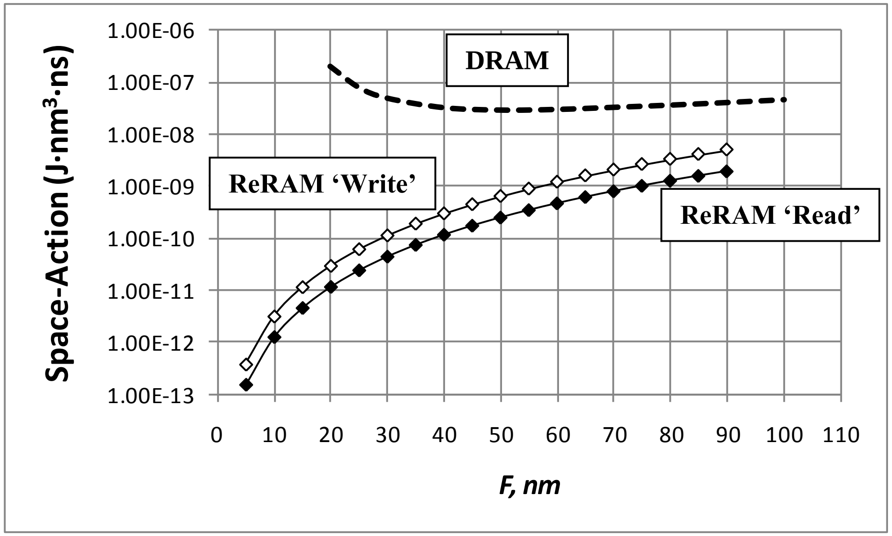
The Least Action principle is a fundamental principle in Physics $E \cdot t = \min$ **($\geq h$)**

Plank's constant
h=6.62x10^{-34} Js

Scaling optimization for DRAM based on minimal space action



DRAM vs. ReRAM



Memory Devices:
Space-Time-Energy Trade-offs

	$N_{carriers}$	V_{stor}, nm^3	E_w, J	t_w, ns	*Space-Action,* J-ns-nm^3	Critical Component	
DRAM	10^5	10^5	10^{-14}	1 ns	$\sim 10^{-7}$-10^{-8}	Storage Node	
Flash	10	10^3	10^{-16}	10^3 ns	$\sim 10^{-9}$	Sensor	FET
STT-RAM	10^5	10^3	10^{-14}	1 ns	$\sim 10^{-10}$	Selector	FET
ReRAM	100	3	10^{-17}	1 ns	$\sim 10^{-13}$	Selector	FET or 2-t select device

Constraints by remote sensor not considered

$$Energy \times time \times Volume = \min$$

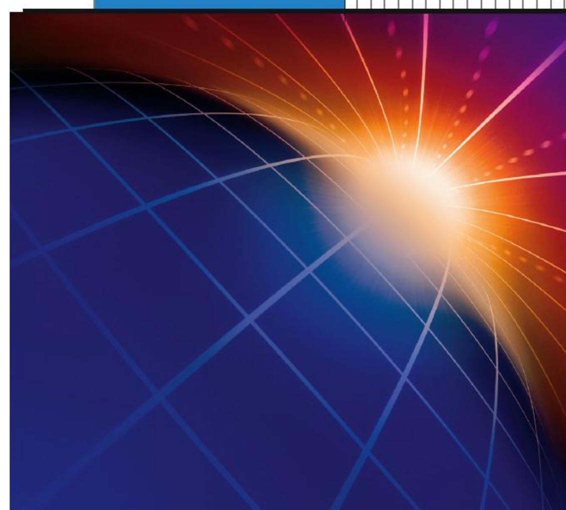
Architectural Implications

- Advances in memory technologies could drive the emerging data-centric chip architectures
  - *Nanostores* - Chips consisting of multiple 3D-stacked layers of dense nonvolatile memory with a top layer of power-efficient processor cores
- *Nanostores* architectures could be an important direction for the future of information processing.

- Ultra-fast data access
- Flattening memory hierarchy
- LOW ENERGY!

Matches with future data-centric workloads

COVER FEATURE



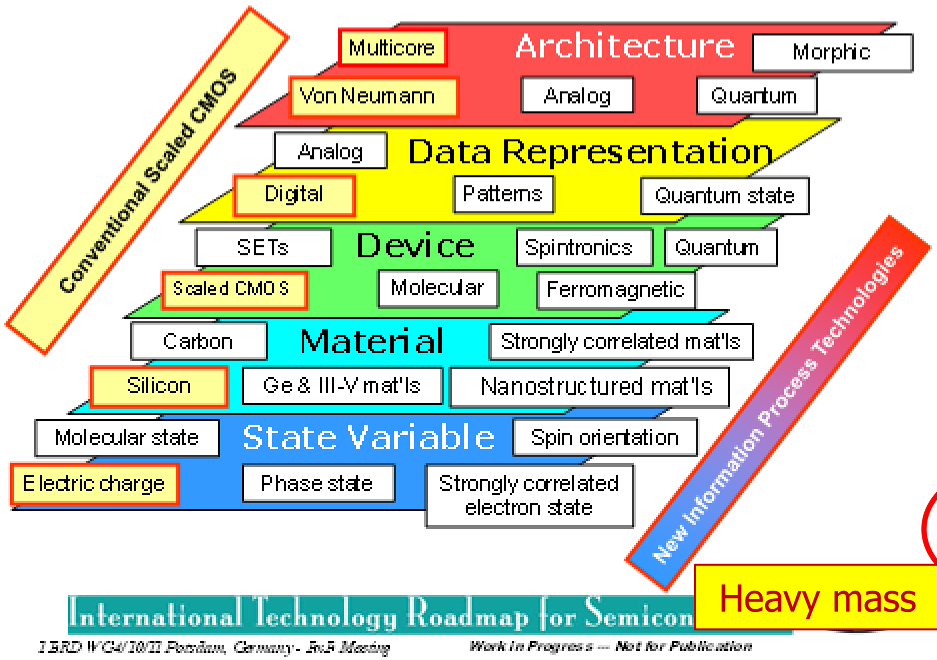
From Micro-processors to Nanostores: Rethinking Data-Centric Systems

Parthasarathy Ranganathan, *HP Labs*

***Computer*, Jan. 2011**

Beyond Moore: Two Views

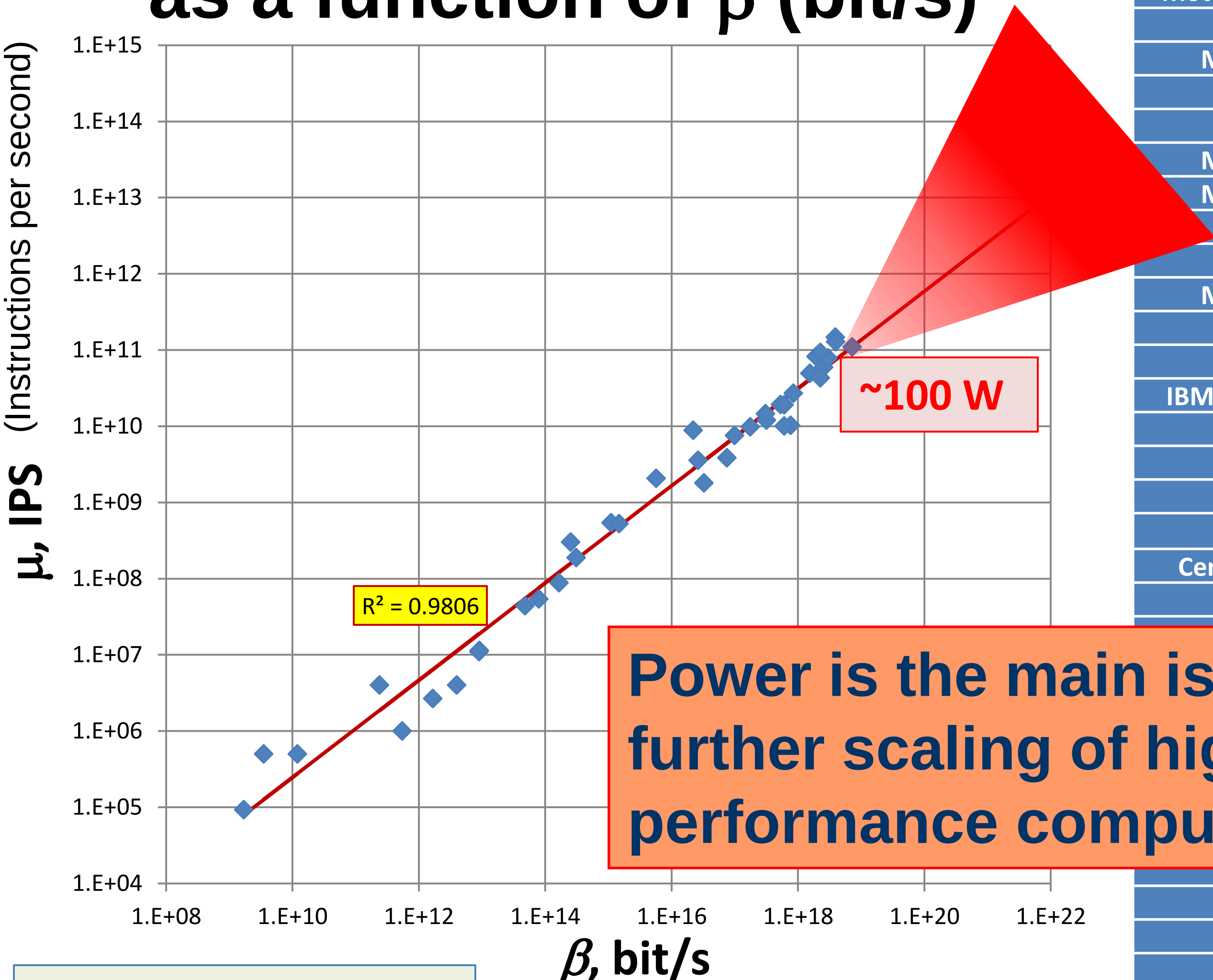
A Taxonomy for Nano Information Processing Technologies



Device	Physical Entity	Properties		
		Control Variable	State Variable	Output Variable
FET – Novel Materials (III-V, Ge, carbon-based, etc.)	Electron	Charge	Charge	Charge
SpinFET	Electron	Charge	Spin	Charge
Spin-Torque	Electron	Spin	Spin	Charge
Spin-Wave	Electron	Spin Waves	Spin	Charge Photon
Tunneling Transistor	Electron	Charge	Charge	Charge
Molecular switch	Electron or Atoms	Charge	Charge	Charge
NEMS	Atoms	Charge	Position	Charge
Atomic Switch	Atoms	Charge	Position	Electron
Memristor	Atoms	Charge	Charge,	Electron
Magnetic Cellular Automata	FM Domain	Magnetic dipole	Spin	FM Domain
Moving Domain Wall	FM Domain	Magnetic Dipole	Spin	FM Domain
Multi-Ferroic Tunnel Junction	FM Domain	Spin	Charge	Electron
Optical or Plasmonics	Atoms or Electrons	Charge	Optical Density	Photons
Thermal Transistor	Phonons	Thermal Energy	Temperature	Phonons

There are no evident replacement technologies yet

Benchmark capability μ (IPS) as a function of β (bit/s)



Power is the main issue for further scaling of high-performance computing

$$\beta = N_{tr} \cdot f$$

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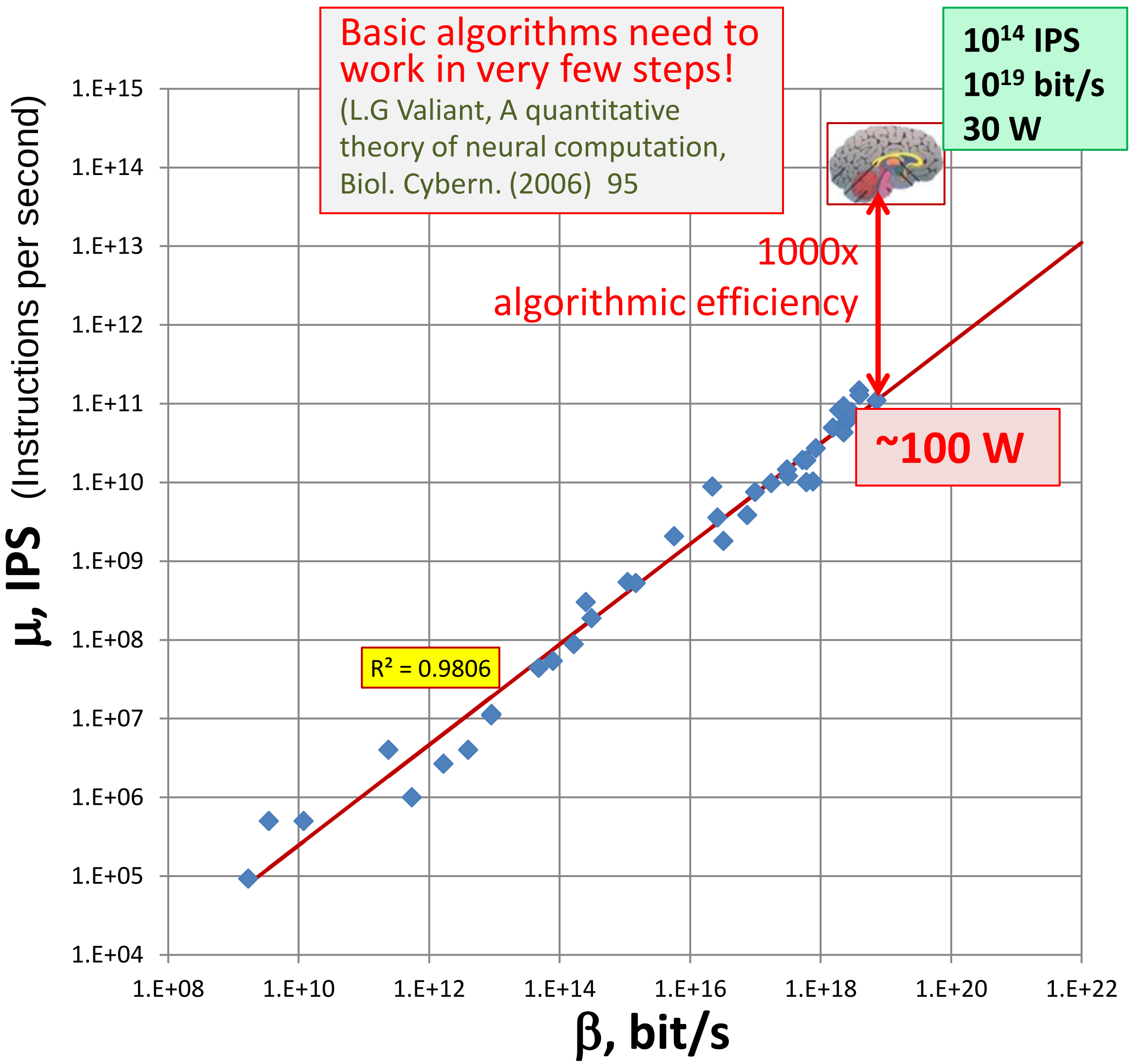


Estimates of computational power of human brain:

Binary information throughput:

$\beta \sim 10^{19}$ **bit/s**

Gitt W, "information - the 3rd fundamental quantity", Siemens Review 56 (6): 36-41 1989

(Estimate made from the analysis of the control function of brain: language, deliberate movements, information-controlled functions of the organs, hormone system etc.

Number of instruction per second

$\mu \sim 10^{8}$ **MIPS**

H. Moravec, "When will computer hardware match the human brain?" J. Evolution and Technol. 1998. Vol. 1

(Estimate made from the analysis brain image processing)

What can we learn about information processing from Nature?

Breakthrough Technology Challenges for next decades

- From fundamental physics it seems likely that the scaling of MOSFET devices will end in the few nanometer regime.
  - Industry is working with universities to develop replacement technologies
  - Some brilliant ideas are emerging but---
  - There are no evident replacement technologies yet

- Are there other models for information processing technologies that offer the promise to sustain Moore's Law?

- We suggest that inspiration can be derived from organic systems, i.e., at the intersection of chemistry, biology, and information processing

Way Beyond Moore: Information Processing By Nature

1) Living cell as an *in carbo* information processor
2) Information content of a material system/living cell
3) Essential parameters of an *in carbo* processor: Logic and Memory hardware
4) *In silico* vs. *in carbo* information processors: A comparison

V. V. Zhirnov and R. K. Cavin, "Microsystems for Bioelectronics" (Elsevier 2010)

R. K. Cavin, P. Lugli and V. V. Zhirnov, "Science and Engineering Beyond Moore's Law", *Proc. IEEE* 100 (2012) 1720-1749

In collaboration with Technische Universität München

Specifications of a Human Cell

- 10 μm overall size
- 10^7 biochemical operations per second
- 1 pW power consumption
- 30,000 node gene-protein molecular network with nanoscale devices.
- 20kT per molecular operation
(vs. 10^4 -- 10^5 kT in advanced nanoelectronics)
- 0.36 nm between base pairs in DNA. Average protein is 5 nm.
- Functions: sensing, communication, actuation, feedback regulation, molecular synthesis, molecular transport, detoxification, defense, self assembly of organism from a single embryonic cell.

The cell is a marvel of nanotechnology

Biology computes efficiently and precisely with noisy and unreliable components on noisy real-world signals.

Rahul Sarpeshkar, Analog Circuits and Biological Systems Group,
Massachusetts Institute of Technology

Living Cell as an General Purpose Processor

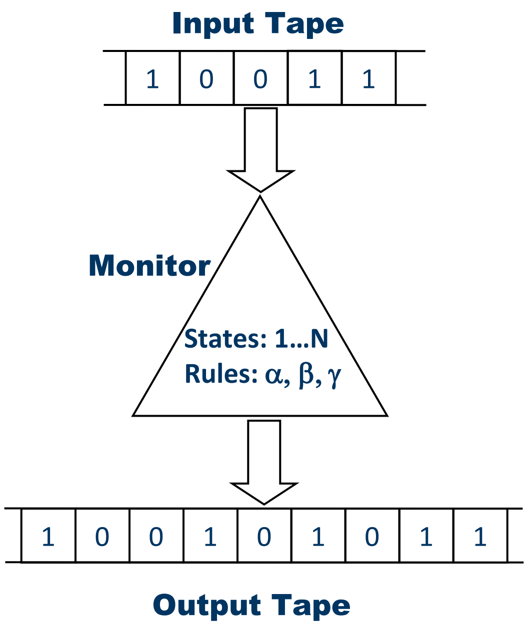
- Single-cell living organisms, such as bacteria, have the formal attributes of a Turing Machine, i.e. a machine expressing a program.
- In fact, the cell can be thought of as von Neumann's Universal Constructor, as the cell *expresses the output of its information processing on the matter* constituting the building blocks of the cell itself
  - *computer making computers*.
- In addition, single-cell organisms have been shown to exhibit the ability to learn, the ability to communicate with each other, various complex social behavior, etc.

A. Danchin, Bacteria as computers making computers, FEMS Microbiol. Rev. 33 (2009) 3

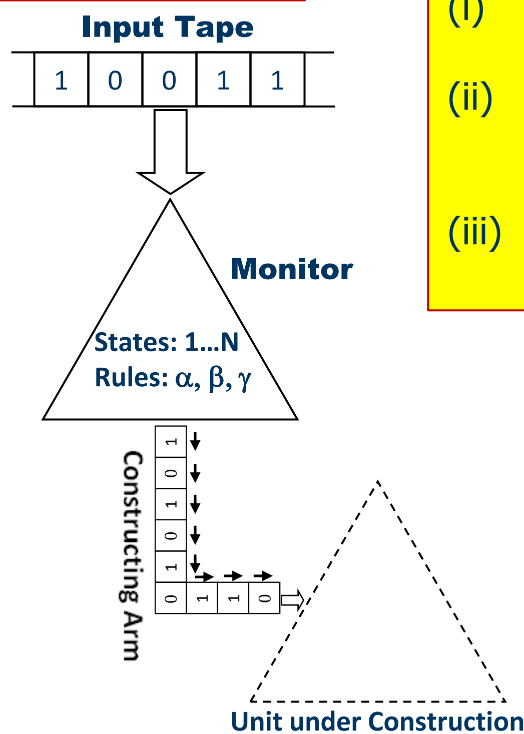
Abstract Information Processors

The input information for the *in carbo* information processor comes from two sources:
(i) from the cell's surroundings via a number of *sensors*
(ii) by the cell's internal *memory* unit, the DNA molecule.

The output information of the *in carbo* processor has at least three components:
(i) assembly of matter to make a new cell,
(ii) actuation of motility organs, such as flagella, in response to external stimuli
(iii) communication with other organisms.



Turing Machine

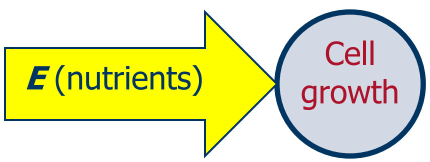


von Neumann Universal Constructor

Consider a computer with the task of controlling the assembly of a structure from building blocks

Information Content of Bacterial Cells: Theory vs. Experimental Estimates

- An upper bound estimate: ~3×10¹² bits
- Experimental estimates: 10^{11}-10^{13} bits
  - Experimental estimates of the information content of living cells were made based on *microcalorimetric measurements*.
  - It has been concluded that the major consumption of energy during a cell's reproduction cycle arises from the correct placement of molecules within the cell. W. W. Forrest, "*Entropy of microbial growth*", *Nature* 225 (1970) 1165-1166



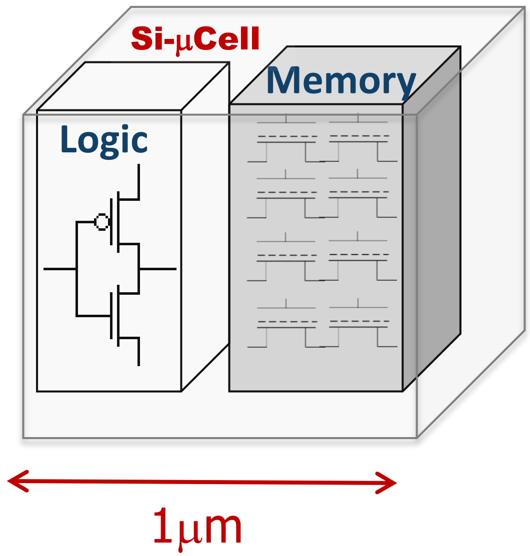
$$\Delta E = T\Delta S + P\Delta V + \sum_i \mu_i \Delta N_i$$

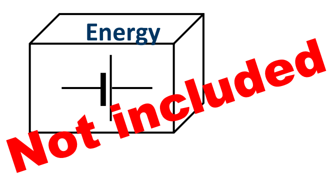
$\Delta I = -\Delta S$

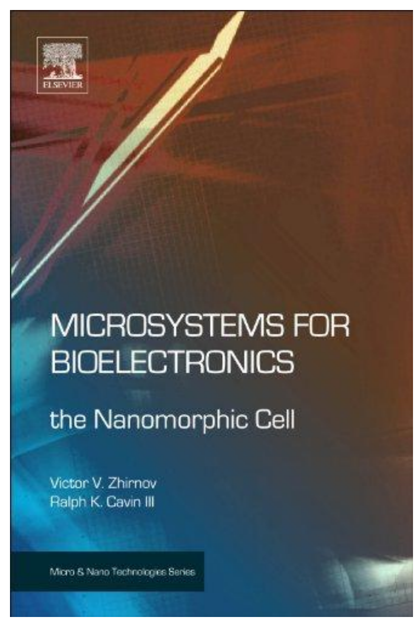
- In the following, the conservative edge of the estimated range is used: $\sim 10^{11}$ bits
  - (the number of *output bits*)

In-Silico versus *In-Carbo*

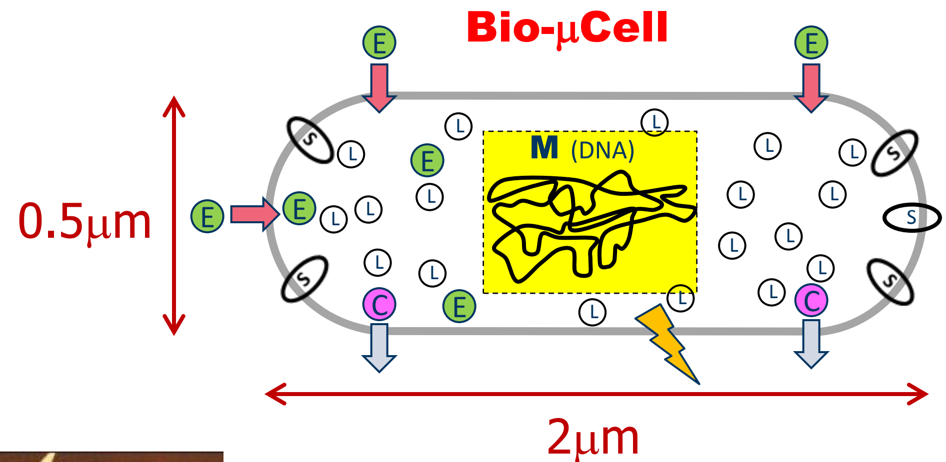
In silico







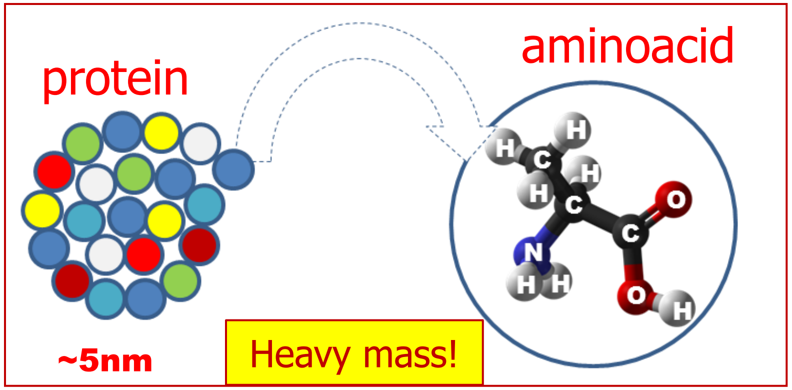
In carbo

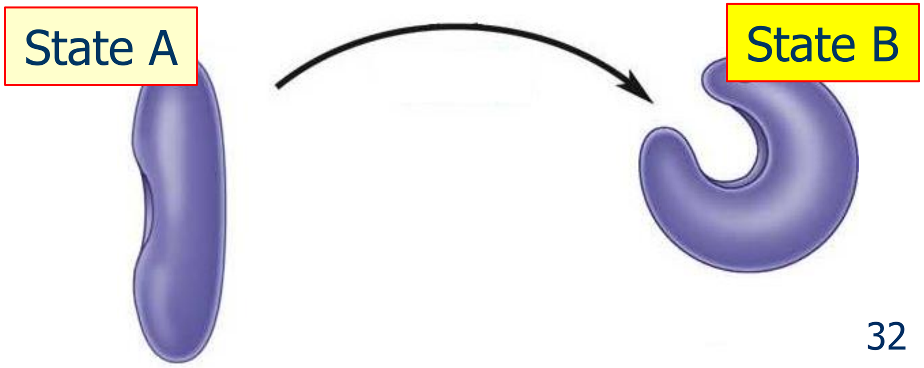


- (E) 'Energy molecules', e.g. glucose
- (L) 'Logic molecules', e.g. proteins
- (C) 'Communication molecules'
- (S) Sensor proteins

Logic Hardware

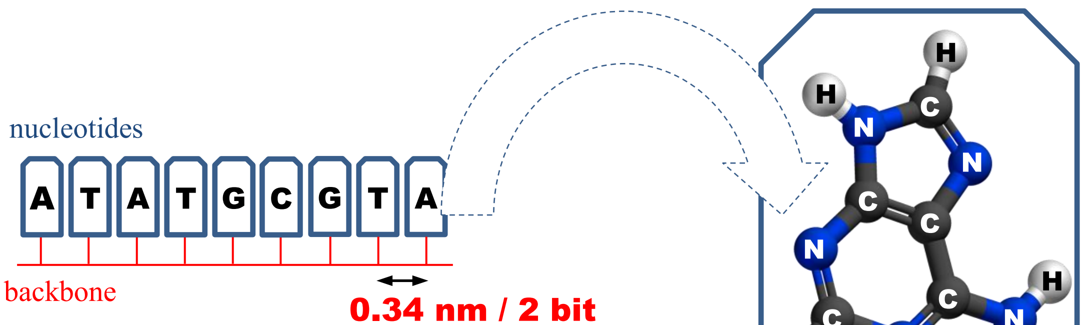
- Many proteins in cells have as their primary function the transfer and processing of information
  - are regarded as logic elements of the in-carbo processor
  - the proportion of components devoted to computational networks increases with the complexity of the cell, and are absolutely dominant in humans
- Proteins can alter their 3D structural shapes (*conformation*) in response to external stimuli,
  - different conformations can represent different logic states.
  - These *nanomechanical* changes form a state variable – **conformon**
  - Different *nanomechanical* conformations of these protein devices are recognized by other elements of the in-carbo cell circuit by a process based on *selective affinity* of certain biomolecules with given conformational states (e.g. electrostatic attraction)





DNA Memory Characteristics

- All data about structure and operation of a living cell are stored in the long DNA molecule
    - Nonvolatile memory
- DNA coding uses a **base-4** (quaternary) system
    - The information is encoded digitally by using four different molecular fragments, to represent a state: adenine (A), cytonine (C), guanine (G), and thymine (T).



10^{19} bit/cm^3

Electronic NVM:
F_{min}~10nm/1bit

<10^{16} bit/cm^3

DNA is <u>NOT</u> a read-only memory

DNA memory operations

<u>READ</u>

- *Multi-access capability* by distinct computing units

<u>WRITE</u>

Vertical gene transfer - exact copying of the parental DNA

Lateral (horizontal) gene transfer :

(1) direct uptake ('swallowing') of a naked DNA by a cell,

(2) by a virus,

(3) by direct physical contact between two cells.

Essential parameters of a Bio-μCell Processor (*E.coli* example)

Devices		
In Carbo **'device' count**		***Function***
DNA size	4.6×10^6 bp=**9.6 Mbit**	Nonvolatile memory
Number of RNA/cell	222,000	Memory interface
Number of cytoplasmic proteins	1,000,000	1) Logic processor 2) Signal processor 3) Metabolic functions*
Number of ribosomal proteins	900,000	I/O interface
Number of logic 'devices' (Proteins and RNA)	**>1,000,000**	1) Logic processor 2) Signal processor 3) Memory interafce 4) I/O interface
Number of all proteins	3,600,000	1) Logic processor 2) Signal processor 3) Metabolic functions* 4) Structural functions*
Timing		
Time for cell replication	40min=2400s	
Energetics		
Energy stored in cell	$\sim 2 \times 10^{-12}$ J	
Power dissipation	1.4×10^{-13} W	

Example:

DNA memory access

1. Address specification

DNA-binding proteins act as *gates* to the specific snippets of DNA. The *signaling network* (logic circuitry) regulates the state of the DNA-gating proteins that determine when and where a DNA snippet (a gene) is activated.

2. Information retrieval

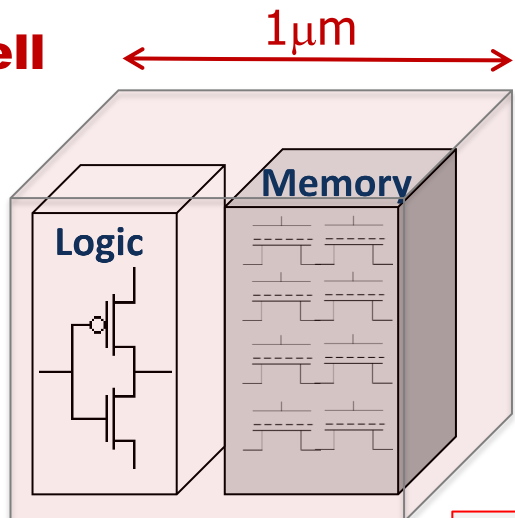
RNA polymerase protein - memory *read head* moves along the specified snippets of DNA and copies its information into pieces of messenger RNA (mRNA).

3. Information transfer

The mRNA transfers the information to the ribosomes (output devices).

In-Silico versus *In-Carbo*

Si-µCell

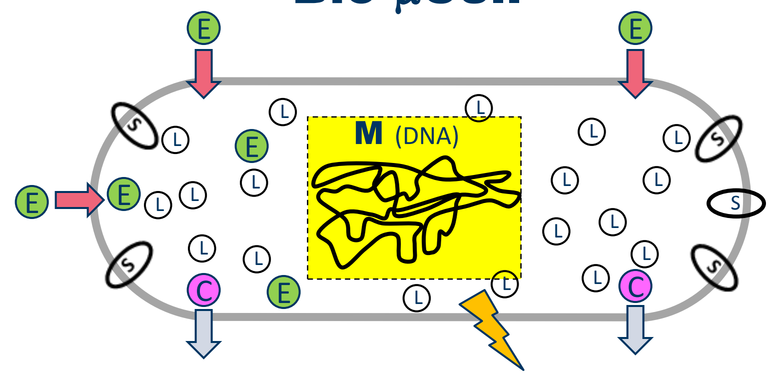


Memory:	~10^4bit
Logic:	~300–150,000 bit
Power:	~10^{-7} W
Heat:	~1 W/cm^2
Total energy/task*:	**~10^{-2} J**
Task time*:	510,000 s ~ 6 days

10^{16} bit/cm^3

10^{17} bit/cm^3

Bio-µCell



Memory:	10^7 bit
Logic:	>10^6 bit
Power:	10^{-13} W
Heat:	10^{-6} W/cm^2
Total energy/task*:	**10^{-10} J**
Task time*:	2400s=40min

10^{19} bit/cm^3

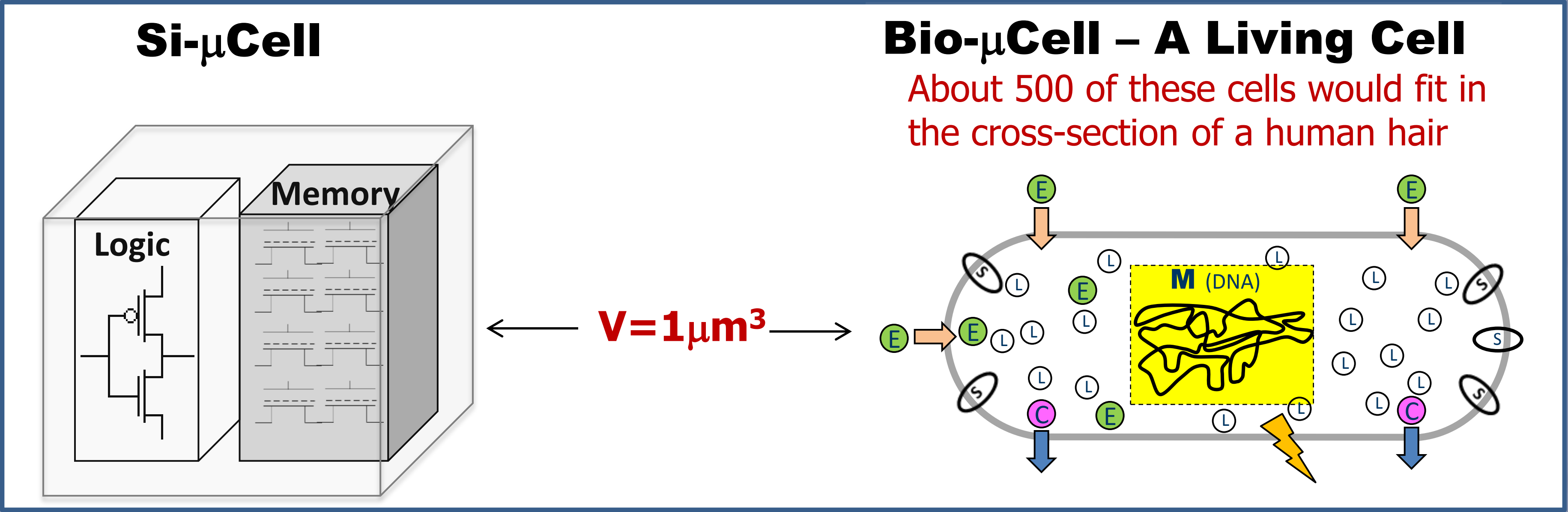
10^{18} bit/cm^3

*Equivalent to 10^{11} output bits

A Si-µCell fundamentally cannot match the bio-µCell in the operational energy

R. K. Cavin, P. Lugli and V. V. Zhirnov, "Science and Engineering Beyond Moore's Law", *Proc. IEEE* 100 (2012)

Nature Has Been Processing Information for a Billion Years



Our studies show that the Si-μCell cannot match the Bio-μCell in the density of memory and logic elements, nor operational speed, nor operational energy:

Memory: 1000x more
Logic: >10x more
Power: 1000,000x **less**
Algorithmic efficiency: 1000x more

Lower-hanging fruit?

Example I: DNA Memory

Sciencexpress 16 August 2012

Next-Generation Digital Information Storage in DNA

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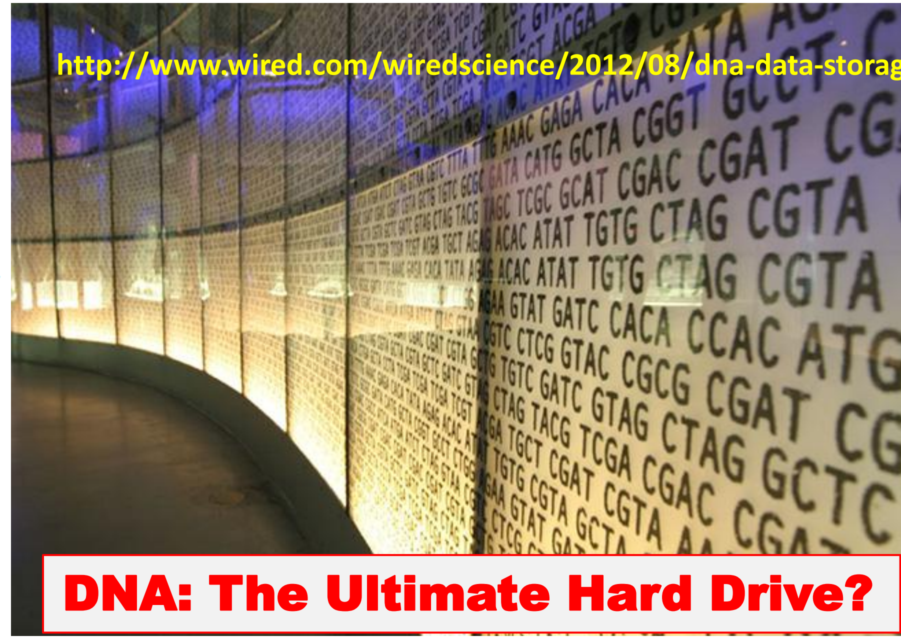
*To whom correspondence should be addressed. E-mail: sri.kosuri@wyss.harvard.edu



DNA: The Ultimate Hard Drive?

Researchers **stored an entire genetics textbook** in less than a picogram of DNA — one trillionth of a gram — an advance that could revolutionize our ability to save data.

5.27×10^6 bit

DNA memory can be stable ~ 100y+

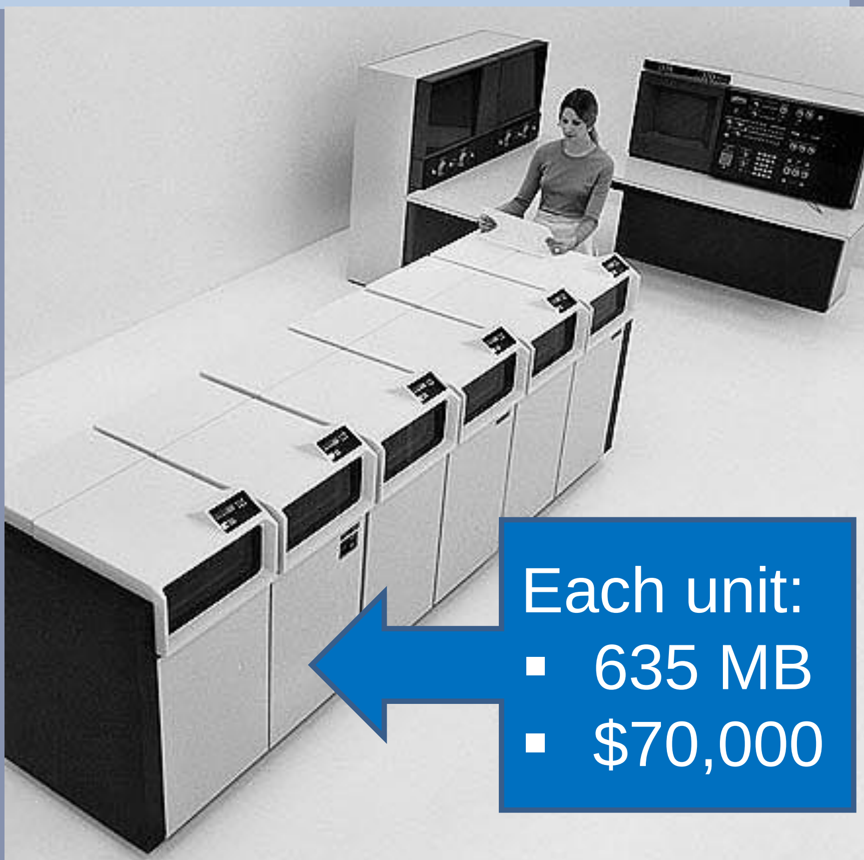
HARDWARE: Agilent Oligo Library Synthesis microarray platform

- Agilent Technologies, a spin-off of Hewlett-Packard (1999), originally a semiconductor company, which became now a global company offering products & services in communications, electronics, semiconductor, test and measurement, life sciences and chemical analysis industries.
  - Example of a successful convergence of semiconductor and bio industries

What 30 years of progress can enable

The iPod was un-imaginable circa 1980…

1982: Best available storage technology was the **IBM 3350**



Each unit:
- 635 MB
- $70,000

80Gb cost
$9,000,000 !!!
in 1982 dollars

126 IBM 3350's =
storage in
1 iPod

2012

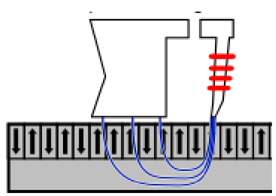
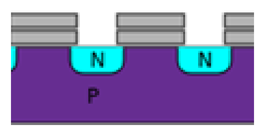
iPod(5G)
80GB

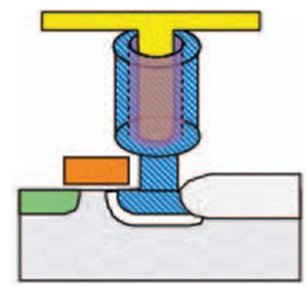
80Gb cost
<$100
in 2012 dollars

DNA-Inspired Memory

DNA-inspired memory

- DNA volumetric memory density far exceeds **(1000x)** projected ultimate electronic memory densities
- Potential for very <u>low-energy</u> memory access
- **Goal:** Demonstrate a miniaturized, on-chip integrated DNA storage




	HardDiskDrive	NAND flash	DRAM	DNA in cell
Read/Write latency	3-5 ms/bit	~100μs/bit	<10 ns/bit	<100μs/bit
Endurance (cycles)	unlimited	10^4-10^5	unlimited	unlimited
Retention	>10 years	~10 years	64 ms	>10 years
ON power (W/GB)	~0.04	~0.01-0.04	0.4	$<10^{-11}$
Aerial Density	~ 10^{11} bit/cm^2	~ 10^{10} bit/cm^2	~ 10^9 bit/cm^2	n/a
Volumetric Density	n/a	10^{16} bit/cm^3	~10^{13} bit/cm^3	10^{19} bit/cm^3

Conclusions

- CMOS/Moore's Law is facing downstream physical limits
  - There are no evident replacement technologies
  - Power is the main issue for further scaling of high-performance computing

- Several approaches seeking new devices whose operations are not dependent on electron charge are being explored
  - Beyond Moore

- All is not lost! We have just begun to mine the secrets of information processing used by nature
  - If equivalent technologies can be invented to mimic nature, there are many opportunities to enhance information processing at an exponential rate

Messages

- (1) Developments of more complex and powerful information processing devices are mandatory
- (2) A typical latency time from 1st publication to 1st production is **about 12 years**
- (3) Today there are many diffused nanoelectronic endeavors, but
  - We need to drive investments toward most promising approaches
- (4) Due to limited global resources, the cost of wrong decisions is high
- (5) We need to develop mechanisms to focus research programs and to filter unlikely technologies, e.g.
  - e.g. ITRS ERD provides Potential/Risk assessments for beyond-CMOS solutions