4th Workshop: Elaboration of Recommendations

Introduction and summary of the previous workshops

Clivia M Sotomayor Torres (ICN)

OUTLINE

About NANO-TEC

- Context
- Objectives

ACTIVITIES

- Methodology
- Workshops
- Project web site

OUTCOME SO FAR

- Summary of discussions to date
- Lessons learnt

CONTEXT

The JU AENEAS covers the whole of nanoelectronics research, ***except*** the Beyond CMOS Domain.

Beyond CMOS research is carried out mainly in academic and research organisations.

Existing consortia cover several domains including Beyond CMOS, which lacks visibility in the ERA and in the EU Framework program.

Given the existence of the JU AENEAS and the room for the EU to fund Beyond CMOS research, a community with long-term research interests in nanoelectronics is needed.

Of key importance is to address the design issues in Beyond CMOS and build a bridge between technologies and design or, better still from novel device concepts through technologies, systemability, to design for applications.

POSITION of NANO-TEC

Nanofabrication networks, national and EU
MyFab, RENATECH, Micronova, DIMES, TNO, Tyndall, IMEL, NANOLITO, ….

Design Networks
EDA centrum
RD-ACCESS

NANO-TEC

Technology National and EU Networks & projects
FinNano (FI)
NANOFUNCTION,SINANO
CNANO & CNFM (F)
Linneqs & Gigabit Wave (SE)
nanoTHERM (ES)
ENI2

Interest groups and JTI
ENIAC Scientific Community Council
AENEAS & CATRENE
ITRS & SRC (USA)

OBJECTIVES AND PARTNERS

To identify the next generation of (emerging) device concepts and technologies for ICT.

To build a joint technology-design community to coordinate research efforts in nano-electronics.

REMIT of NANO-TEC

Thematically:

Puts emphasis on Beyond CMOS Devices and Design

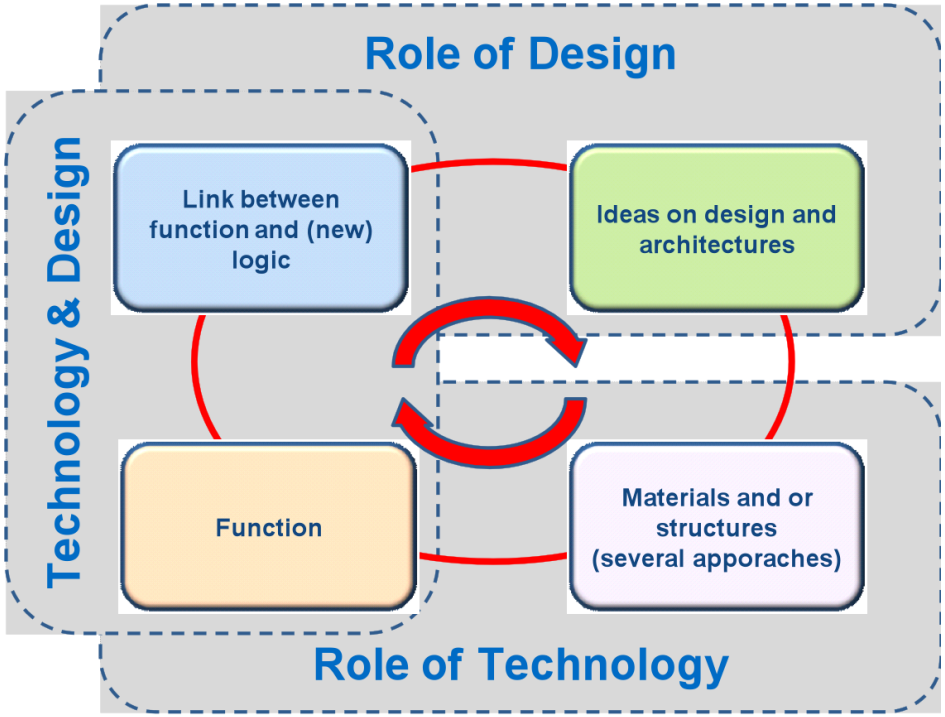
As Instrument:

Organises and coordinates discussions and makes recommendations

Actors:

Mainly from academia and research organisations. Industry via Advisory Board.

ACTIVITIES

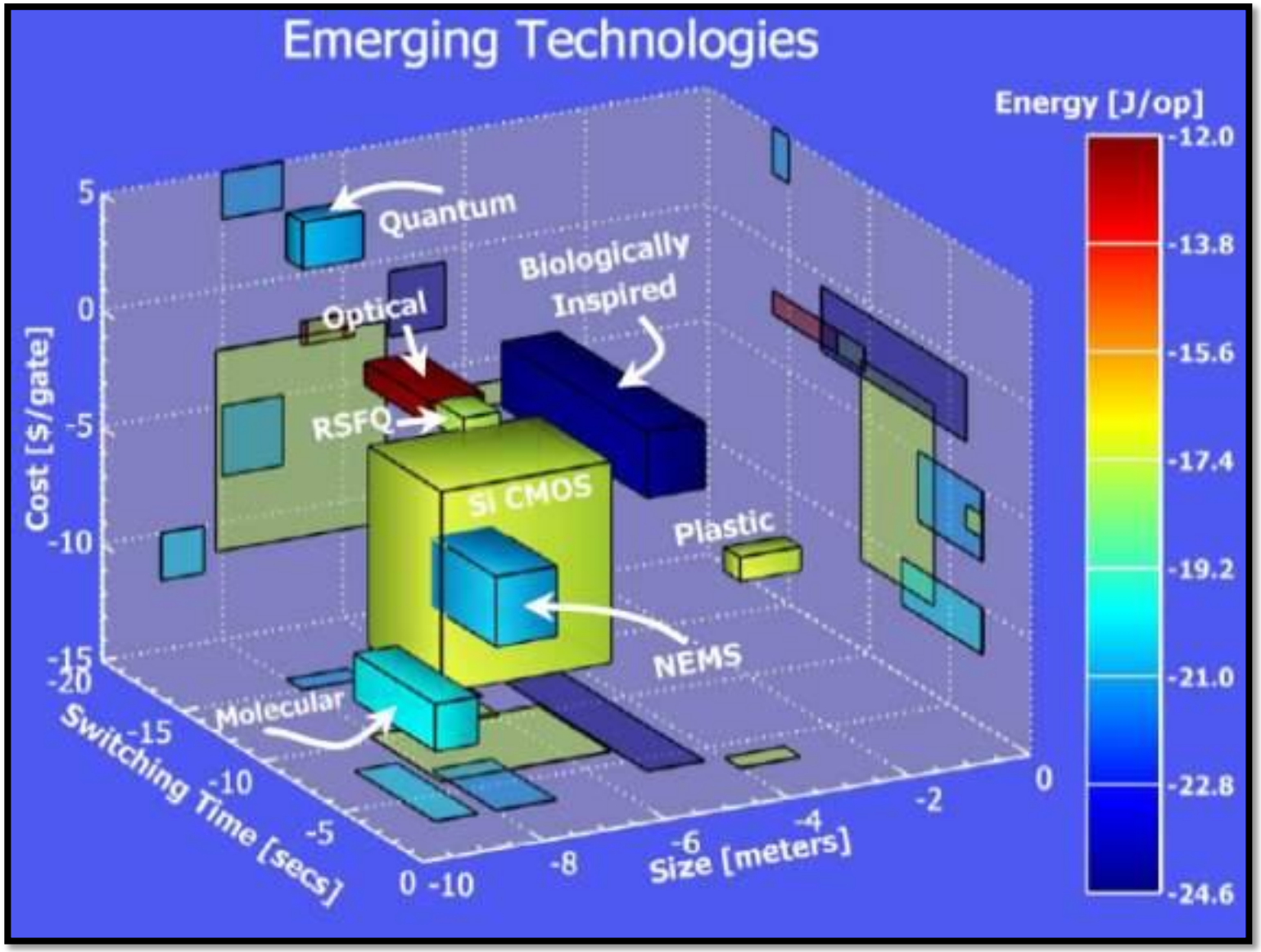


4 workshops with invited experts on Beyond CMOS devices, benchmarking and a SWOT analysis of new devices.

A state-of-the-art web platform for working groups, enabling discussions fora, meetings, communications and access to an information repository.

A report on Emerging Nanoelectronics.

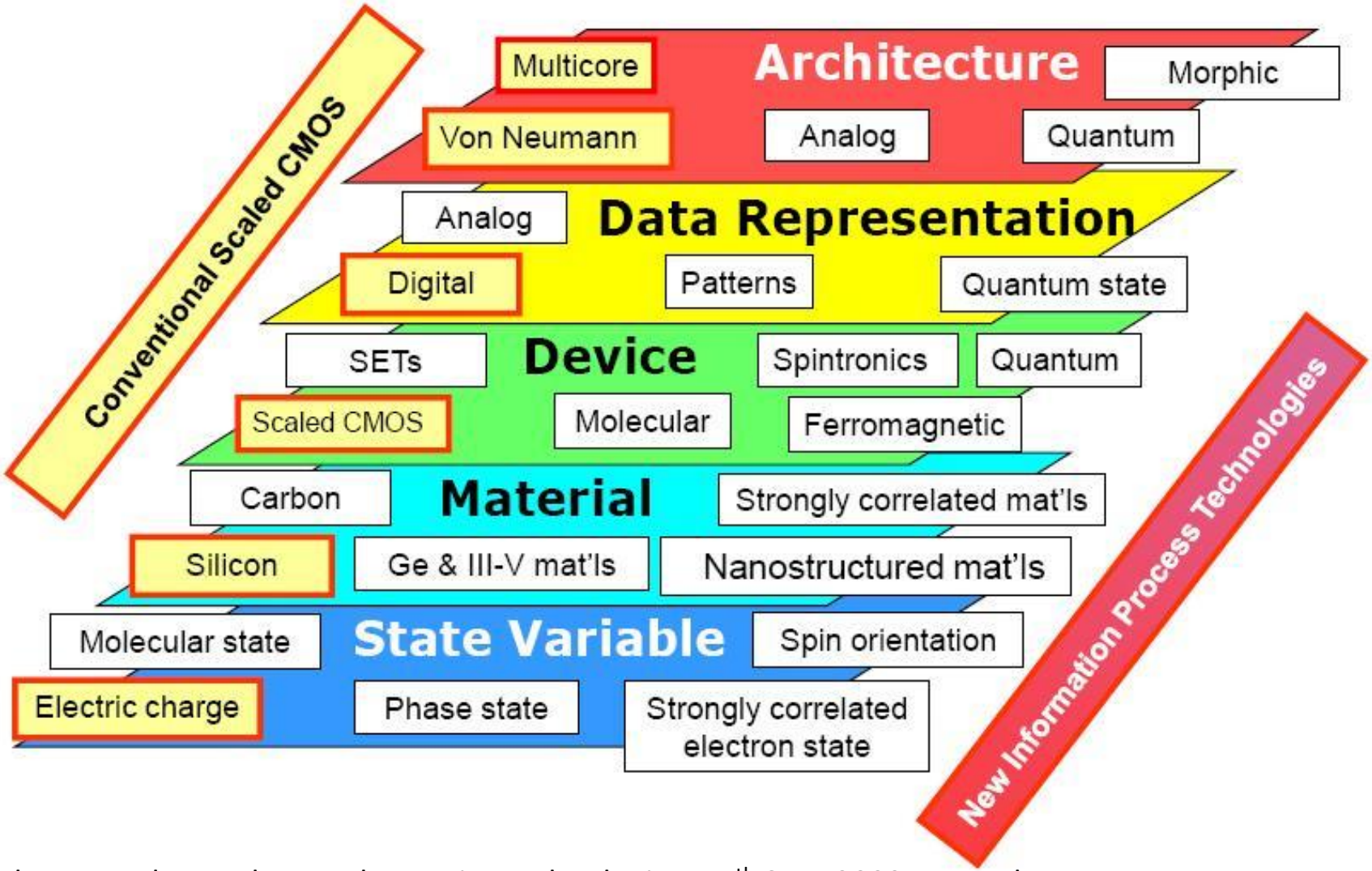
BEYOND CMOS TECHNOLOGIES a la ITRS



(Reproduced after ERD ITRS)

BEYOND CMOS TECHNOLOGIES a la EU

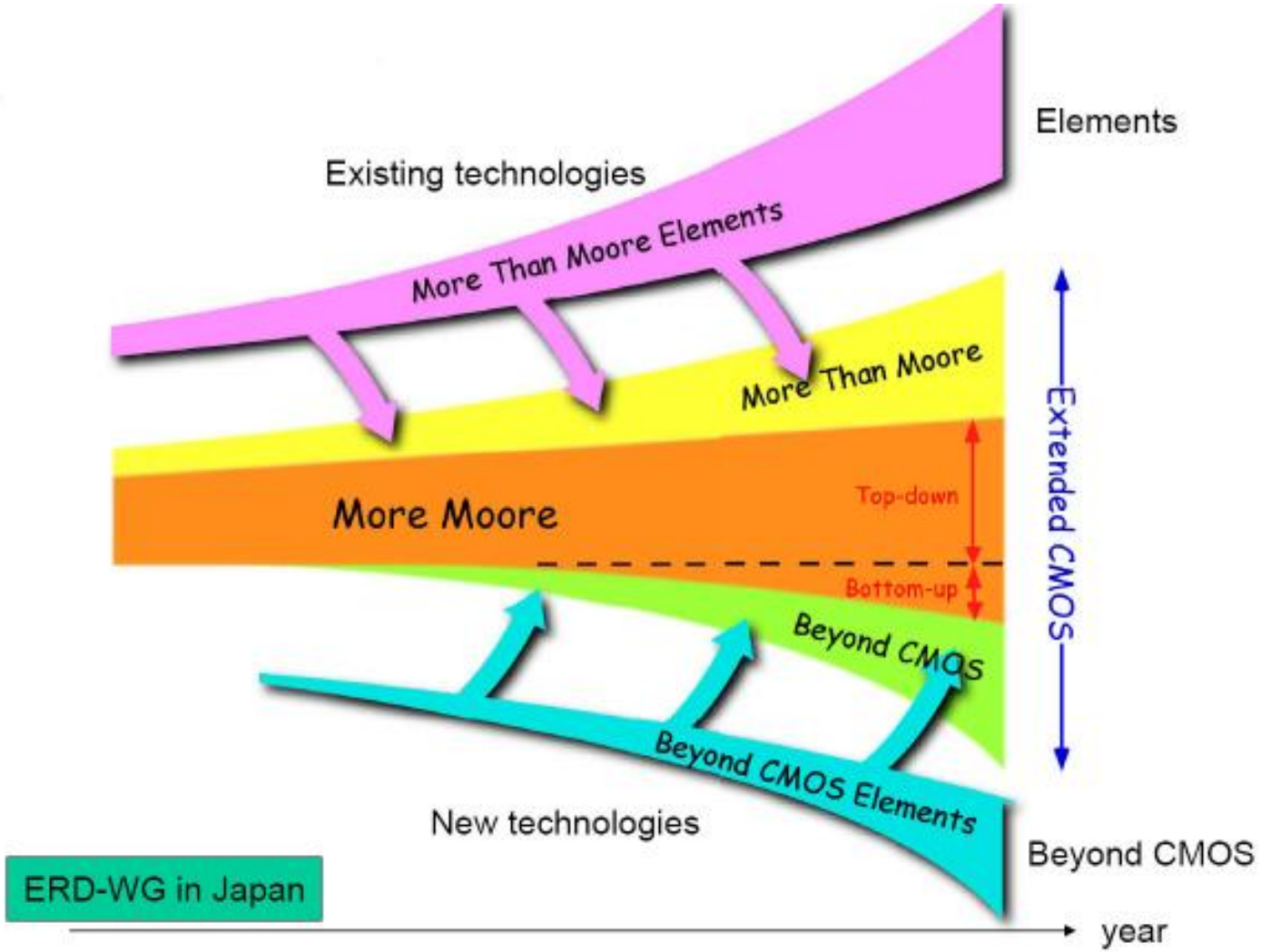
New information processing devices and architectures



FP7 Workshop on Advanced Nanoelectronics Technologies, 11th Sept 2009, Brussels

PERCEIVED ROLE OF BEYOND CMOS TECHNOLOGIES

ITRS-ERD vision on the role of More than Moore and Beyond CMOS elements to foRM future extended CMOS platforms.



Currently vision stops at "extended CMOS"

FP7 Workshop on Advanced Nanoelectronics Technologies, 11th Sept 2009, Brussels

METHODOLOGY

Workshop series:

- Gather perspectives from a wide range of experts from Europe and beyond
- Arrange for speaker, discussant and rapporteurs
- Document each workshop with presentations and reports
- Build on previous workshop(s)

Test new methodologies to discuss Beyond CMOS:

- Benchmarking
- SWOT analysis

Web-based platform:

- Project Communications
- Workshop organisation
- Document repository
- Working Group discussions

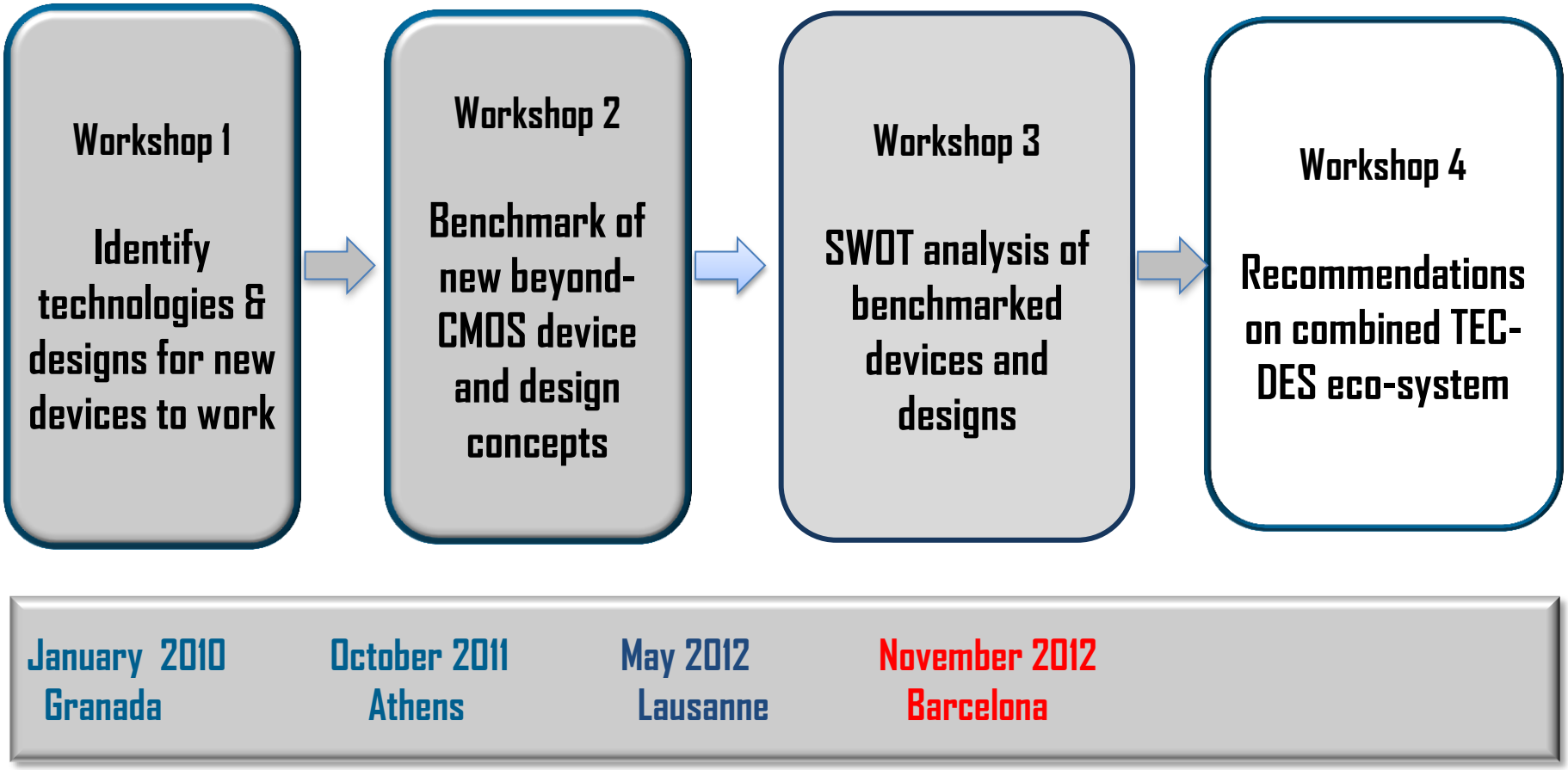
And, above al,l … find ways to involve the design community.

Dissemination:

- Incorporate the design community and involve the nanoelectronics one.

NANO-TEC Workshops timeline

Main mechanism to reach suitable recommendations



TECHNOLOGY SELECTION

WORKSHOP 1 Winter 2011 (non-exhaustive list) :

- SRC experience
- **Si-based Nanoelectronics**
- **Compound semiconductor based electronics**
- Carbon-based electronics
- Spintronics & Magneto-electronics
- Molecular electronics / Quantum Computing
- Analogue mixed Design
- **Panel: Bridge to Design**

Nanowires and MEMS/NEMS left for WS2

WS1 CONCLUSIONS & RECOMMENDATIONS (non-exhaustive)

Address cross-cutting issues:

Power consumption, manufacturability and cost vs. performance.

New technologies issues:

Device functionality at the nanoscale needs to be strengthened
Increasing need for new architectures
Alternative concepts to do computation.

Beyond CMOS design issues:

Variety of nanodevices and materials
Novel circuits and architectures needed to exploit fully nano components.
Mode of operation of such devices?
Multi-scale approach needed in to describe realistic systems.

Some recommendations:

Graphene and molecular electronics need targeted programs.
Spintronics needs a targeted program on architectures and systemability.

WORKSHOP 2:

- **Guardian Angels & Graphene Flagships**
- Graphene
- Spintronics (Memories)
- Molecular electronics
- MEMS
- Solid-state based Quantum Computing
- Nanowires
- Memristors
- **Panel Discussion on Design**

Working Groups benchmarked technologies

Benchmarking Beyond CMOS Devices

Technology	[Wires, graphene, MEMS etc… please insert name]
Gain **Signal/Noise ratio** **Non-linearity**	
Speed **Power consumption**	
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	
Other specific properties	
Manufacturability **(Fabrication processes needed, tolerances etc.)**	
Timeline **(When exploitable or when foreseen in production)**	

Benchmarking exercise in the US

NRI Switch Candidates

- 15 nm LV CMOS
- 15 nm HV CMOS
- Excitonic FET
- MTJ Logic Switch
- All Spin Logic
- Graphene PN Junction
- Electronic Ratchet
- Graphene thermal logic
- BDD Architecture
- Nanomagnet logic
- gnrTFET
- InAs TFET
- e-Struct. Modulation Trans
- RAMA
- BiSFET
- RIEFET
- HetTFET
- Spin Wave
- MTJ/STT
- Spin Torque Amplifiers
- Magnetic Domain Wall Logic
- Graphene spin transport
- MOTT Device
- Spin-Injection Hall Effect
- Few Spin Device

Bernstein et al., Device and Architecture Outlook for Beyond CMOS Switches, Proc. IEEE 98 (2010) 2169.

Benchmarking exercise in US

Circuits used to Benchmark Device

- Inverter with a fanout of 4
- 2-input NAND with a fanout of 1
- 32b adder

Bernstein et al., Device and Architecture Outlook for Beyond CMOS Switches, Proc. IEEE 98 (2010) 2169.

BENCHMARKING in NANO-TEC

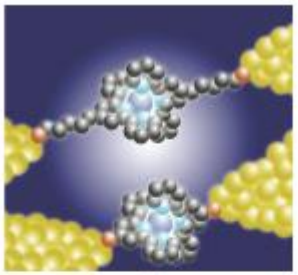
Aim to a broader scope:

- No direct comparison with CMOS
- Allow for other concepts in addition to digital switches
- Challenge the design community

Example: MOLECULAR ELECTRONICS (1/3)

D. Vuillaume, 2nd NANO-TEC Workshop

Single molecule electronics

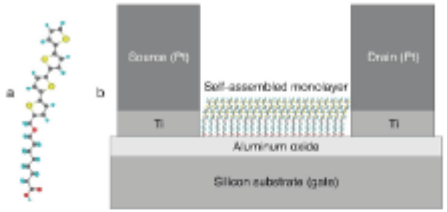


L < a few nm
t < a few nm

basic science
knowledge development

no foreseen applications
in a reasonable time-scale

Self-assembled molecular electronics



L ~ tens nm - µm
t < a few nm

basic science
knowledge development

possible applications
foreseen

Thin film molecular electronics

L > µm
t > few 10 nm

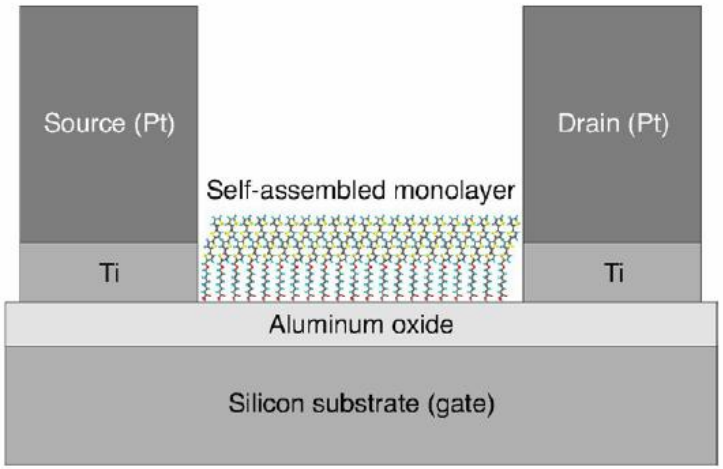
plastic electronics
(OLED, OFET, OPV)

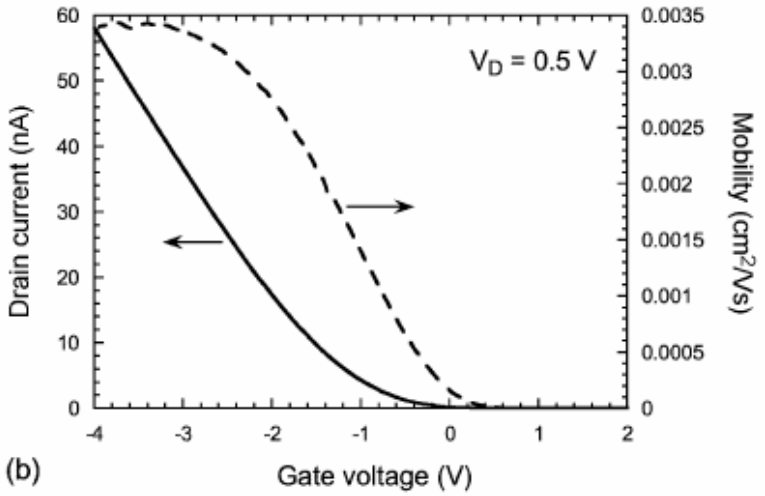
some products already
commercialized

Example: MOLECULAR ELECTRONICS (2/3)

SAMFET: Self-Assembled Monolayer Field Effect Transistor

- Built by immersing a Si substrate in a solution of liquid crystalline molecules, resulting in a monolayer of self-assembled semi-conductive molecules.
- Molecules stand upright. Conduction takes place by charges jumping from one molecule to the other.
- As the length of the SAMFET increased, its conductivity decreases exponentially.
- The SAMFET can be used to make sensors that give a large signal triggered by a small change.

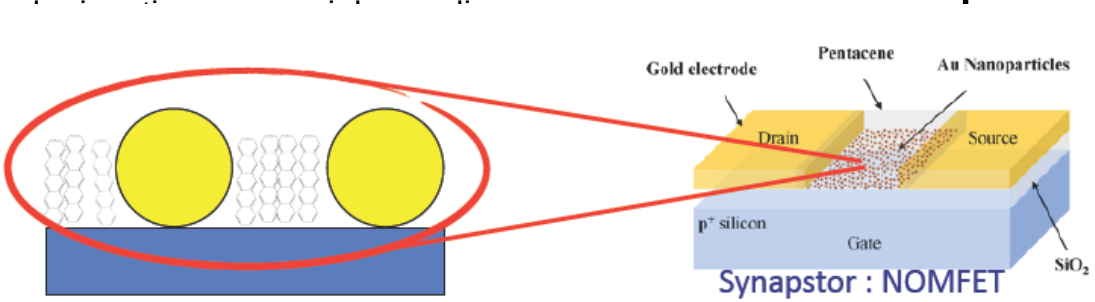




Example: MOLECULAR ELECTRONICS (3/3)

Benchmarking Beyond CMOS Devices

Technology	Molecular Electronics D. Vuillaume, CNRS & University of Lille
Gain **Signal/Noise ratio** **Non-linearity**	Ok with SAMFET (to be optimized), 2-terminal junction: low current Noise not yet studied (a few publications) Mole
Speed **Power consumption**	Low Low
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	Mole funct
Other specific properties	Almost infinite combination of molecules, adjustable by chemistry, specific design (1 molecule = 1 function)
Manufacturability **(Fabrication processes needed, tolerances etc.)**	Solution processing, compatible with flexible substrate. Defect control? Large variability (but not a problem if we envision artificial neural networks)
Timeline **(When exploitable or when foreseen in production)**	> 5 – 10 years (if ever?)



WS2 CONCLUSIONS & RECOMMENDATIONS (non-exhaustive)

General recommendation:

- Refine the benchmarking methodology to cover a wider range of Beyond CMOS technologies and design approaches.
- Memory or switching functions of FET-like devices found too restrictive.
- In some cases benchmarking needs to be application-specific.

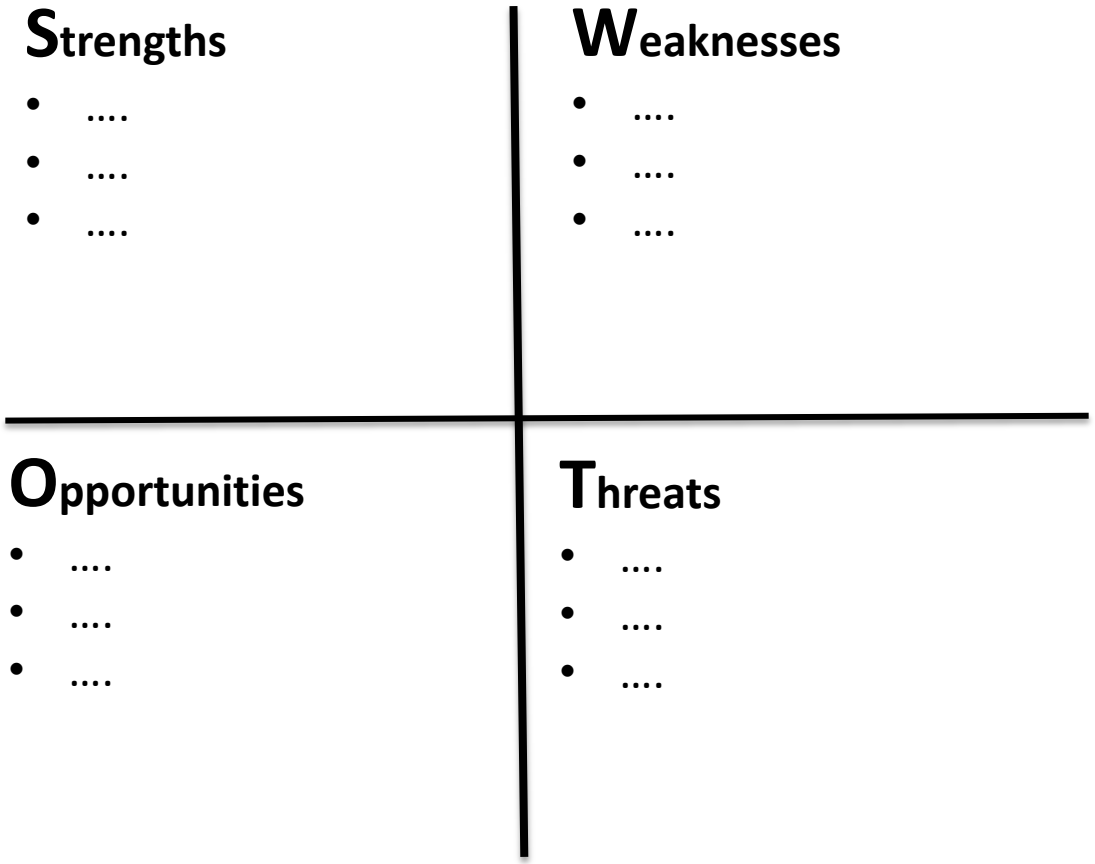
Common specific recommendation:

- The design component must be built-in from the very beginning.
- Make use of the 3rd dimension, eg, MEMS
- Initially seek to integrate on a Si platform, eg. Quantum computing
- Variability and systemability seen as main challenges.
- Thermal issues and stability need to be addressed.
- Design tools need to incorporate multi-physics and multi-scale approaches.

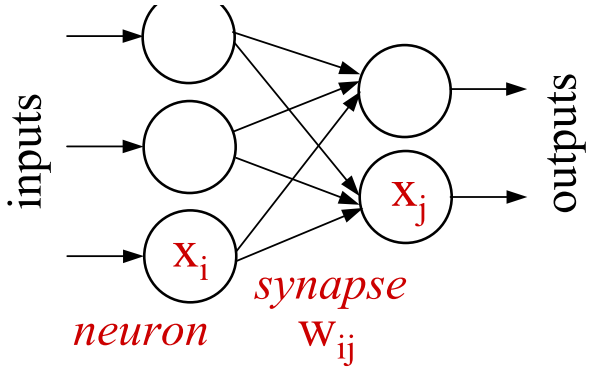
SWOT Analysis

WORKSHOP 3:

- Graphene
- Spintronics
- Molecular electronics
- MEMS
- Solid-state based Quantum Computing
- Nanowires
- Neuropmorphic Computing
- **Panel Discussion "From technology to Applications"**



EXAMPLE: SWOT Analysis of Neuromorphic Computing



- **synapses should have a memory : the weights have to be stored**
  (non-volatility)

- **synapses should be small : 10^4 synapses/neuron in human brain**

- **synapses should be plastic : synaptic plasticity**

Biological synapse : change in strength in response to either use or disuse of transmission
Artificial synapses : the weigths w_{ij} should be adjustable

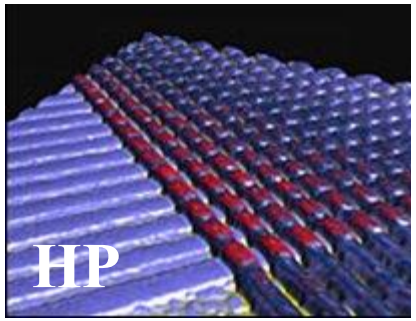
a learning rule specifies how to adjust the weights for a given input/output pair

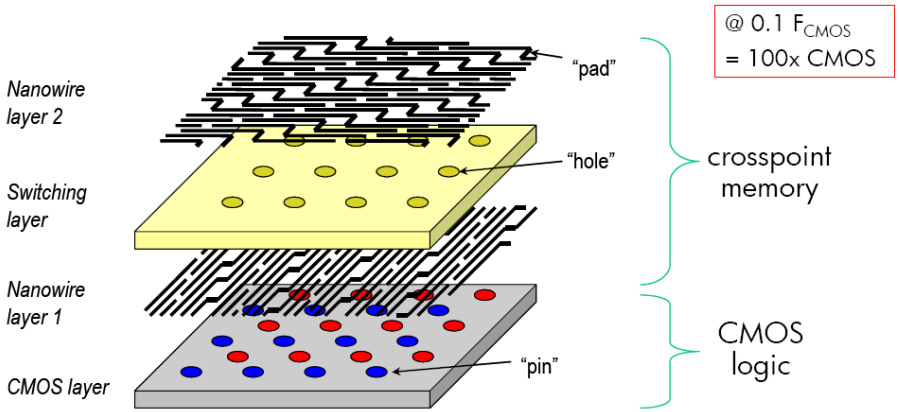
J Grollier, 3rd NANO-TEC workshop

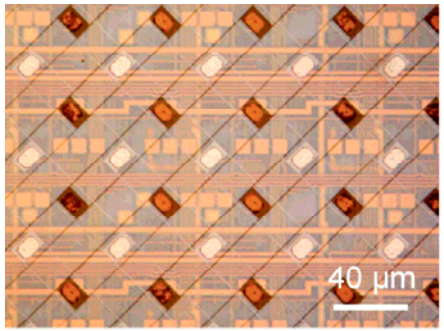
Example: SWOT Analysis of Neuromorphic Computing

- **Memristors have a memory :**
  they directly store the synaptic weights *(w = conductance)*
- **Memristors are small *(< 50 x 50 nm²)***

ex : CMOS "neurons" + memristive "synapses"







Xia *et al.,* Nanoletters (2010)

memristor crossbar arrays

No demonstration yet of operational mixed memristor/CMOS cognitive chip

J Grollier, 3rd NANO-TEC workshop

EXAMPLE: SWOT Analysis of Neuromorphic Computing

Strengths
- speed
- low power
- defect tolerance

Weaknesses
- interconnect
- programming
- design : to be invented
- control device stochasticity

Opportunities
- use differently memory devices
- accelerators for specific functions to interface in heterogeneous multi-core architectures
- adaptive architectures, able to compute with incomplete data → robotics, unmanned vehicles etc.

Threats
- the density cannot be reached
- the interconnection problem cannot be solved
- heat management

J Grollier, 3rd NANO-TEC workshop

WS3 CONCLUSIONS & RECOMMENDATIONS (non-exhaustive)

Considering all technologies discussed:

Strengths	Weaknesses
• Application perspectives • Building blocks for innovation in nanoelectronics • European industrial/academic ecosystem	• Physical constraints • Compatibility issues with conventional technology • Reliability, variability
Opportunities	**Threats**
• Design of circuits and systems • 3D integration of multifunctional systems • Industrial/academic cooperation	• Gap to industrial needs? • 'CMOS competition' • Manufacturability

BRIDGING THE GAP BETWEEN TECHNOLOGY & DESIGN

Based on panel discussions and presentations:

- Strands reflect current approaches in the design community
- Material → property → function → application
- Modelling → design
- Device → systemability → system

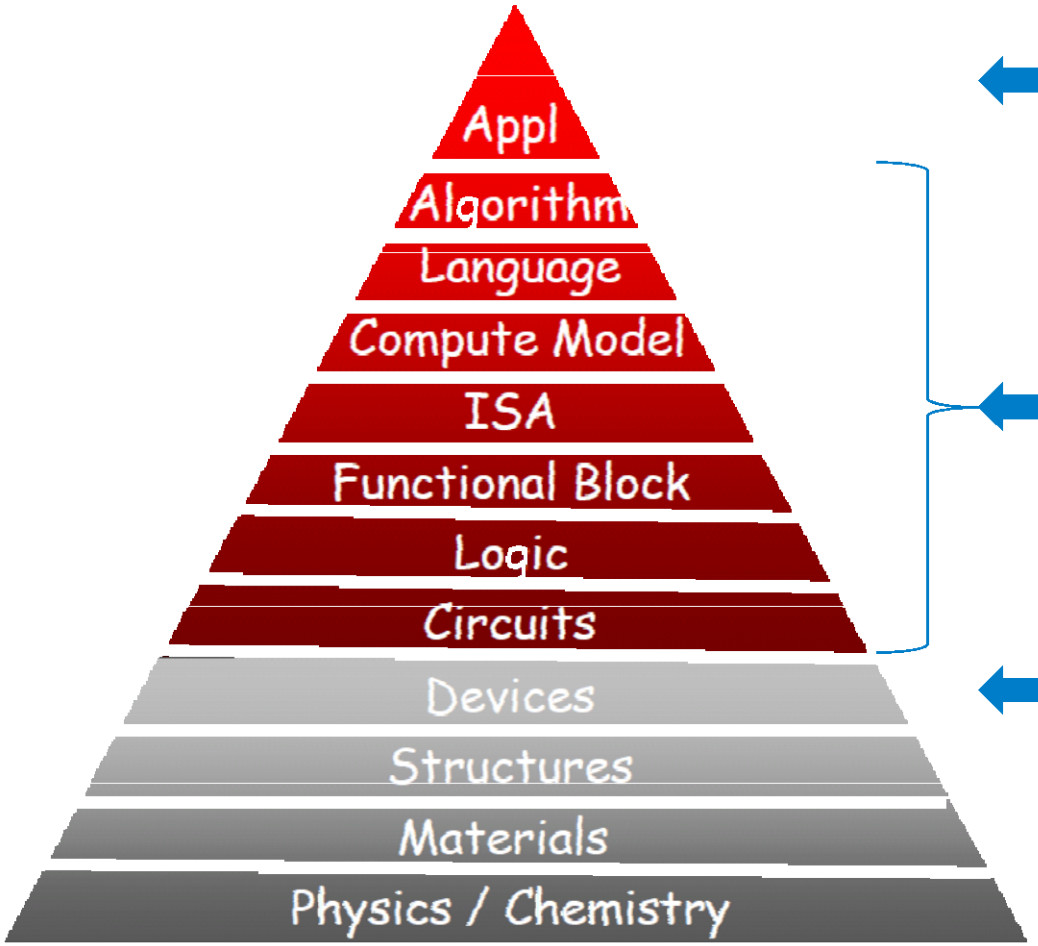
From modelling to design

We can simulate transport in molecular and semiconducting nanostructures quite reliably, accounting for charging effects, dissipation, screening as long as the molecular systems consist of a sufficiently small number of atoms,

but

the simulation of realistic systems, especially in terms of the contacts and in general the coupling with the external environment is still a problem

The Food Pyramid

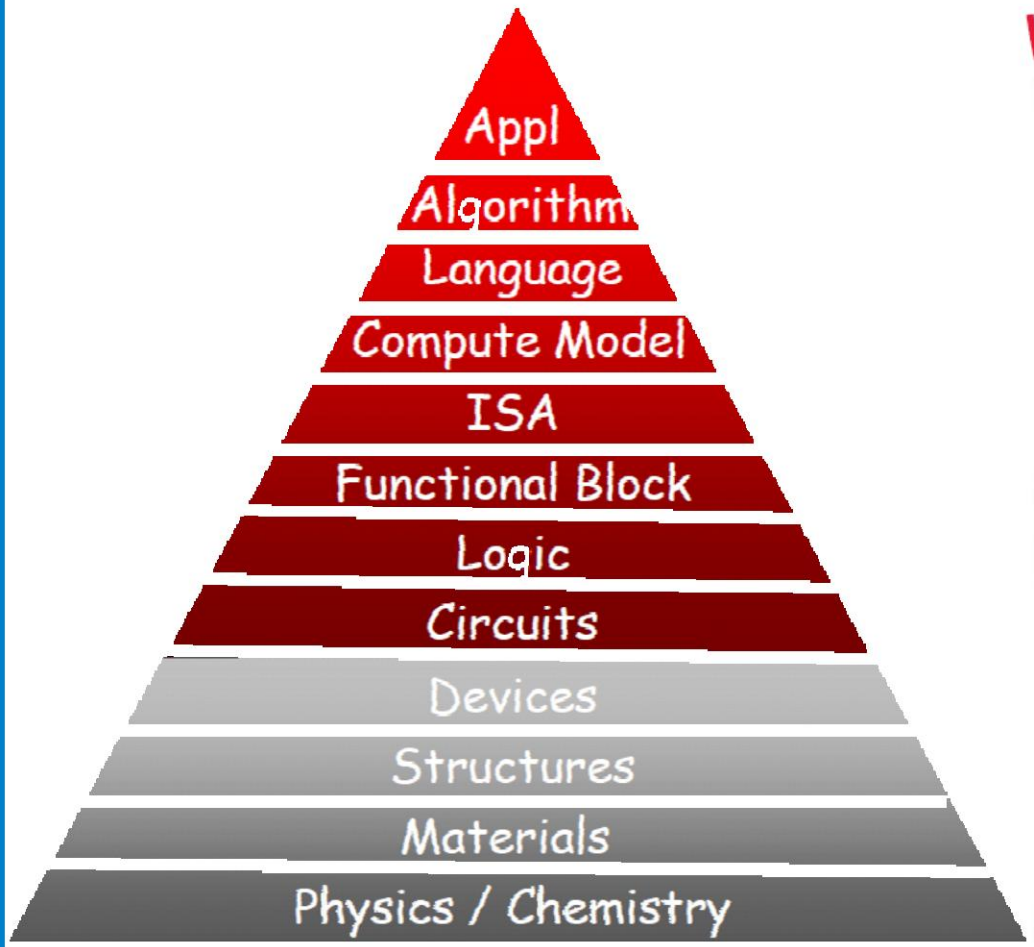


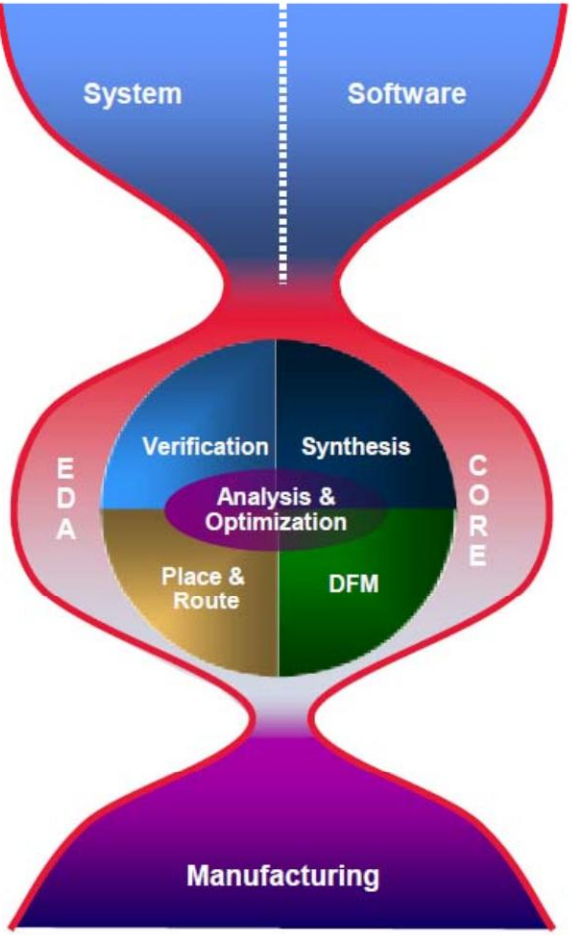
Here needs are born that demand for a solution.

Here Design has to bridge the gap.

Here the Beyond CMOS comes out

A lot of work is done to bridge the gap



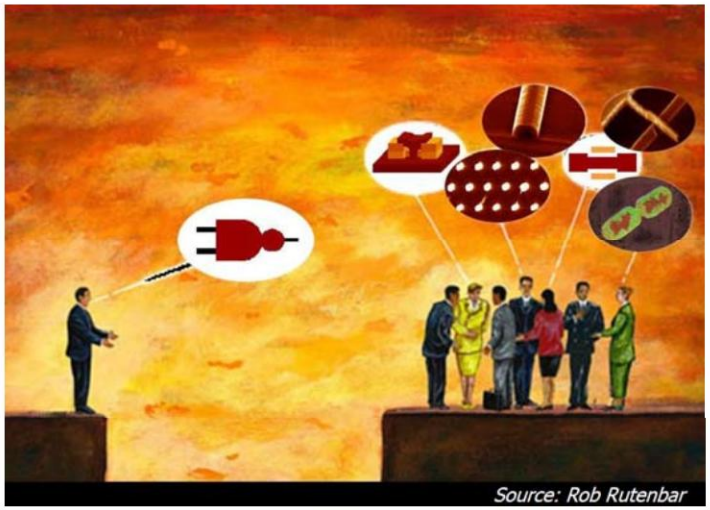


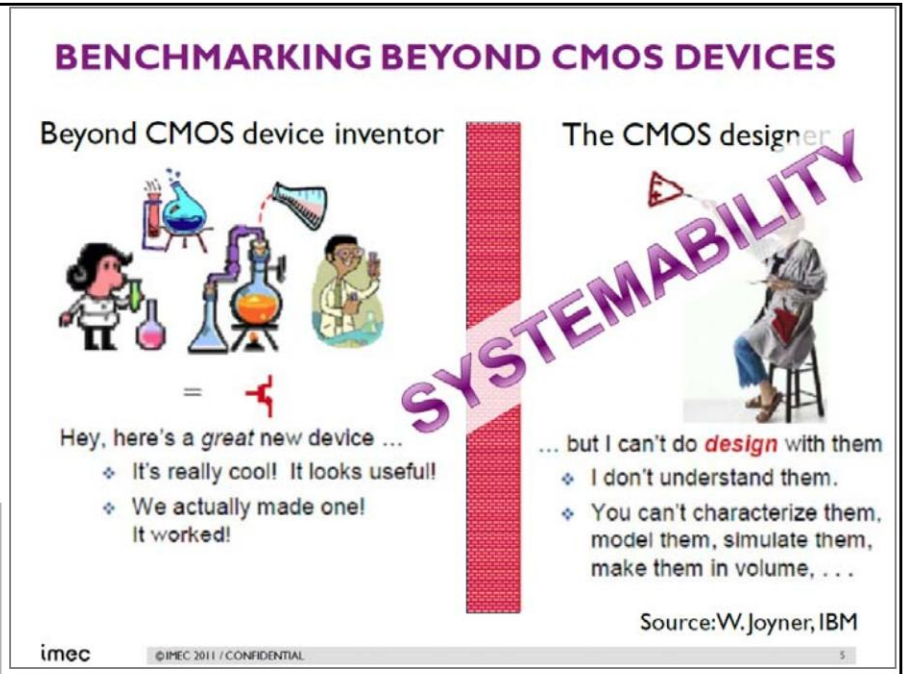
but most of Design today focuses on the "Middle"

The Gap on the bottom is known!

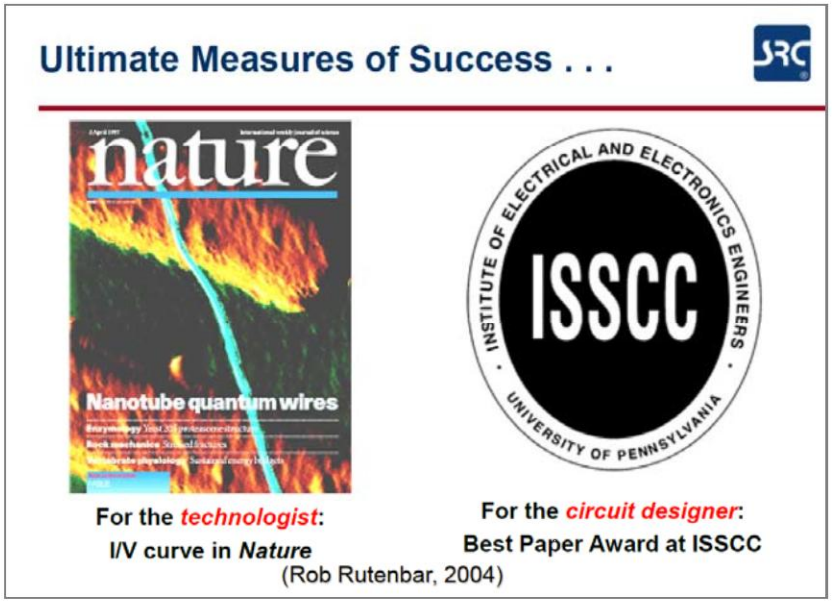
It is between device and system.

SYSTEMABILITY:
The ability to economically design and manufacture reliable systems from the interaction of devices fabricated in a given technology.





Source : D. Verkest, NANO-TEC-WS2, 2011



A Bridge to the system is needed

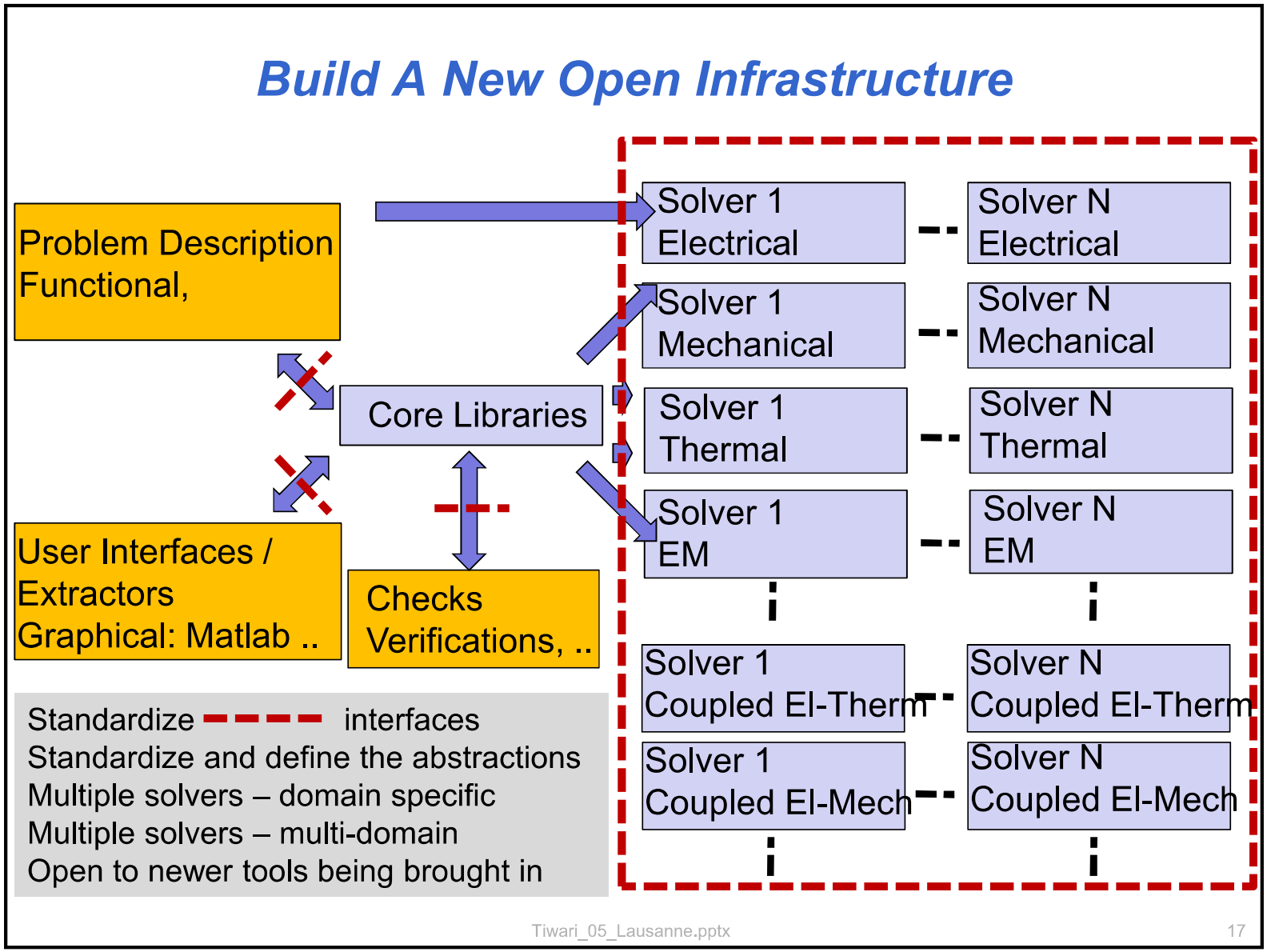
SYSTEM = COMPUTATION, STORAGE, INTERCONNECT, I/O, (ANALOG)

Every contender

- Must add value to one or more of the 4 system functions and be compatible with the others
- All-in throughput/Watt and/or transactions/Joule must beat CMOS at time of manufacturing at equivalent or lower cost
- System level manufacturability, reliability, testability must beat ultimate CMOS solutions
- Room temperature operation is mandatory
- Device variability must be mitigated and modeled and cost efficient error resilient design solutions must be available
- Design methods and tools must be in place supporting design from device to system. Design tool development time is 3x technology development time.

Source :
D. Verkest,
NANO-TEC-WS2, 2011

A POSSIBLE TECHNOLOGY & DESIGN INFRASTRUCTURE



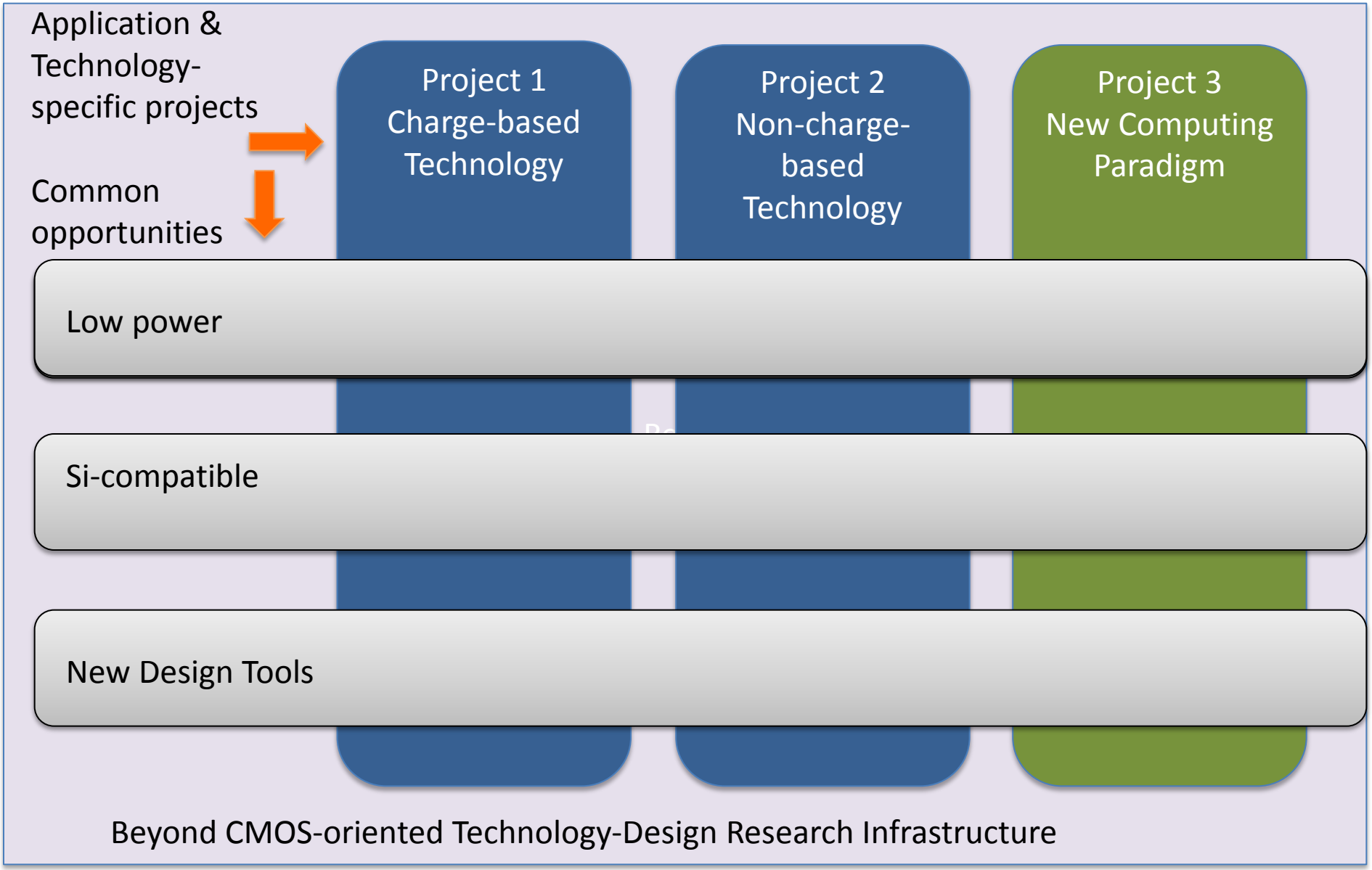
S Tiwari

A BOLD SUGGESTION (1/2)

An “experiment”:

- Develop methods to ensure the technology gap is bridged
- Cluster three pilot project in Beyond CMOS technology-design
- Better still, launch two or three super Integrated Projects
- If clusters then projects each dealing with one of charge-based, non-charge based and a computing paradigm -- at different stages in the TRL.
- If super IPs, then cluster them anyway in joint annual working sessions.
- In either case these should be ideally supported by a pilot distributed technology-design research infrastructure

A BOLD SUGGESTION (2/2)



Beyond CMOS-oriented Technology-Design Research Infrastructure

TODAY's SCOPE

Includes presentations:

- Summary of discussions and recommendations per
  - Charge-based state variable
  - Non-charge-based state variables
  - New computing paradigms
  - Ecosystem technology
  - Design and technology integration
- Working groups to discuss and refine recommendations → final report for the Commission and the community of Beyond CMOS in the combined ecosystem.

AND

- Perspective in Europe and the USA
- Scientific presentations on Neuromorphic computation and Topological Insulators