

# Ecosystems Technology & Design for Nanoelectronics A European Coordination Action

www.fp7-nanotec.eu

#### **Mart Graef**

Delft University of Technology, The Netherlands

ZEROPOWER Glasgow Workshop, 3-4 July 2012





# Outline

- Objectives
- Roadmapping
- Methodology
- Results
- Conclusions





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# **About NANO-TEC**

NANO-TEC is a European Project (Coordination Action) funded by the European Commission ICT theme to run for 30 month until February 2013 with an EU contribution of € 720.000.

Contract Nr FP7/2007-2013

#### Aim

- To identify the next generation of emerging device concepts and technologies for ICT, through a foresight exercise on medium and long-term requirements in nanolectronics research
- To build a joint technology-design community to coordinate research efforts in nanoelectronics by harmonising the efforts of existing and new initiatives and projects





# Project partners

Jouni Ahopelto Noemi Baruch **Alain Cappy Georgios Fagas** Isabelle Ferain Piotr Grabiec Mart Graef Wladek Grabinski Guilhem Larrieu Androula Nassiopoulou Ralf Popp Wolfgang Rosenstiel Clivia M Sotomayor Torres Thomas Swahn Helena Theander Christian Pithan Dag Winkler













de Nanotecnologia

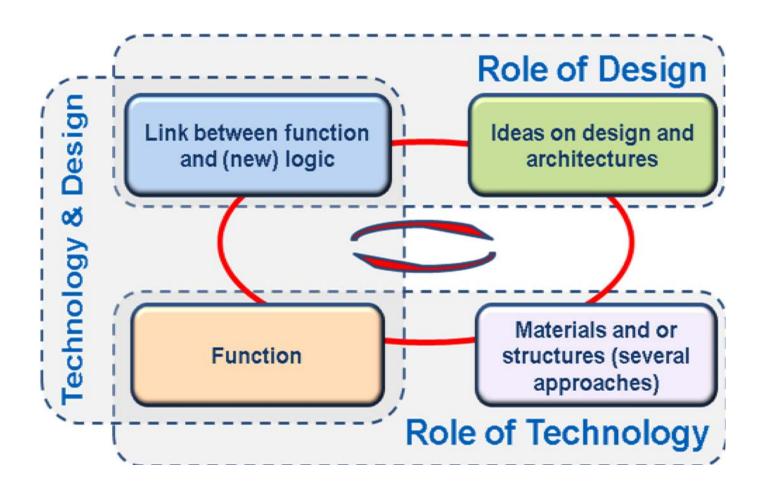








# **NANO-TEC Concept**







# Outline

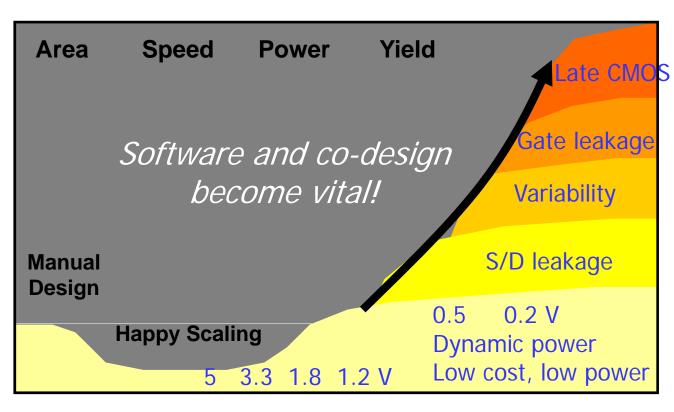
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## More Moore: Increasing complexity





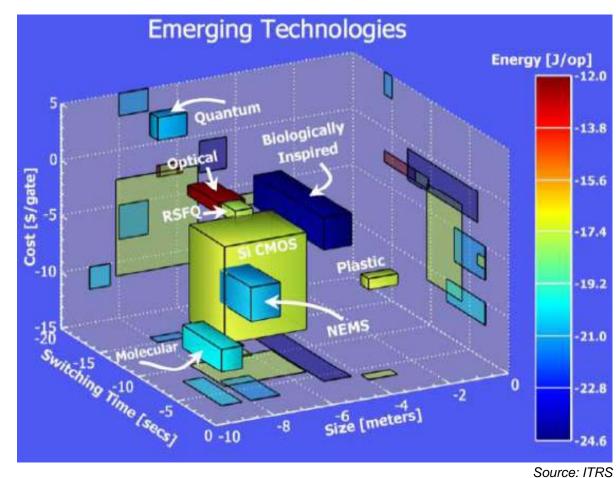
FINFET
FDSOI
Multi-MG
High k
Low k
Strained SiGe

Critical dimension [nm] 500 250 180 130 90 65 45 32 22 Year 1980 1990 2000 2010 2020





# Parameterization of emerging technologies

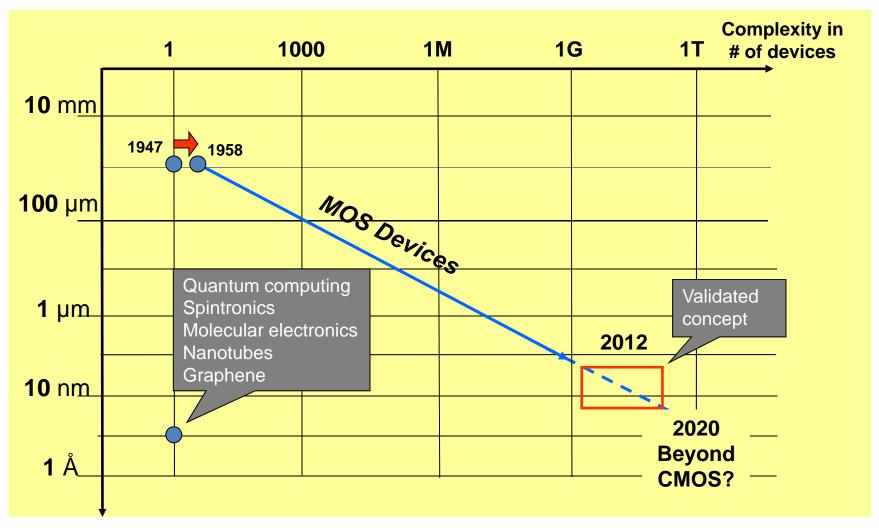








# Reaching dimension/complexity limits

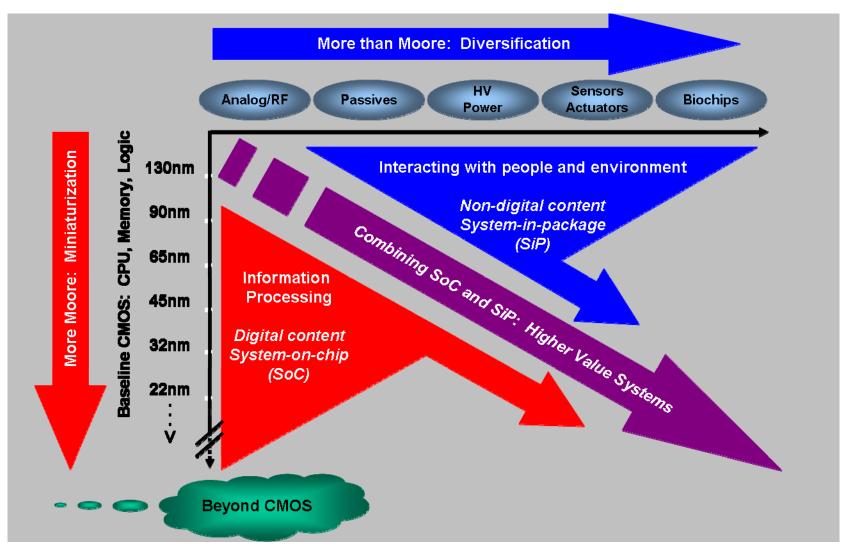


Source: STMicroelectronics





### "More Moore" & "More than Moore"



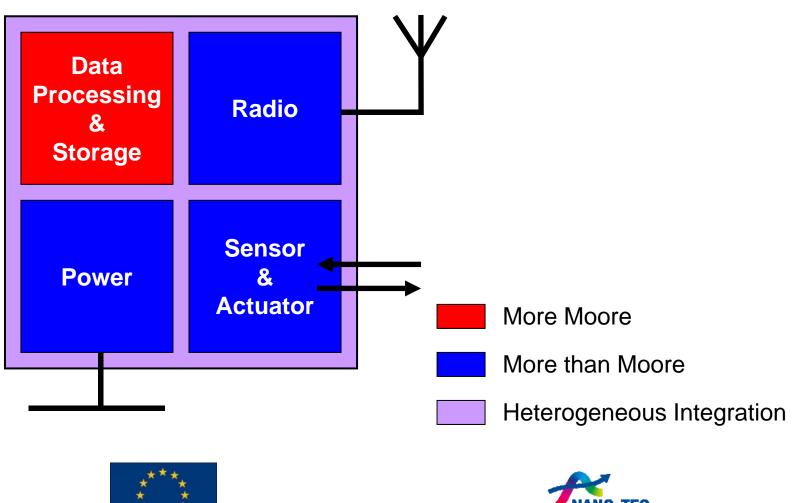






# Smart microsystems:

Beyond CMOS = More Moore + More than Moore







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# NANO-TEC methodology

#### Workshop series with invited experts on 'Beyond CMOS' devices

- Selection of speaker, discussants and rapporteurs from academia, institutes and industry
- Guidelines for all three groups focusing on workshop target
- Report of each Workshop building on previous one towards final recommendations

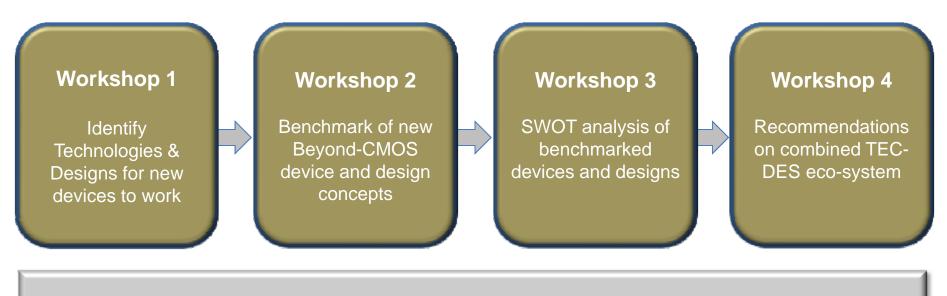
Web platform for working group discussions, communication and access to an information repository

Report on recommendations for Emerging Nanoelectronics, and the desired combined technology-design ecosystem





# NANO-TEC workshops



January 2010 Granada October 2011 Athens May 2012 Lausanne November 2012 Barcelona





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#### 1st NANO-TEC WORKSHOP

#### **Identifying Beyond CMOS devices**

#### 20-21 January 2011, Granada, Spain





# Topics of WS1

- Nanotechnology trends for the next decade
- Carbon-based electronics
- Silicon-based electronics
- Compound semiconductor-based electronics
- Spintronics
- Bridge to Design
- Analogue-Mixed signal design
- Molecular Electronics/quantum computers





# Recommendations of WS1

- Address power consumption, manufacturability and performance as priorities
- Strengthen research in device functionality at the nanoscale, addressing new architectures and alternative concepts to do computation
- On Beyond CMOS design issues, research needs include:
  - Circuits and architectures for a full exploitation of nanocomponents
  - Mode of operation of such devices
  - Multi-scale approach, in order to describe realistic systems





# 2<sup>nd</sup> NANO-TEC Workshop Benchmarking of new Beyond CMOS device/design concepts

#### 12-14 October 2011, Athens, Greece







# **Motivation for Benchmarking**

- Large number of emerging 'Beyond CMOS' device concepts
- Various types of functions (data processing, computation, memory,interconnect...)
- Device fabrication/production?
- Architectures, design tools, libraries?
- Application prospects?
- Unique exercise in advancing the research of future emerging devices in Europe.







# **Benchmarking Beyond CMOS Devices**

| Technology   | [Wires, graphene, MEMS etc please insert name] |
|--|--|
| Gain   |  |
| Signal/Noise ratio                                       |  |
| Non-linearity  |  |
| Speed  |  |
| Power consumption  |  |
| Architecture/Integrability                               |  |
| (Inputs/outputs, digital, multilevel, analog, size etc.) |  |
| Other specific properties                                |  |
| Manufacturability  |  |
| (Fabrication processes needed, tolerances etc.)          |  |
| Timeline   |  |
| (When exploitable or when foreseen in production)        |  |

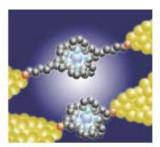




# Example: Molecular electronics

D. Vuillaume (CNRS, Lille), 2nd NANO-TEC Workshop

# Single molecule electronics

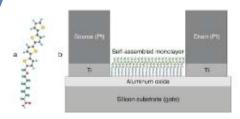


L < a few nm t < a few nm

basic science knowledge development

no foreseen applications in a reasonable time-scale

Self-assembled molecular electronics



 $L \sim tens nm - \mu m$ t < a few nm

basic science knowledge development

possible applications foreseen

Thin film molecular electronics



L > µm t > few 10 nm

plastic electronics (OLED, OFET, OPV)

some products already commercialized





# Example: Molecular electronics

# Benchmarking Beyond CMOS Devices NANO-TEC

| Technology  | Molecular Electronics  D. Vuillaume, CNRS & University of Lille   |
|---|---|
| Gain<br>Signal/Noise ratio<br>Non-linearity   | Ok with SAMFET (to be optimized), 2-terminal junction: low current Noise not yet studied (a few publications)  Molecular junctions are mainly non-linear  |
| Speed<br>Power consumption  | Low (50 zJ/m ol switching energy)   |
| Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.) | Molecule-nanoparticle 2D and 3D arrays could implement some functions (e.g. reconfigurable logic, neuro-inspired functions)                               |
| Other specific properties   | Almost infinite combination of molecules, adjustable by chemistry, specific design (1 molecule = 1 function)  |
| Manufacturability (Fabrication processes needed, tolerances etc.)                   | Solution processing, compatible with flexible substrate.  Defect control? Large variability (but not a problem if we envision artificial neural networks) |
| Timeline<br>(When exploitable or when<br>foreseen in production)                    | > 5 - 10 years (if ever?)   |





# Conclusions of WS 2

- Technology/Emerging devices ← Architecture/Design
  - Quite apart
- Emerging device concepts:
   Not enough data for current design tools
  - Transfer functions, memory, interconnects, tolerances, noise...
- Design tools have to develop towards multi-scale approaches
  - Physics, non-Boolean, multilevel...





# 3rd NANO-TEC WORKSHOP SWOT Analysis of the Technology-Design Ecosystem

#### 30-31 May 2012, Lausanne, Switzerland







# **SWOT Analysis of Beyond CMOS Devices**

#### **Strengths**

- Application perspective
- Building blocks for innovation in nanoelectronics
- European industrial/academic ecosystem

#### Weaknesses

- Physical constraints
- Compatibility issues with conventional technology
- Reliability, variability

#### **Opportunities**

- Design of circuits and systems
- 3D integration of multifunctional systems
- Industrial/academic cooperation

#### **Threats**

- Gap to industrial needs?
- 'CMOS competition'
- Manufacturability





#### 4<sup>th</sup> NANO-TEC WORKSHOP Recommendations for the Technology-Design Ecosystem in Nanoeletronics

#### 6-7 November 2012, Barcelona, Spain



Register at: <a href="https://www.fp7-nanotec.eu/registration">https://www.fp7-nanotec.eu/registration</a>





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### **Conclusions**

- The identification, benchmarking and SWOT analysis of Beyond CMOS devices and technologies is well underway. This will lead to a shared vision on needs, capabilities and methodologies.
- NANO-TEC has initiated a dialogue between the technology and design communities in Europe on Beyond CMOS.
- As a result, new opportunities for collaboration on nanoelectronics between industry, institutes and academia are emerging.





# Acknowledgments

#### The NANO-TEC consortium, in particular:

- Clivia Sotomayor Torres
- Jouni Ahopelto
- Ralf Popp



