

ECOSYSTEMS TECHNOLOGY & DESIGN for NANO-ELECTRONICS: a European Coordination Action

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www.fp7-nanotec.eu

INC8 TSUKUBA, JAPAN, 8-11 MAY 2012



OUTLINE

- Objectives of NANO-TEC
- NANO-TEC in the European Nanoelectronics landscape
- Methodology
- Main workshops results
- Bridging the gap Technology Design
- Conclusions



ABOUT NANO-TEC

NANO-TEC is a European Project (Coordination Action) funded by the European Commission ICT theme to run for 30 month until February 2013 with an EU contribution of € 720.000.

Contract Nr FP7/2007-2013

AIMS

- To identify the next generation (emerging) of device concepts and technologies for ICT through a foresight exercise on medium and long-term requirements in nanoelectronics research
- To build a joint technology-design community to coordinate research efforts in nanoelectronics by harmonising the efforts of existing and new initiatives and projects

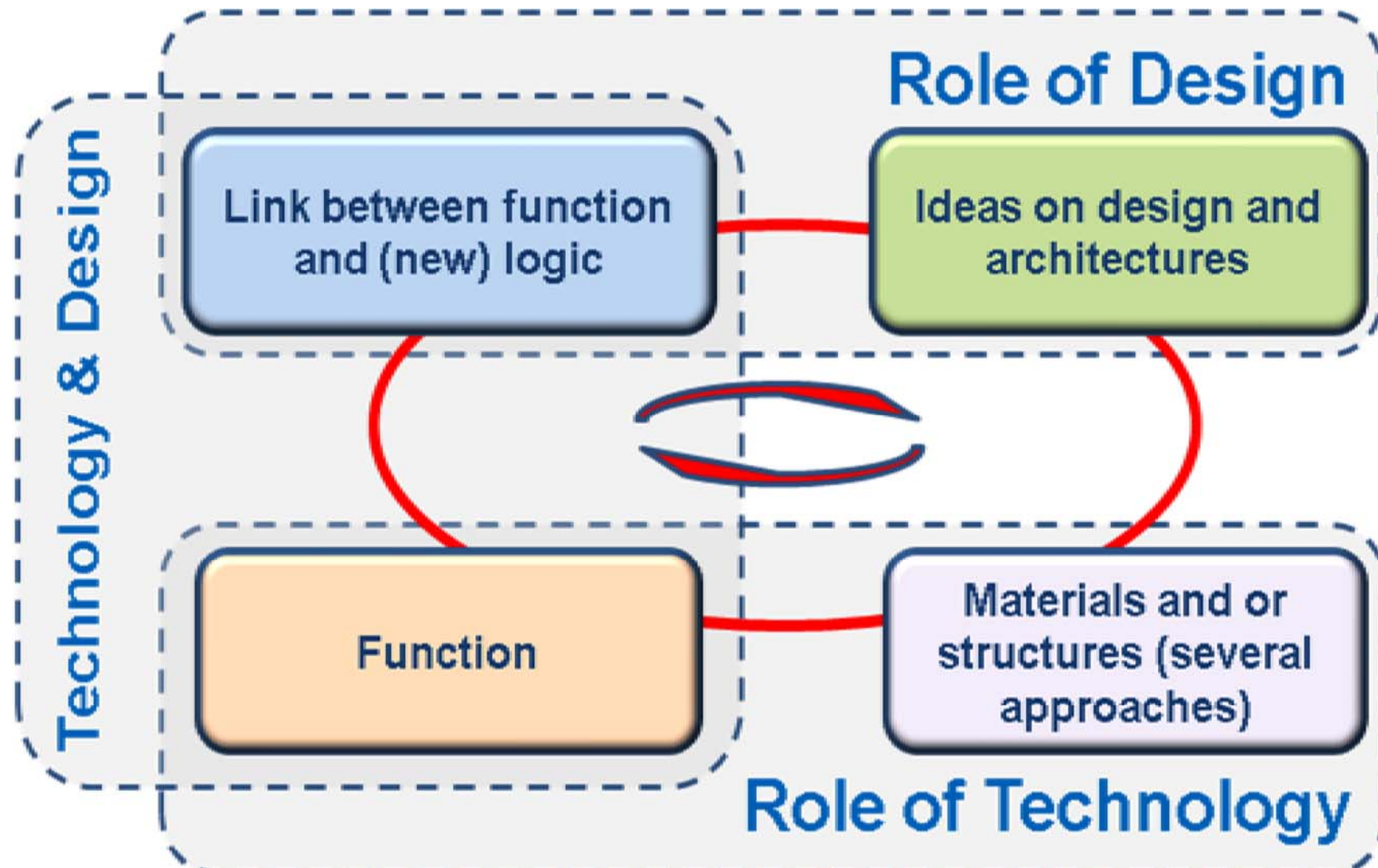


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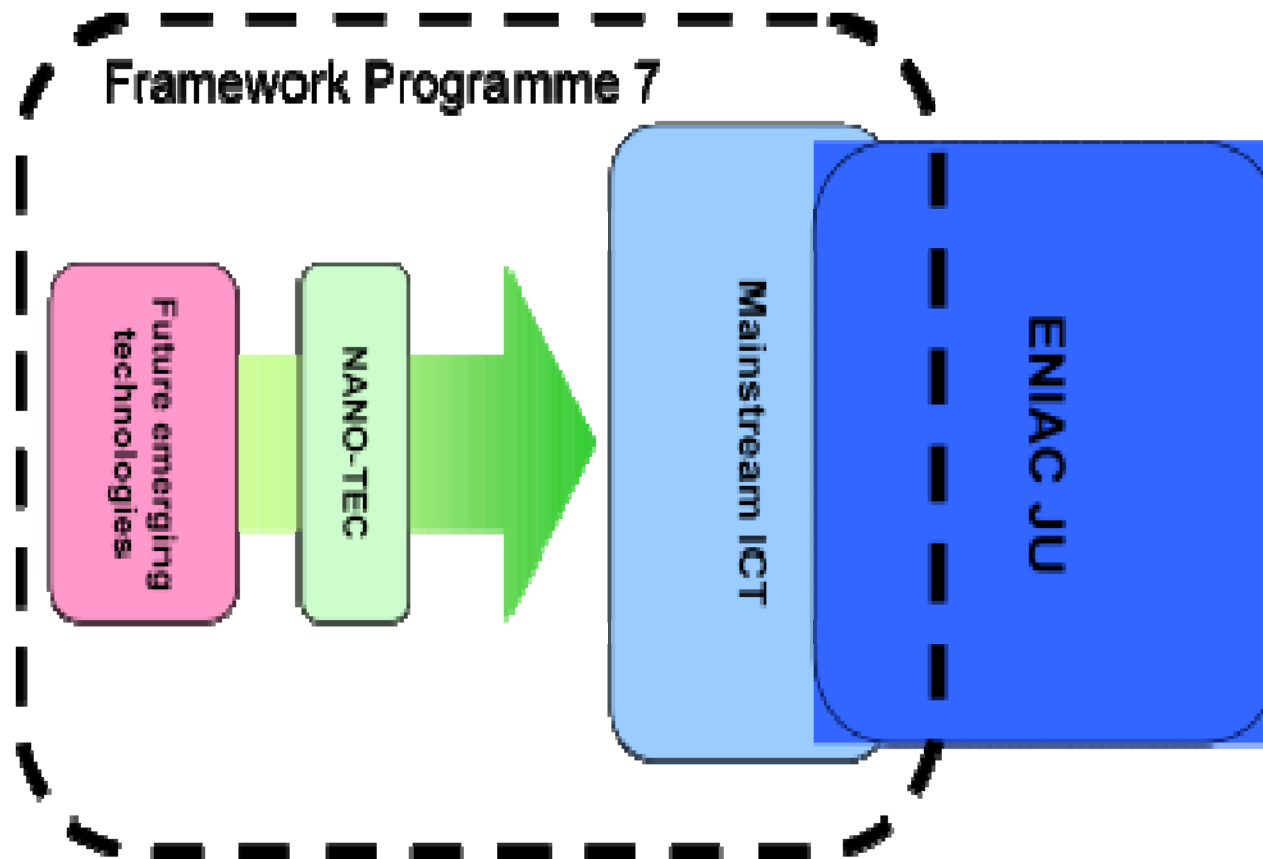


NANO-TEC CONCEPT



EXPECTED IMPACT – 1

Benchmarking and selection of promising device concepts through sieve filtering results from emerging technology projects for mainstream activities



Transfer of Beyond CMOS era concepts and devices to mainstream activities in nanoelectronics

NANO-TEC Advisory Board

Livio Baldi

Michel Brillouet

Danilo Demarchi

Roger de Keersmaecker

Micron

CEA-LETI

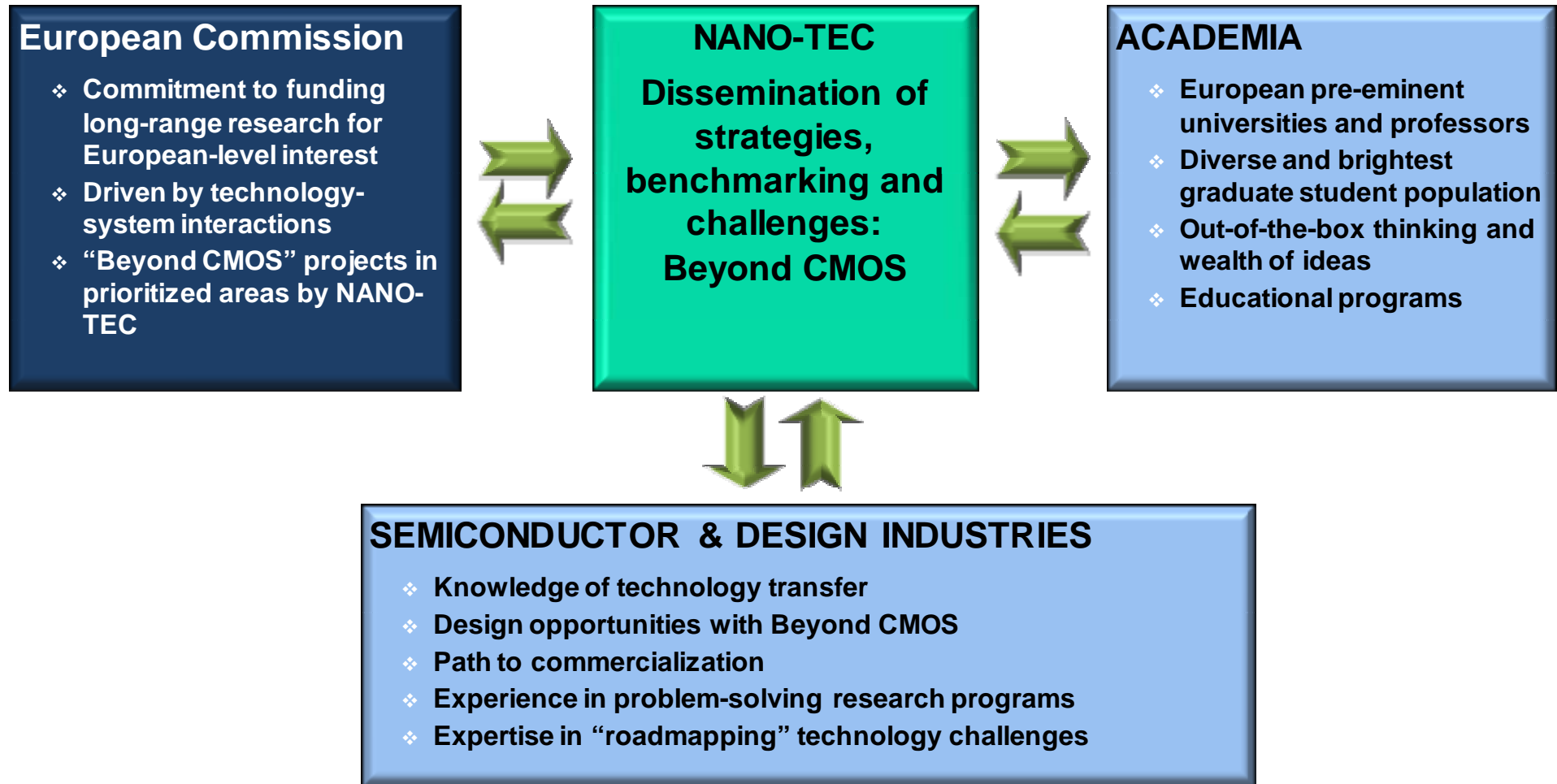
Polytechnic University
of Torino

IMEC



EXPECTED IMPACT - 2

Knowledge transfer and community building through dissemination, training and education activities



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NANO-TEC remit

Thematically:

Emphasis on Beyond CMOS Devices and Design

As Instrument:

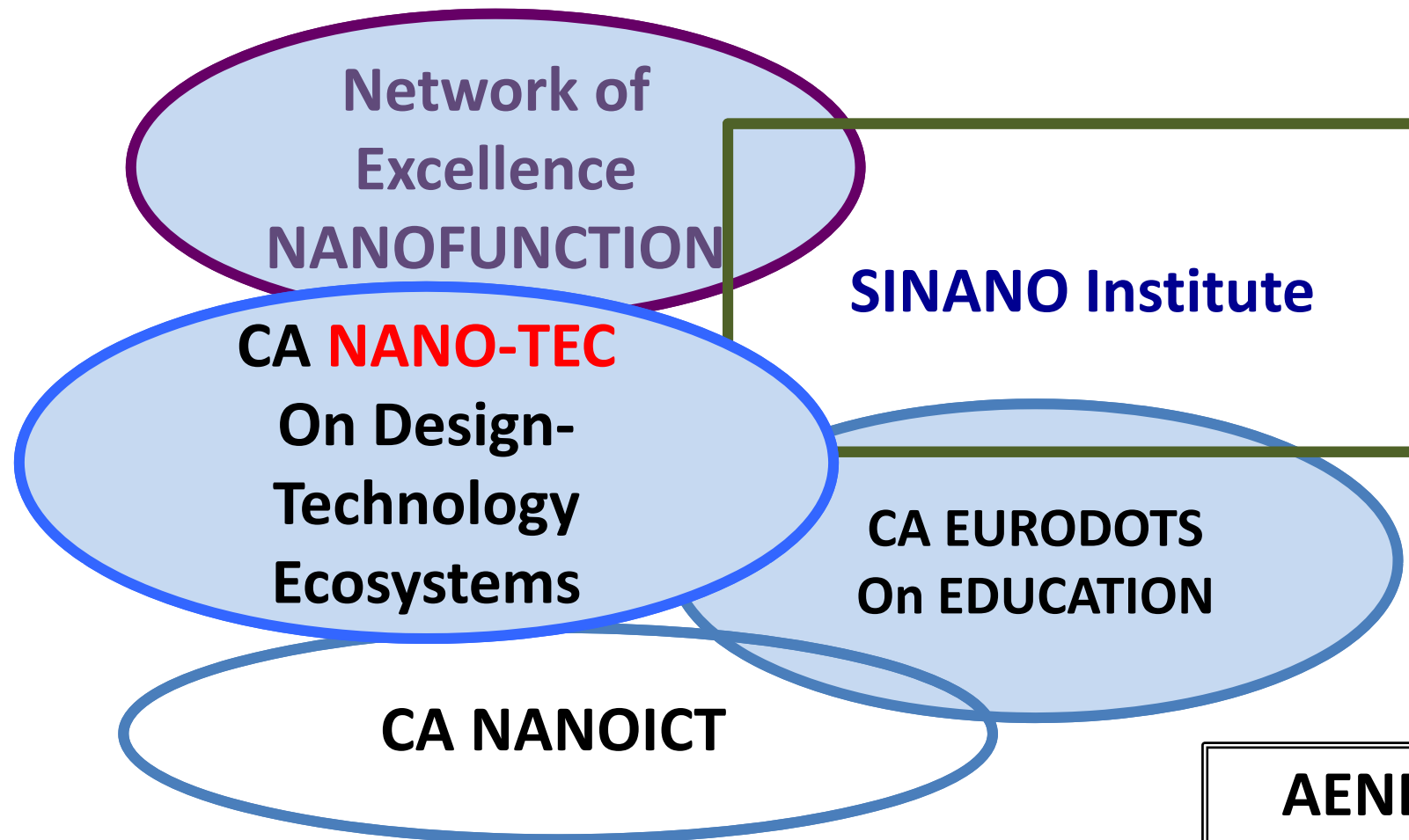
Organises and coordinates discussions and makes recommendations

Actors:

Mainly from academia and research organisation.



NANO-TEC in the EU landscape



Coordination, discussions, policy recommendations
on Nanoelectronics in Europe



AENEAS
CATRENE
FP7/H2020

Examples of information inputs to NANO-TEC

NANOLITO and NANOSPAIN Networks

RENATECH. Long-term fundamental research nanosciences, nanoscience & nanotechnology and engineering

CNANO. Network for Scientific coordination in French nanosciences

CNFM. French network for national coordination for training in Micro and nanoelectronics

Micronova. Centre for Micro and Nanoelectronics

FinNano. National nanoelectronics programme

Swedish Foundation for Strategic Research

Gigabit Wave project. Millimetre wave communication links for ultra-high bit rates

Myfab, Swedish network for micro- and nanofabrication

Linnaeus, Linnaeus Centre on Engineered Quantum Systems

ITRS group on Emerging Research Devices

NANOTEC-related project: NaPANIL, NANOPACK, SOLID, TAILPHOX, SUBTLE, BIODIAGNOSTIC, EuroSQIP, SUPERADC, ACCESS etc...



Position papers on
parts Beyond
CMOS by



2008 CNTs



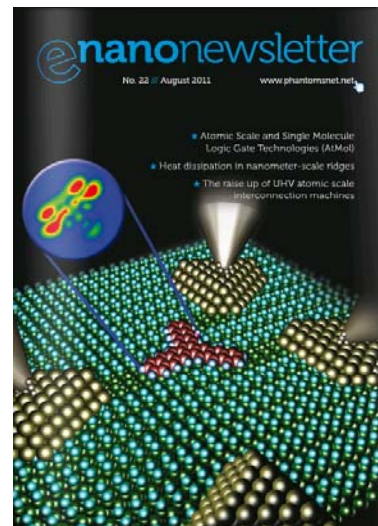
2008 NEMs



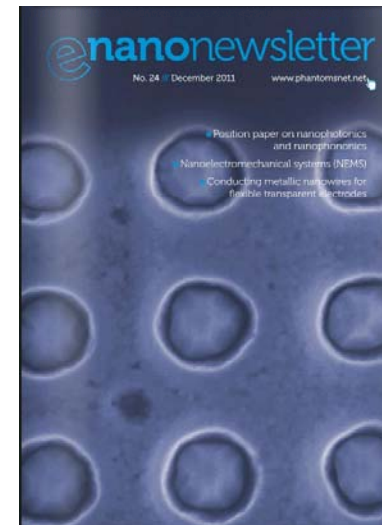
Nov. 2009 Modelling



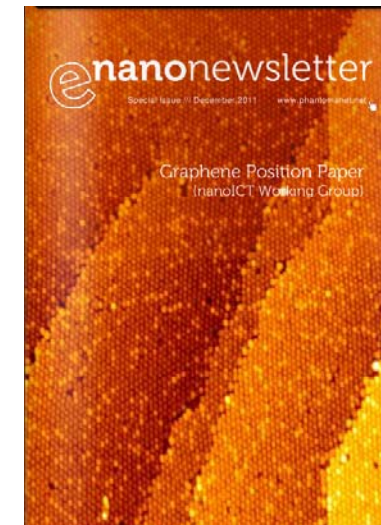
2010 Nanowires
Vol. 17/18



Aug. 2011 Single
Molecule technology



Dec. 2011 nanophotonics-
nanophononics



Dec. 2011
graphene

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NANO-TEC METHODOLOGY

A workshop series with invited experts on beyond CMOS devices and design from Europe, Asia and the Americas.

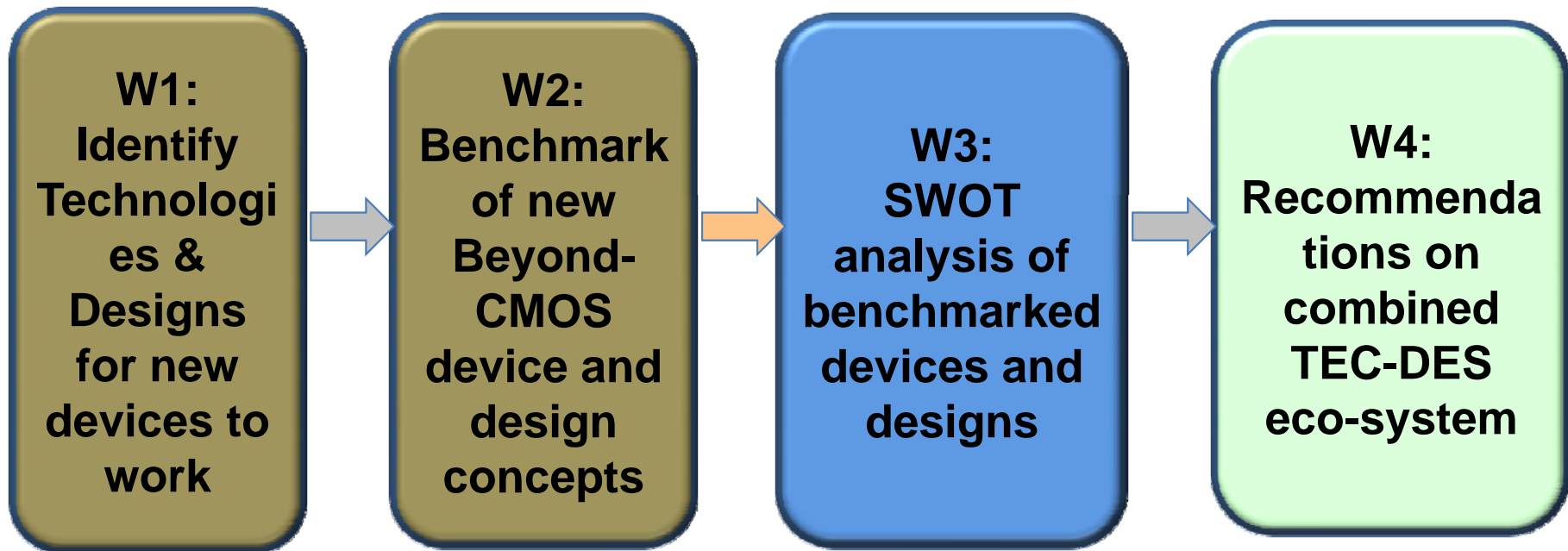
- Selection of speaker, discussants and rapporteurs from academia, ROs and industry
- Guidelines for all three groups focusing on workshop target
- Report of each Workshop building on previous one towards final recommendations

A state-of-the-art web platform for (working groups) discussions, communications and access to an information repository.

A report on recommendations for Emerging Nanoelectronics, and the desired combined ecosystem technology-design.



NANO-TEC workshops



January 2010
Granada

October 2011
Athens

30-31 May 2012
Lausanne

Autumn 2012



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1st NANO-TEC WORKSHOP

Identifying Beyond CMOS devices

20-21 January 2011, Parque de las Ciencias, Granada, Spain



About 75 participants

Topics of WS1

Nanotechnology trends for the next decade (J Welser, SRC)

Carbon-based electronics (Jeong-Sun Moon, HP)

Silicon-based electronics (M Brillouet, CEA LETI)

Compound semiconductor-based electronics (W Stanchina, Pittsburgh)

Spintronics (S Valenzuela, ICN)

Bridge to Design (P Lugli, TU München)

Analogue-Mixed signal design (H Graeb, TU Munich)

Molecular Electronics/quantum Computers (G Wendin, Chalmers)



Recommendations of WS1

- Address *power consumption, manufacturability* and *performance* as priorities.
- Strengthen research in device functionality at the nanoscale addressing new architectures and alternative concepts to do computation.
- On *Beyond CMOS design issues*, research needs include:
 - i) Circuits and architectures will be needed for a full exploitation of nano components.
 - ii) Mode of operation of such devices
 - iii) Multi-scale approach needed in order to describe realistic systems.

And specific recommendations for groups of emerging technologies



2nd NANO-TEC Workshop
Benchmarking of new Beyond CMOS device/design concepts

12-14 October 2011, Divani Caravel Hotel, Athens, Greece



About 70 participants

Topics of WS2

Molecular Electronics (D Vuillaume, CNRS, Lille, France)

MEMS (Lina Sarro, TU Delft, The Netherlands)

Solid State Quantum Computing (Jaw-Shen Tsai - NEC & The Riken Institute)

Spintronics (J Åkerman, Gothenburg U & NanoSC)

Nanowires (Heike Riel, IBM Zurich)

Memristors (J Grollier, CNRS-Thales, Palaiseau, France)

Graphene (J Kinnaret, Chalmers University of Technology, Gothenburg)

Panel Discussion on Design (D Herr, SRC; D Verkest, IMEC; P Lugli, TUM; S Tiwari, Cornell U; L Hedrich, JW Goethe U Frankfurt)



Motivation for Benchmarking

- Large number of emerging "Beyond CMOS" device concepts
- Various types of functions
- Can those be used for data processing
(computation/memory/interconnects...)?
- Device fabrication/production?
- Architectures, design tools, libraries?
- Prospects?
- Unique exercise in advancing the research of future emerging devices in Europe.



Benchmarking procedure

Previous exercise: SRC (USA): “The quest for a better Switch” considered several candidate devices from 15 nm LV CMOS to emerging graphene thermal logic and few spin

Bernstein et al., Device and Architecture Outlook for Beyond CMOS Switches, Proc. IEEE 98 (2010) 2169.

Here aim to a broader scope:

- **No direct comparison with CMOS**
- **Allow for other concepts in addition to digital switches**
- **Challenge the design community**



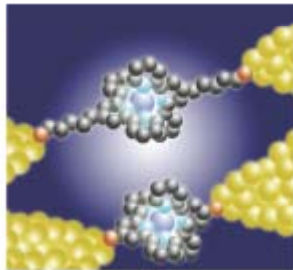
Benchmarking Beyond CMOS Devices

Technology	[Wires, graphene, MEMS etc... please insert name]
Gain Signal/Noise ratio Non-linearity	
Speed Power consumption	
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	
Other specific properties	
Manufacturability (Fabrication processes needed, tolerances etc.)	
Timeline (When exploitable or when foreseen in production)	

Example: Molecular electronics

D. Vuillaume (CNRS, Lille), 2nd NANO-TEC Workshop

Single molecule electronics

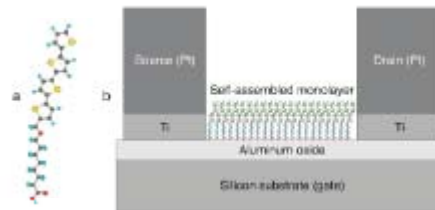


$L < \text{a few nm}$
 $t < \text{a few nm}$

basic science
knowledge development

no foreseen applications
in a reasonable time-scale

Self-assembled molecular electronics



$L \sim \text{tens nm} - \mu\text{m}$
 $t < \text{a few nm}$

basic science
knowledge development

possible applications
foreseen

Thin film molecular electronics



$L > \mu\text{m}$
 $t > \text{few } 10 \text{ nm}$

plastic electronics
(OLED, OFET, OPV)

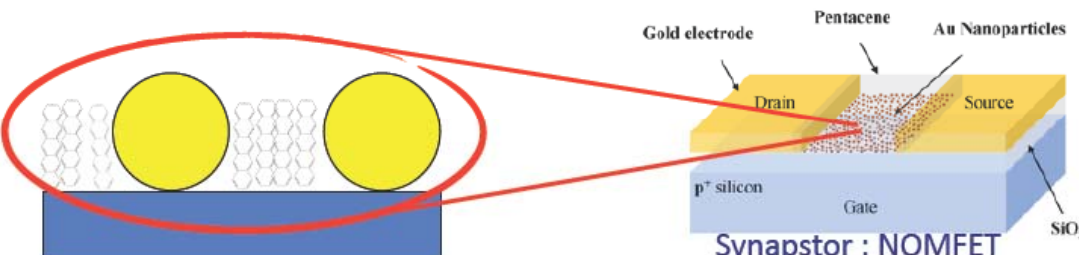
some products already
commercialized



Example: Molecular electronics



Benchmarking Beyond CMOS Devices

Technology	Molecular Electronics D. Vuillaume, CNRS & University of Lille
Gain	Ok with SAMFET (to be optimized), 2-terminal junction: low current
Signal/Noise ratio	Noise not yet studied (a few publications)
Non-linearity	M
Speed	Lc
Power consumption	Lc
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	M fu 
Other specific properties	Almost infinite combination of molecules, adjustable by chemistry, specific design (1 molecule = 1 function)
Manufacturability (Fabrication processes needed, tolerances etc.)	Solution processing, compatible with flexible substrate. Defect control? Large variability (but not a problem if we envision artificial neural networks)
Timeline (When exploitable or when foreseen in production)	> 5 – 10 years (if ever?)



Conclusions of WS 2

Technology/Emerging devices -> <- Architecture/Design
Quite apart

Emerging device concepts: Not enough data for current design tools

Transfer functions, memory, interconnects, tolerances, noise...

Design tools have to develop towards multi-scale approaches

Physics, non-Boolean, multilevel...

Suitable benchmarking method for Beyond CMOS devices and architectures?

To be refined...



Recommendations of WS2

General:

Develop methodology for benchmarking Beyond CMOS devices vis-à-vis design and architectures.

Recommendations per device and categories.

Example of Molecular Electronics

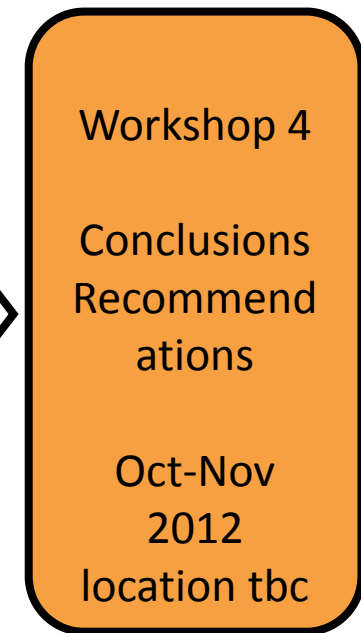
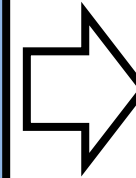
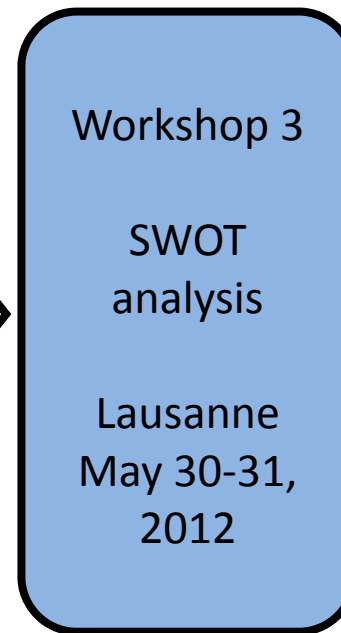
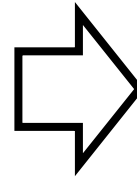
Continue research in *molecular electronics* to gain insights in the behaviour and potential of molecules as building blocks for information processing devices accompanied by efforts in design. In this way, advances will be made in architectures for molecular devices, switches and memories, as well as in neuron inspired devices.



The next step



- Molecular Electronics
- MEMS
- Solid-State Quantum Computing
- Spintronics
- Nanowires
- Memristors
- Graphene



3rd NANO-TEC WORKSHOP
SWOT Analysis of the Technology-Design Ecosystem

30-31 May 2012, Hotel Beau Rivage Palace, Lausanne, Switzerland



Register at: <https://www.fp7-nanotec.eu/registration>



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NANO-TEC and the DESIGN Community



Embedded tutorial **BEYOND CMOS - BENCHMARKING FOR FUTURE TECHNOLOGIES** at the DESIGN, AUTOMATION and TEST in Europe, Dresden 12th March 2012. About 70 participants.

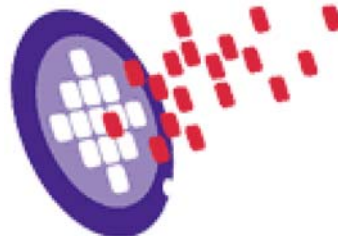
- Emerging Technologies: More Moore and More than Moore
 - Dr Mart Graef, Delft University of Technology, The Netherlands
- Technology and Design challenges in future low power memory devices and circuits
 - Dr Paolo Fantini, Micron Semiconductors, Italy
- Bridging Technology and Design for Beyond CMOS
 - Prof Paolo Lugli, Technical University of Munich, Germany
- Bridging Technology and design in More than Moore
 - Dr Wladek Grabinski, EPFL, Switzerland
- Benchmarking for Beyond CMOS technologies
 - Prof Jouni Ahopelto VTT, Finland



NANO-TEC and the DESIGN Community

The logo for edaWorkshop12, featuring the text "edaWorkshop12" in white on a dark blue rectangular background.

Dr Isabelle Ferain (Tyndall National institute) will give a seminar at the EDA Workshop in May 2012, Hannover, Germany on **NANO-TEC: Building Bridges Between Beyond CMOS Technologies and Design**



17-21 September 2012 - Bordeaux- France

Tutorial on **ECOSYSTEMS TECHNOLOGY & DESIGN for NANO-ELECTRONICS** has been accepted for ESSCIRC/ESSDERC 2012
Prof Dr Androula Nassiopoulou and Dr Wladek Grabinski



Conclusions

NANO-TEC has made a significant start in the dialogue between Technology and Design in Beyond CMOS in Europe.

The identification of Beyond CMOS devices and technologies has come up from a bottom-up open and frank discussion and has triggered a search for suitable benchmarking procedures.

The SWOT analysis is expected to strengthen the joint communities and result in a common vision of needs, potentials and modus operandi.

New facets of collaborations in nanoelectronics among Industry, Research Organisations and Academia, in the context of societal challenges now and in the future, will emerge and be developed.

Expect findings will have impact in policy decisions in Europe in the field of Nanoelectronics.

