edaWorkshop12

"NANO-TEC: Building Bridges Between Beyond CMOS Technologies and Design"

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University College Cork

NANO-TEC has received funding from the European Community's Seventh Framework Programme (FP7/2007-2013) under grant agreement n° 257964

Agenda

- **About NANO-TEC**
  - Objectives
  - Activities
  - Timeline
- **'Beyond CMOS' devices**
  - Taxonomy
  - Motivation
  - Benchmarking Methodology
- **Building Bridges**
  - Molecular Electronics
  - Nanowire Transistors
  - Switching Memristors
  - Graphene Transistors
- **Conclusion**

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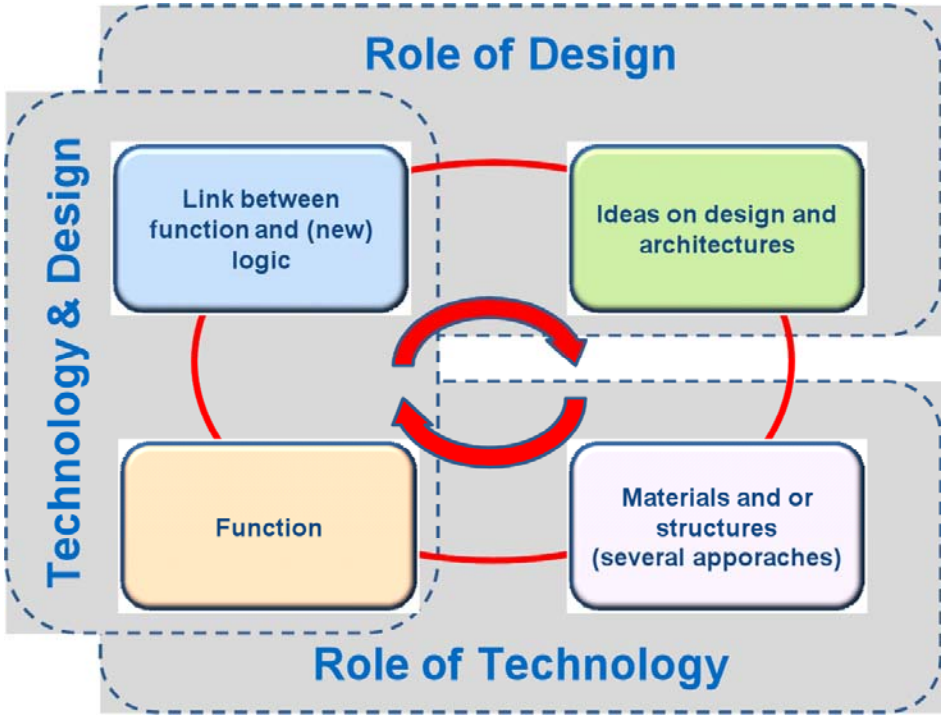
About NANO-TEC: Objectives

- To identify the next generation of (emerging) device concepts and technologies for ICT.
- To build a joint technology-design community to coordinate research efforts in nano-electronics.

About NANO-TEC: Activities



- 4 workshops with invited experts on Beyond CMOS devices, benchmarking and a SWOT analysis of new devices.
- A state-of-the-art web platform for working groups, enabling discussions fora, meetings, communications and access to an information repository.
- A report on Emerging Nanoelectronics.

About NANO-TEC: Timeline

Workshop 1

Identify Technologies & Designs for New Devices to Work

Workshop 2

Benchmark of New Beyond-CMOS Device and Design Concepts

Workshop 3

SWOT Analysis of Benchmarked Devices and Designs

Workshop 4

Recommendations on Combined TEC-DES Eco-System

January 2010 Granada

October 2011 Athens

30-31 May 2012 Lausanne

Autumn 2012

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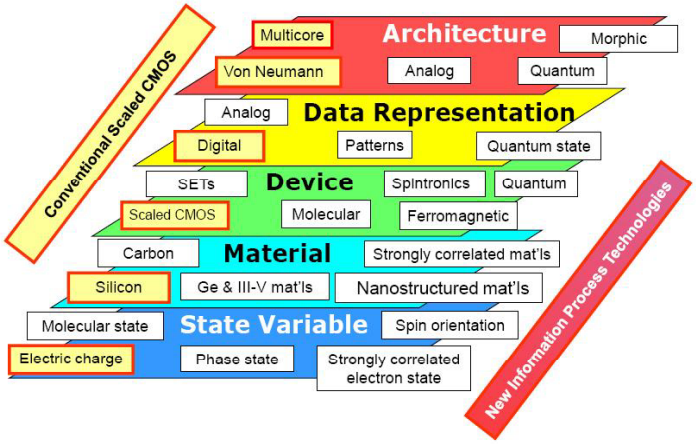
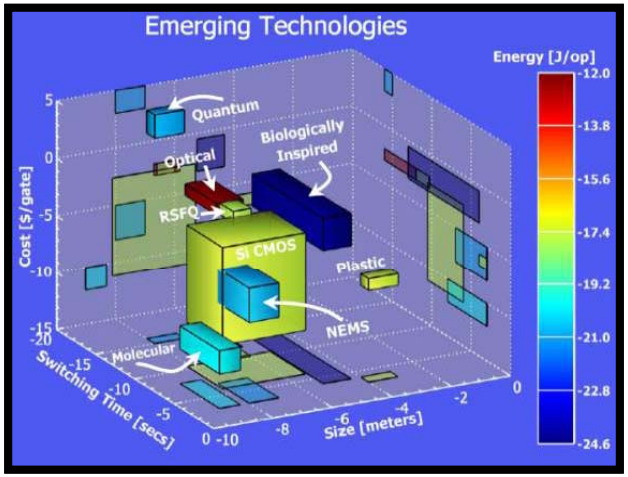
"Beyond CMOS" technologies: Taxonomy

- **New information processing devices and architectures**



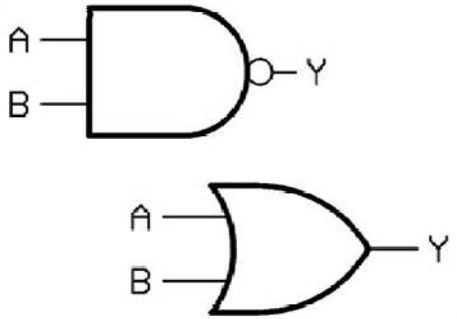


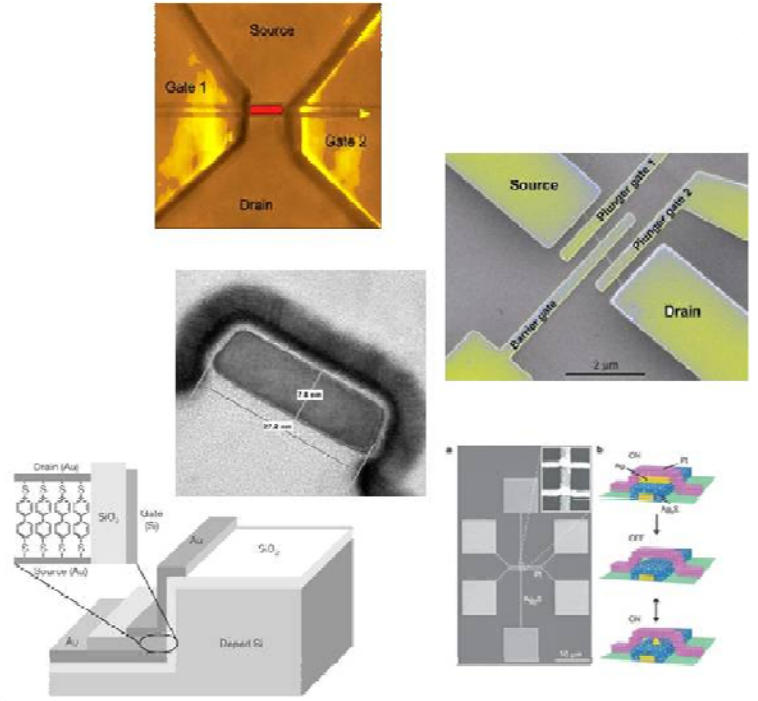
(Reproduced after ERD ITRS)

- Nano-Electro Mechanical Switches
- Collective Spin Devices
- Spin Torque Transfer Devices
- Atomic Switch / Electrochemical Metallization
- Carbon-based Nanoelectronics
- Single Electron Transistors
- CMOL / Field Programmable Nanowire Interconnect (FPNI)

"Beyond CMOS" technologies: Motivation

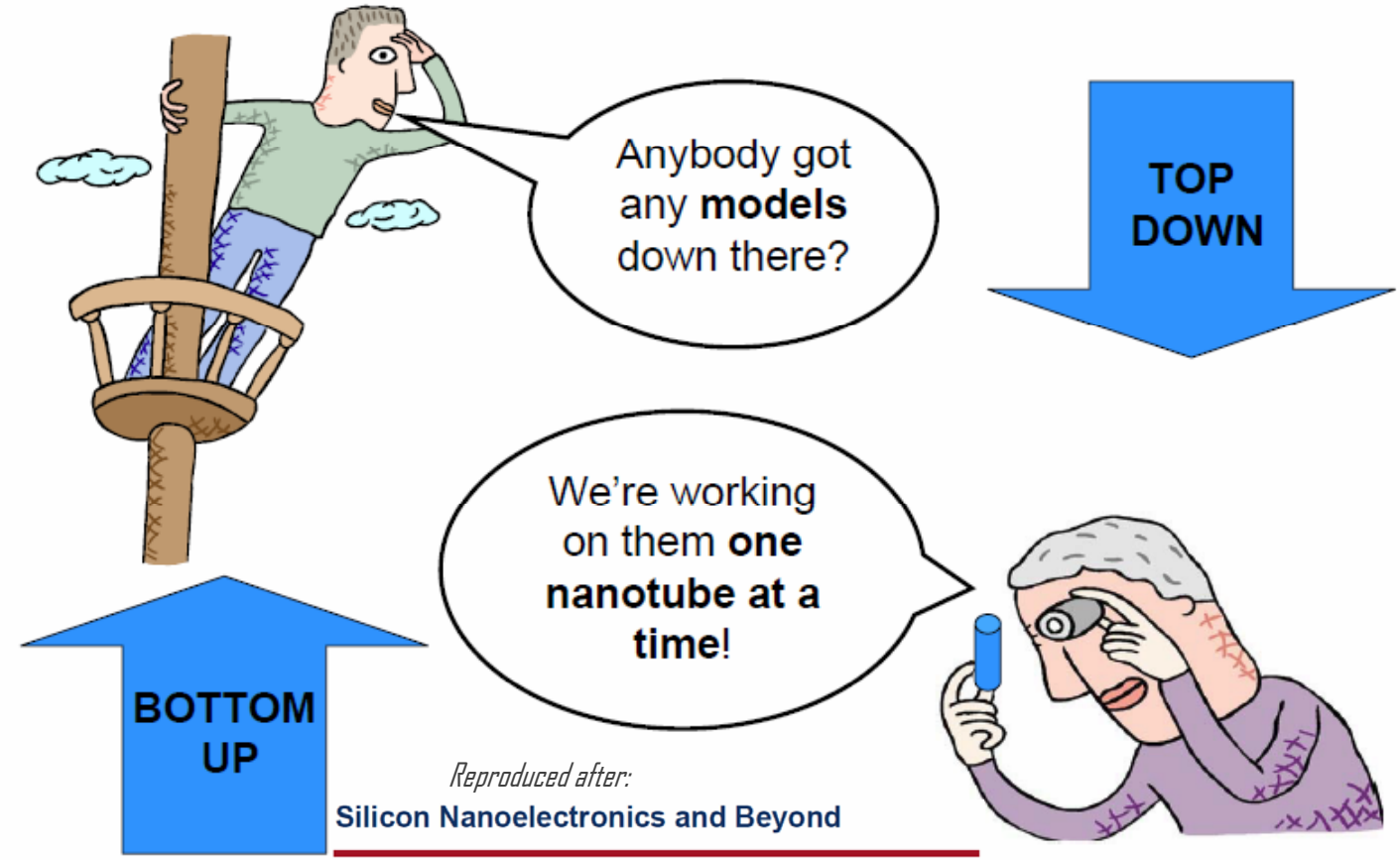
- **Large number of emerging "Beyond CMOS" device concepts**
  - Can those be used for data processing (computation/memory/interconnects…)?
  - Device fabrication: manufacturability? Variability? Reliability?
  - Architectures, design tools, libraries?





"Beyond CMOS" technologies: Towards design libraries?

The System/Circuit Designer and the Technologist Start from *Different Places*



Reproduced after:

Silicon Nanoelectronics and Beyond

William H. Joyner, Jr.
Director, Computer-Aided Design and Test, SRC
william.joyner@src.org 919-941-9472

September 13, 2005

"Beyond CMOS" technologies: Benchmarking Methodology

Workshop2:
"Benchmarking of new beyond CMOS device concepts"
on 10/13-14/11
in Athens

NANO-TEC **Benchmarking Beyond CMOS Devices**

Technology	[Wires, graphene, MEMS etc… please insert name]
Gain **Signal/Noise ratio** **Non-linearity**	
Speed **Power consumption**	
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	
Other specific properties	
Manufacturability **(Fabrication processes needed, tolerances etc.)**	
Timeline **(When exploitable or when foreseen in production)**	

Technologies under scope:

- *Molecular Electronics*
- MEMS
- Solid-State Quantum Computing
- Spintronics
- *Nanowires*
- *Memristors*
- *Graphene*

Charge based Beyond CMOS, Non-Conventional FETs

Presentations of WS2 are available at:
https://www.fp7-nanotec.eu/workshop2/presentations

Slides re- Mol. Electronics, Memristors and Graphene transistors:
Courtesy Dr. D. Vuillaume, Dr. J. Bollier and Dr. J. Kinaret (Workshop 2)

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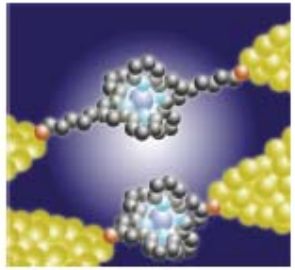
Building Bridges: Molecular Electronics (1/3)

single molecule electronics

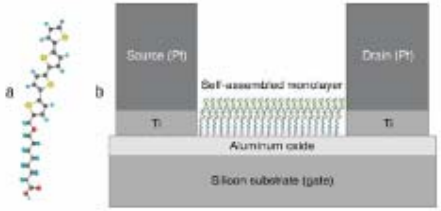


L < a few nm
t < a few nm

basic science
knowledge development

no foreseen applications
in a reasonable time-scale

self-assembled molecular electronics



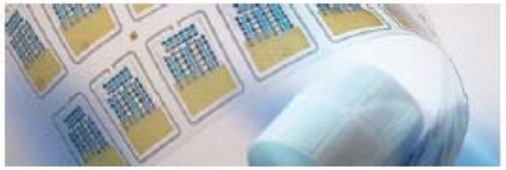
L ~ tens nm - µm
t < a few nm

basic science
knowledge development

possible applications
foreseen

SAMFET

thin-film molecular electronics



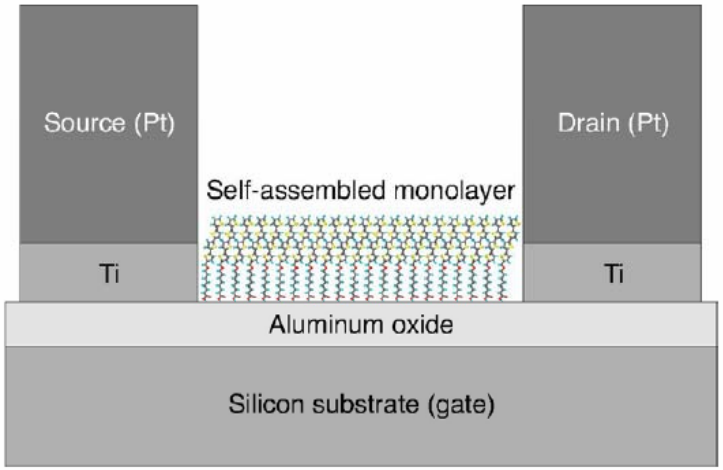
L > µm
t > few 10 nm

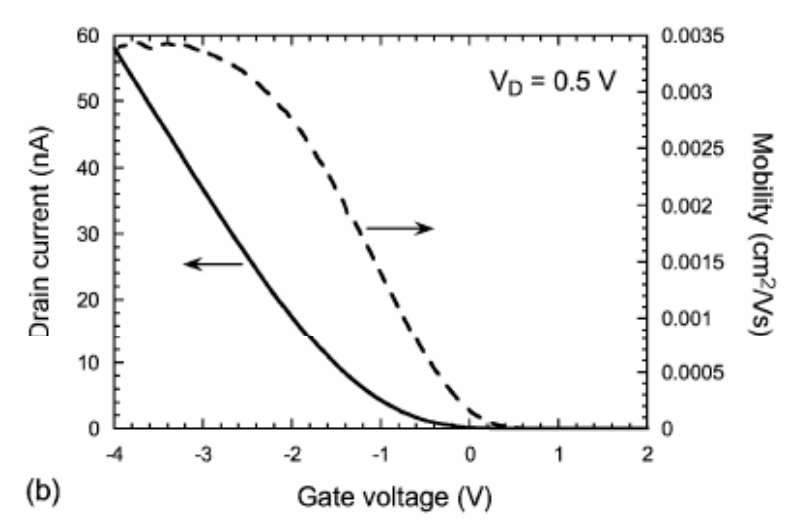
plastic electronics
(OLED, OFET, OPV)

some products already
commercialized

Building Bridges: Molecular Electronics (2/3)

- **SAMFET: Self-Assembled Monolayer Field Effect Transistor**
  - Built by immersing a silicon substrate into a solution containing liquid crystalline molecules that self-assemble onto this substrate, resulting in a semi-conductive layer, a single molecule thick.
  - The monolayer of the SAMFET consists of molecules that are standing upright. Conduction takes place by charges jumping from one molecule to the other.
  - As the length of the SAMFET increased, its level of conductivity decreased exponentially.
  - The SAMFET can be used to make sensors that give a large signal that is triggered by a small change.





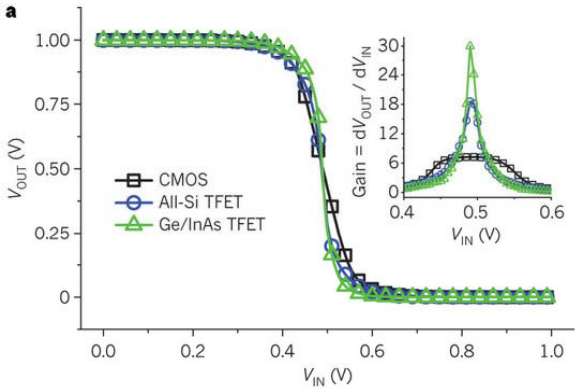
Building Bridges: Molecular Electronics (3/3)

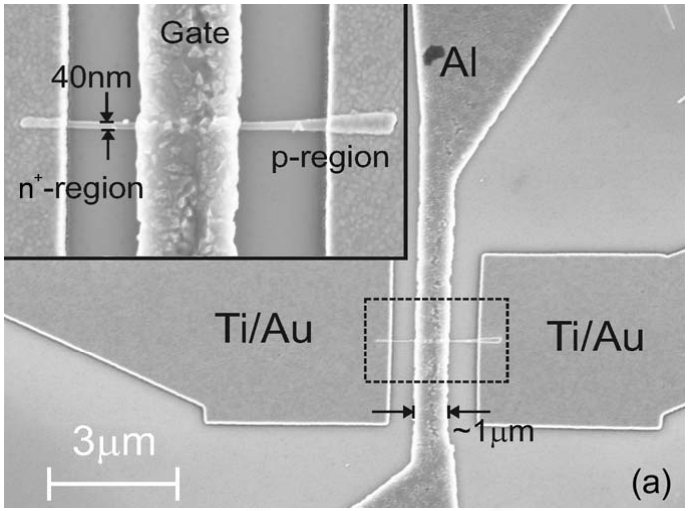
Benchmarking Beyond CMOS Devices

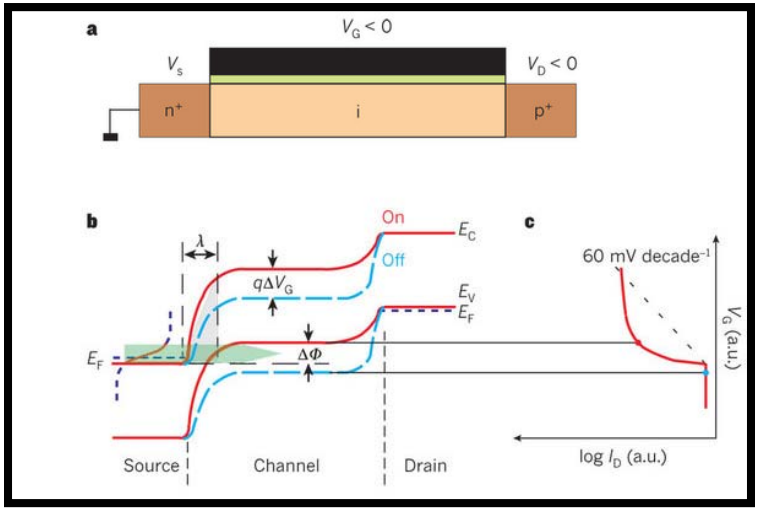
Technology	Self-assembled molecular electronics
Gain/restoring level **Signal/Noise ratio** **Non-linearity**	Ok with SAMFET (to be optimized), (2-terminal junctionlow current (G_0 max) Noise not yet studied (a few publications) Mol junctions are mainly non-linear
Speed **Power consumption**	low low (50 zJ/mol switch)
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	molecule-NP 2D and 3D arrays could implement some functions (e.g. reconfigurable logic, neuro-inspired function)
Other specific properties	almost infinite combination of molecules, adjustable by chemistry, specific design (1 molecule = 1 function)
Manufacturability (Fabrication processes needed, tolerances etc.)	solution process, compatible with flexible substrate. Defect control? large variability (but not a problem if we envision ANN applications)
Timeline (When exploitable or when foreseen in production)	> 5 - 10y (if ever?)

Building Bridges: Nanowire Transistors (1/5)

- **Tunnel Field Effect Transistors (TFET)**







BTBT across the source-channel junction
Controlled by the gate-to-source bias

Advantages

- Low power
- CMOS-toolset compatible

Challenges

- Drive current enhancement - scalability
- Shallow tunnel junctions engineering
- Steep subthreshold slope on a limited voltage range

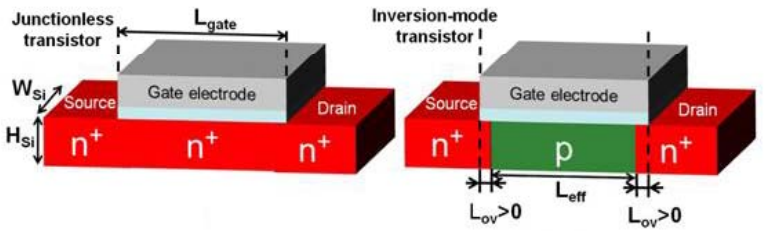
Building Bridges: Nanowire Transistors (2/5)

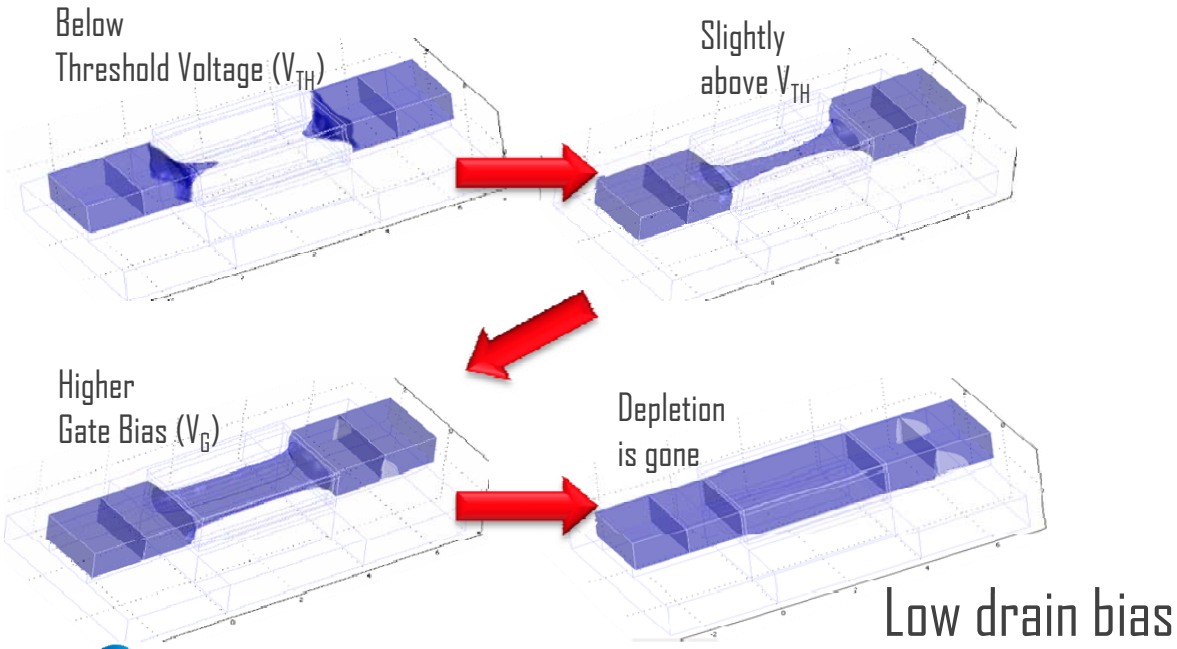
Benchmarking Beyond CMOS Devices

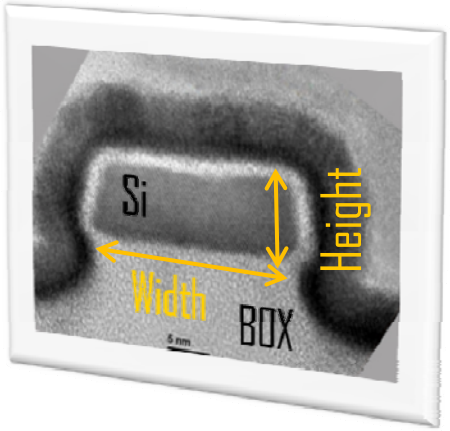
Technology	Tunnel FETs
Gain **Signal/Noise ratio** **Non-linearity**	Similar functionality than MOSFET but promises lower voltage and lower power consumption, I_{on} may be smaller, Potentially better noise margin and high gain at extremely low current/voltage
Speed **Power consumption**	Depends on the I_{on} that can be achieved, probably not faster, maybe a little bit smaller Lower power consumption
Architecture/Integrability (Inputs/outputs, digital, multilevel, analog, size etc.)	Similar architecture, some circuit changes needed, may have density penality but there is room for new clever circuit designs.
Other specific properties	
Manufacturability (Fabrication processes needed, tolerances etc.)	SiGe TFET CMOS compatible, Integration of III-V heterojunction TFETs need more work but should be possible, junction quality, interface states, self-alignment critical, variability may be more critical due to exponential dependence of tunneling, V_T variation, doping tails and stochastic behavior of doping, high-k gate stack…
Timeline (When exploitable or when foreseen in production)	On the roadmap after GAA and conventional III-V → 5-10 years

Building Bridges: Nanowire Transistors (3/5)

- **Junctionless Field Effect Transistor**
  - Gated resistor
  - Pinch-off transistor
- **Full depletion in off-state, controlled by the gate-to-channel work function difference**





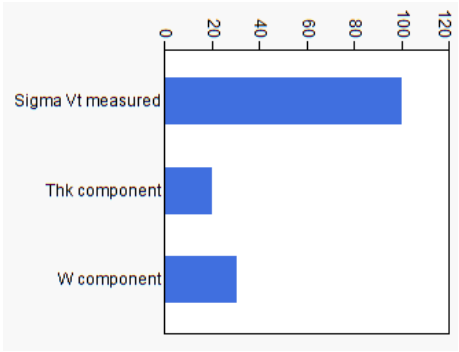


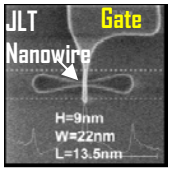
Silicon Quantum WIRE transistors (SQWIRE)
Collaborative project, Grant agreement no: 257111

Building Bridges: Nanowire Transistors (4/5)

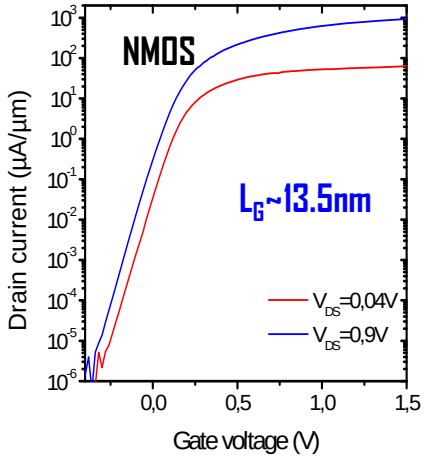
- **Advantages**
  - No shallow source/drain junctions required
  - 60mV/decade subtreshold slope at Room T
  - CMOS-toolset compatible, fabrication is simpler

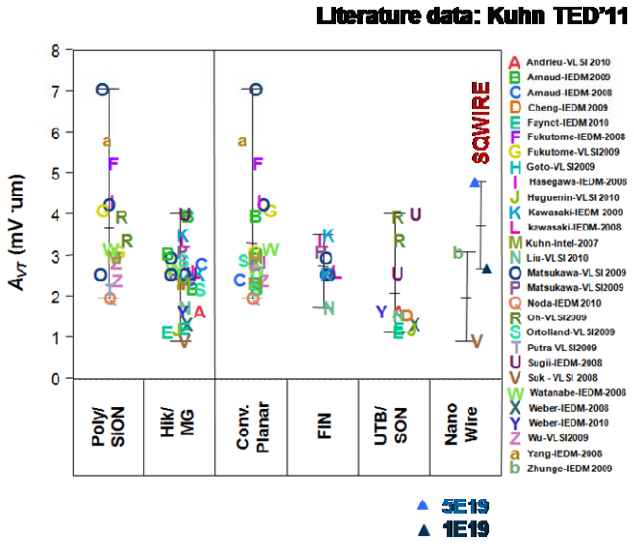
- **Challenges**
  - Drive current enhancement
  - Dimensions control





W=22nm
DIBL~120mV/V
SS~70mV/dec
I_{on}~454µA/µm
I_{off}~0.94nA/µm





Building Bridges: Nanowire Transistors (5/5)

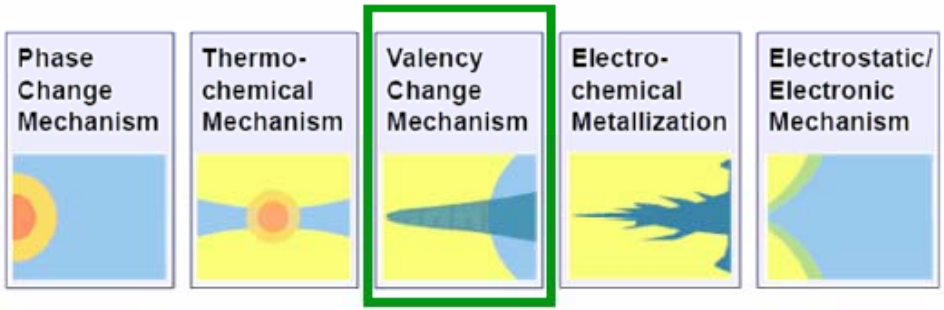
Benchmarking Beyond CMOS Devices

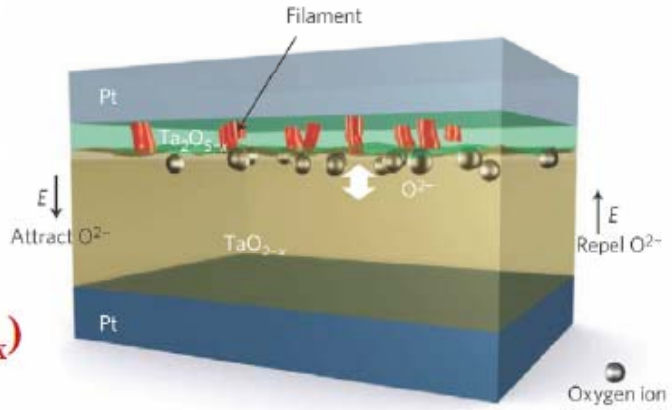
Technology	Junctionless Nanowire Field Effect Transistor (JNT)
Gain, Signal/Noise ratio **Non-linearity**	Not investigated yet (single-device characterization)
Speed **Power consumption**	CV/I: lower Miller capacitance than inversion mode FETs, SS~60mV/dec at V_{dd}=1V, I_{on} similar to IM FETs (contact resistance is the main issue!)
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	Same as FinFETs/GAA NW: high density required SOI is the substrate of choice (thermal dissipation issues?) Bulk Si OK
Other specific properties	
Manufacturability **(Fabrication processes needed, tolerances etc.)**	Fully CMOS compatible, no need for ultra- shallow junction engineering. Need for SOI thickness and LER control
Timeline **(When exploitable or when foreseen in production)**	Outperforms bulk Si GAA IM FETs at gate lengths < 25nm (in terms of SCE control), σ_{VT} being addressed,

Building Bridges: Switching Memristors (1/5)

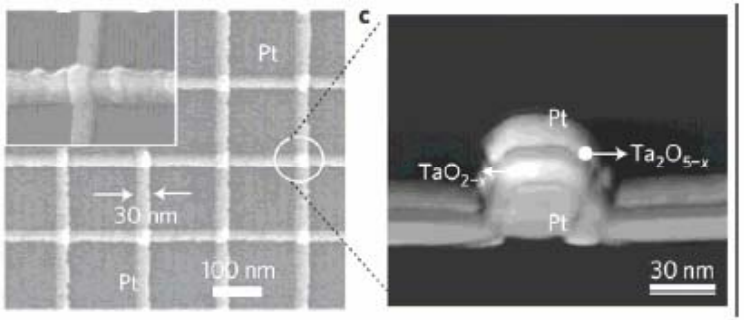
- **Combines the electrical properties of a memory element and of a resistor**
  - Memory switches
    - Resistance of the switch = f(voltage history)
  - Advantages
    - Faster and denser (memristors are small (< 50 x 50 nm^2)) than regular MOS transistors
    - Energy-efficient and Reconfigurable
- **Applications**
  - logic functions, FPGAs
  - NV RAM Technologies
    - Ferroelectric RAM (FRAM) as well as ferroelectric polarization memories made using organic materials
    - Phase-change memory (PCM) or phase-change RAM (PCRAM)
    - Conductive-bridging RAM (CBRAM)
    - Resistive RAM (RRAM or ReRAM)
    - Magnetic RAM (MRAM)

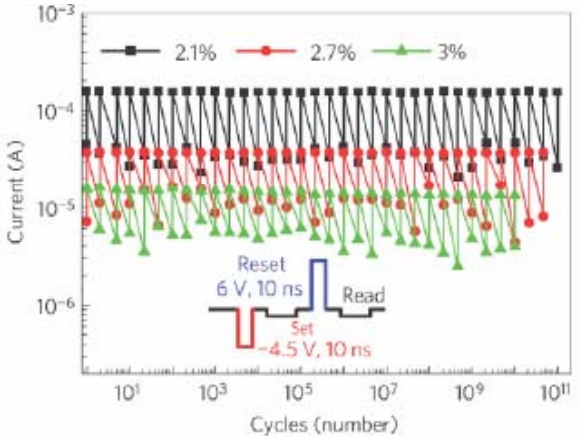
Switching Memristors (2/5)





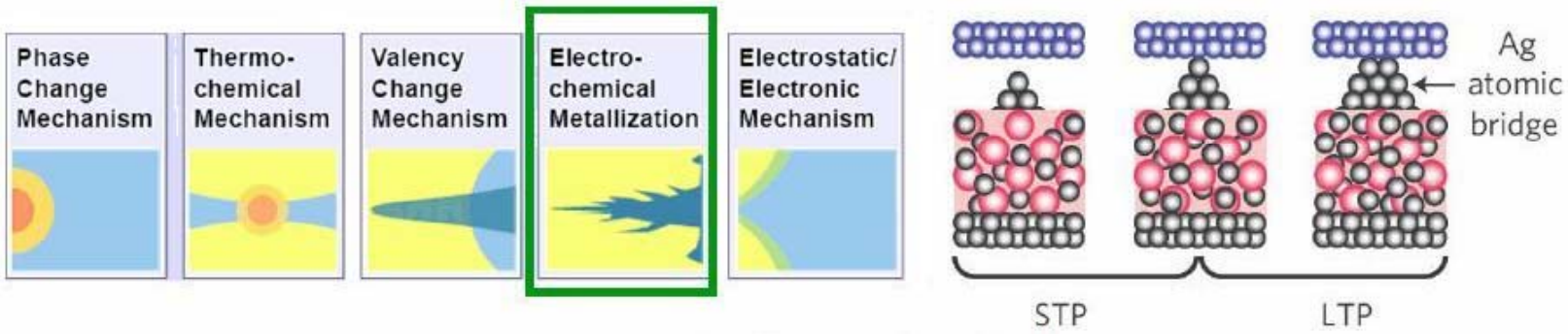
Lee et al., Nature Materials 2011 (Ta_2O_{5-x}/Ta_{2-x})



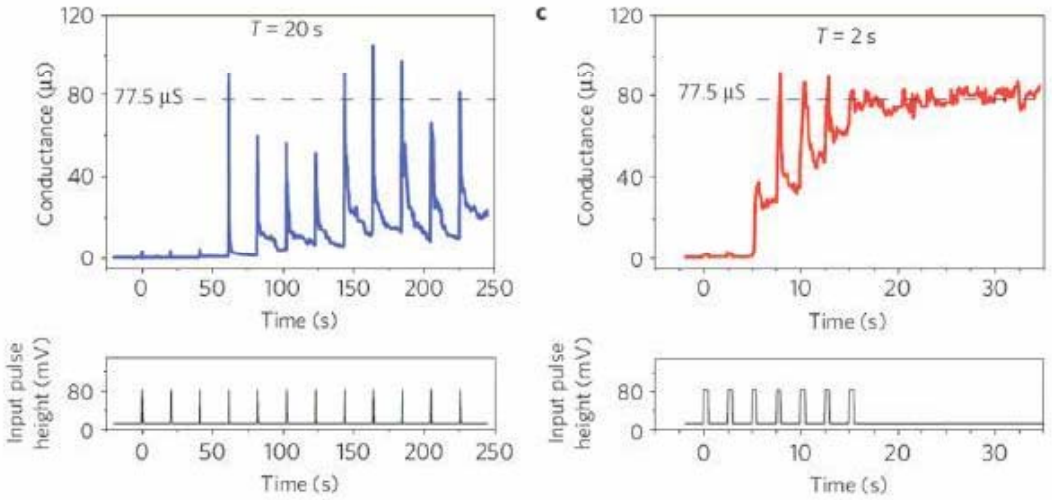


good cyclability > 10^{12}, fast (10ns) and reduced power consumption

Switching Memristors (3/5)

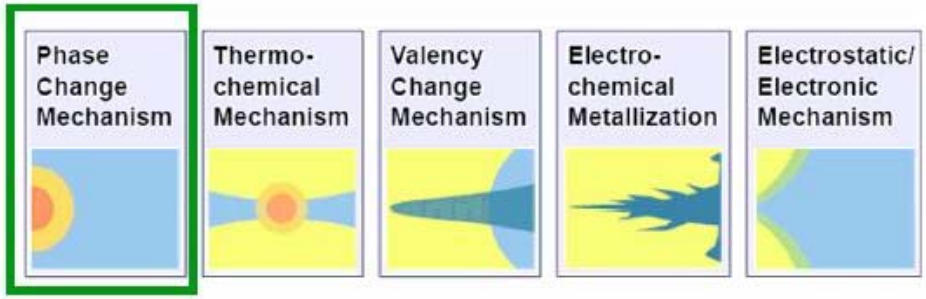


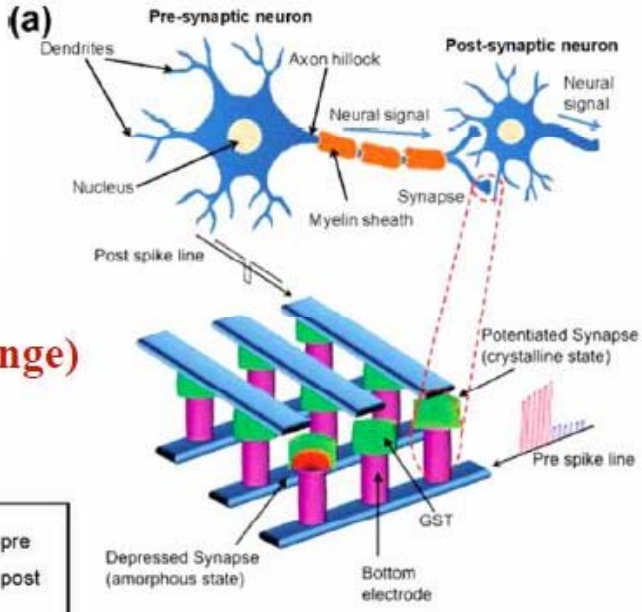
Ohno et al., Nature Materials 2011 (Ag_2S atomic switch)



Short AND long term potentiation ! STDP ? Cyclability ?

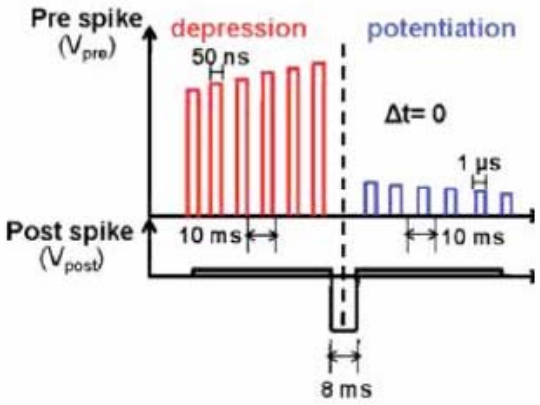
Switching Memristors (4/5)

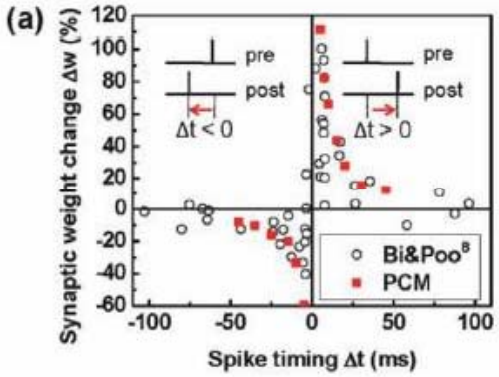




Kuzum et al., Nature Materials 2011 (Phase change)

see also : Wright et al., Advanced Materials 2011





Phase change : unipolar switching. STDP = yes, complicated ?

Switching memristors (5/5)

Technology *digital memristor*	PCM	Red-Ox	FeT	STT
Gain, Signal/Noise ratio **Non-linearity**			N/A	
Speed **Power consumption**	50 ns 6 pJ	10 ns < 1 pJ	10 ns 10 fJ	25 ns 0.02-5pJ
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	6 F^2	5/8 F^2	5/8 F^2	20/40 F^2
Other specific properties				
prototypes	commercial	some	---	yes
forming step	no	some	no	no
switching	unipolar	both	bipolar	bipolar
good theoretical understanding	yes	no	yes	yes
Manufacturability	CMOS compatible			
Timeline **(When exploitable or when foreseen in production)**	available	< 5 y	?	< 3 y

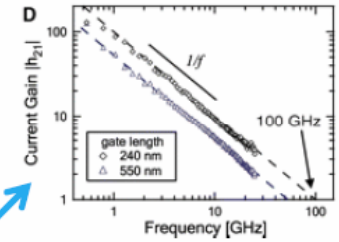
Graphene Transistors (1/4)

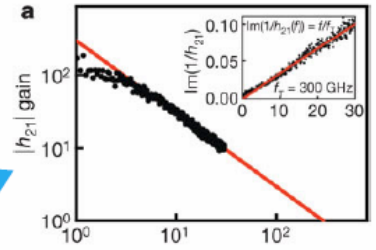
- Key improvement demanded:
  - Bandgap vs. mobility: high mobilities relate to gapless graphene → useless for digital electronics
  - Fabrication: bandgap extremely sensitive to surface roughness variations
- Benchmarking:
  - Criteria are available
  - Some are met, e.g..
    - Devices at room temperature
    - Integrability
- No „beyond CMOS“ due to lack of digital transistor:
  - ‘CMOS logic requires both n and p-channel FETs with well controlled Vt, and graphene FETs with these properties have not yet been reported’ (F. Schwierz, Nature Nano)

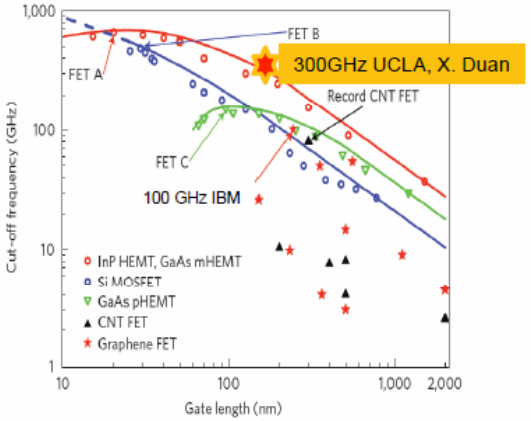
Graphene Transistors (2/4)

Analog electronics

- High mobility and high saturation velocity give promise for fast electronics
- Extrapolated performance
  IBM: f_T = 100 GHz @ 240 nm;
  UCLA: f_T = 300 GHz @ 144 nm
- Poor power gain due to absence of a gap
- Ambipolar: new design feature that enables novel devices (Palacios)







nature nanotechnology
REVIEW ARTICLE
PUBLISHED ONLINE: 30 MAY 2010 | DOI: 10.1038/NNANO.2010.89

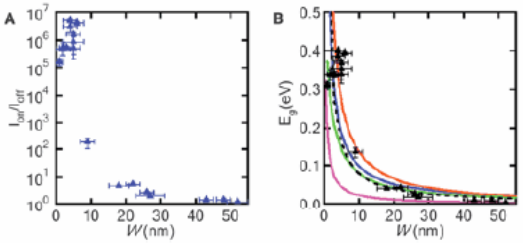
Graphene transistors

Frank Schwierz[1*]

Graphene Transistors (3/4)

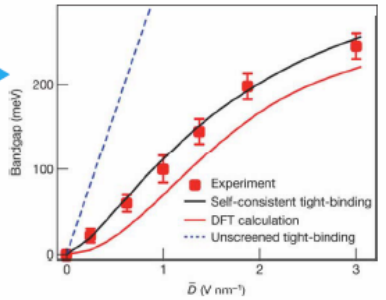
Digital electronics

- Challenge: absence of a band gap makes it hard to turn the devices off
- Old thinking: create a gap
  - Graphene nanoribbons (GNR)
    $E_g \approx 0.8$ eV nm/W
    - Lithographically: hard, need width 2-5 nm, good edges
    - Chemical synthesis: on metals, hard to position, no transport measurements exist yet
    - Unzipping of CNTs or synthesis inside a CNT



X.Li *et al.*, Science **319**, 1229 (2008)

  - Bilayer graphene with electric field: gap 100-200 meV, required V_{bg} ~100 V



Y. Zhang *et al.*, Nature **459**, 820 (2009)

  - Chemical modification (*e.g.*, nitrophenyl), gap 0.4 eV (S. Niyogi *et al.*, Nano Lett. **10**, 4061 (2010))
- New thinking: under research
  - BiSFET, tunnel FET, Veselago lens device: both BiSFET and tunnel FET are predicted to have very low switching energies, but they have not been demostrated experimentally

Graphene Transistors (4/4)

Benchmarking Beyond CMOS Devices

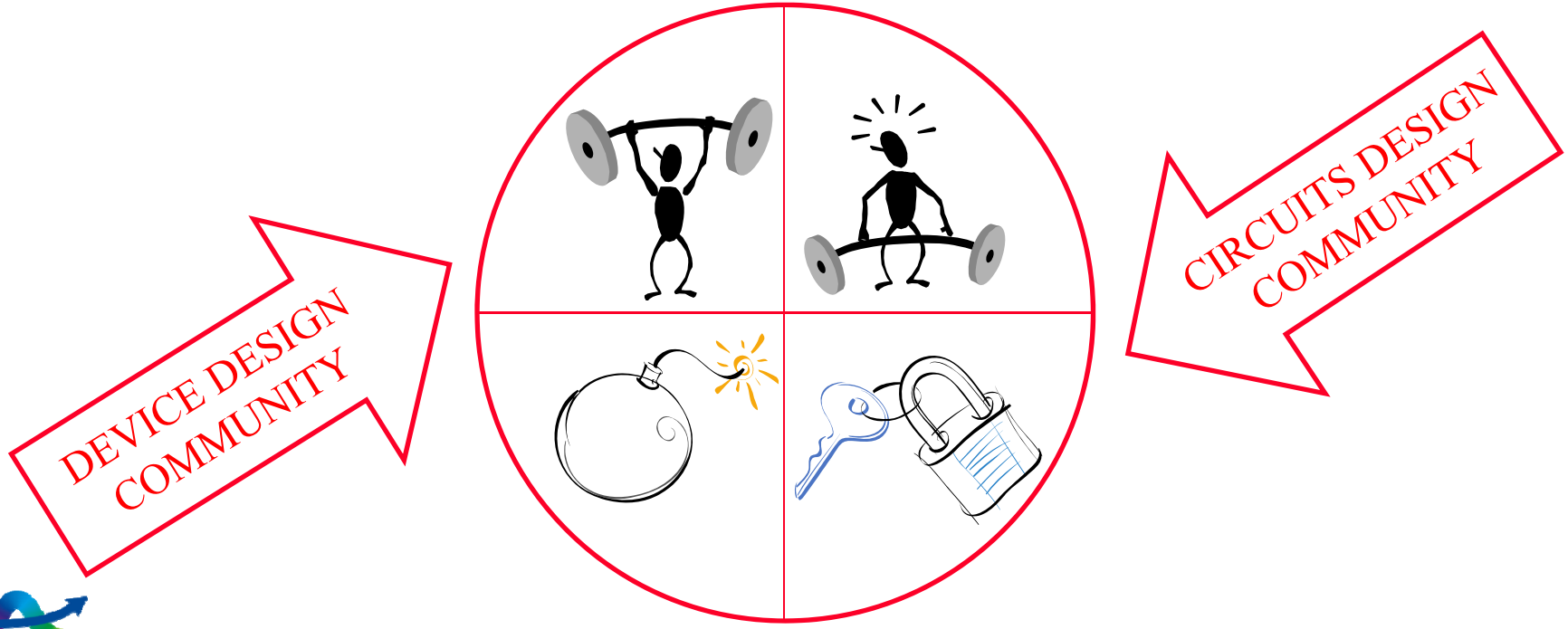
Technology	Graphene
Gain **Signal/Noise ratio** **Non-linearity**	Poor, would benefit from a gap
Speed **Power consumption**	High Low – high mobility, good gate coupling
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	Demonstrated integrability.
Other specific properties	System level integration - multifunctional
Manufacturability **(Fabrication processes needed, tolerances etc.)**	Mostly OK, except for ribbon fabrication Challenges in transferless fabrication
Timeline **(When exploitable or when foreseen in production)**	Optical and printable first (~2 years). Analog a few years later. Digital last. Non-standard devices (BiSFET etc.) not demonstrated yet.

Agenda

- About NANO-TEC
  - Objectives
  - Activities
  - Timeline
- 'Beyond CMOS' devices
  - Taxonomy
  - Motivation
  - Benchmarking Methodology
- Building Bridges
  - Molecular Electronics
  - Nanowire Transistors
  - Switching Memristors
  - Graphene Transistors
- Conclusion

Conclusion

- **Building bridges 'Technology/Emerging devices→ ← Architecture/Design'**
  - Device research: proofs of concept
    - limited amount of demonstrations at circuit levels
    - not enough data for current design tools
  - Logic / Memory applications: limited space for other types of application
  - Design Community: Join the discussion at the next NANO-TEC Workshop …



NANO-TEC Workshop 3:
"SWOT Analysis of the Technology–Design Ecosystem"

- **Time:** May 30-31, 2012
- **Location:** Hotel Beau Rivage Palace
  Lausanne, Switzerland
- **Fee:** free of charge
- **Deadline** May 15, 2012

- **Program:**
  - a series of plenary presentations on several selected technologies
  - a panel discussion on the programmatic and explorative perspectives of these technologies

- **Join the discussion on a SWOT Analysis of Beyond CMOS and tell the technology community about designer's needs**

References

- **Beyond CMOS devices (pictures)**
  - Mottaghi, M. et al. Adv. Funct. Mater. 17, 597–604 (2007) .
  - H. W. Schumacher et al., Applied Physics Letters 75(8) 1999.
  - http://www.nanoelectronics.ch/media/index.php

- **Molecular Electronics:**
  - K. Terabe et al., Quantized conductance atomic switch, Nature 2005:433. pp. 47-50.

- **Tunnel FETs:**
  - A.M. Ionescu et al. Tunnel field-effect transistors as energy-efficient electronic switches. Nature 2011; 479, pp. 329–337; K. E. Moselund et al. Silicon Nanowire Tunnel FETs: Low-Temperature Operation and Influence of High-k Gate Dielectric. IEEE Transactions on Electron Devices, 2011:58(9), p.911.

- **Gated Resistor:**
  - JP Colinge et al. Nanowire transistors without junctions. Nature Nanotechnology 2010; K. Kuhn et al., Process Technology Variation. IEEE Transactions on Electron Devices, 2011: 58(8), p.2197.

- **Memristors:**
  - Waser et al., Nature Materials 2007; Lee et al. Nature Materials 2011 (Ta_2O_{5-x}/Ta_{2-x}); Ohno et al. Nature Materials 2011 (Ag2S atomic switch); Kuzum et al. Nature Materials 2011 (Phase change) and Wrigth et al., Advanced Materials 2011.

- **Graphene Transistors:**
  - D. Reddy et al., J. Phys. D 44, 313001 (2011); F. Schwierz, Nature Nanotechnology 5, 487 (2010); S.K. Banarjee et al., Proc. IEEE 98, 2032 (2010); A. Venugopal et al., J. Appl. Phys. 109, 104511 (2011) and S. Bae et al. Nature Nano. 5, 571 (2010).