
# Tutorial: EU project NANOTEC on ECOSYSTEMS TECHNOLOGY & DESIGN for NANOELECTRONICS: an experience in Europe

*Half day Tutorial, Monday, September 17, 2012*

"Palais des Congrès" – Bordeaux Lac, allée Louis Ratabou, 33000 Bordeaux (F)

*Salle D2*

## Organization

This Tutorial is organized by the EU project NANOTEC

## Aim

The outcome of the EU project NANOTEC will be presented in this Tuitorial.

The project NANO-TEC (Ecosystems Technology and Design for Nanoelectronics) is a support action funded by the European Commission under number 257964. The aim of NANO-TEC is to address the gap between technology and design in Nanoelectronics in the area of Beyond CMOS. Within the scope of NANO-TEC, a number of workshops have been organized, where specific 'Beyond CMOS' device concepts were presented and discussed by experts in the field. Some categories of beyond CMOS devices were selected, that were benchmarked and a swot analysis was carried out. The outcome of this study will be presented during the tutorial by different partners of the project.

## Schedule

### 13:30 – 13:45 Welcome and introduction

A. G. Nassiopoulou, NCSR Demokritos, Athens, Greece / A.Nassiopoulou@imel.demokritos.gr

### 13:45-14:00 EU project NANOTEC on ECOSYSTEMS TECHNOLOGY & DESIGN for NANOELECTRONICS: an experience in Europe

Androula Nassiopoulou, NCSR Demokritos/IMEL, Athens, Greece

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While a recognised European strength is in heterogeneous integration, the academic community is also very strong in research addressing ways to carry out information processing operations using different concepts, state variables and associated technologies. A second aim of NANO-TEC is to consolidate and strengthen the academic community in Europe in the area of Beyond CMOS. This trend is presently decoupled from the research in design and it is this gap which weakens the impact of the progress being made in Beyond CMOS, since ways to realise devices operating under real conditions in a competitive manner to existing technologies are simply not viable without a design counterpart.

To this end NANO-TEC carries out a continued consultation and analysis of research needs and trends based on a workshop series with invited experts from the Americas, Asia and Europe covering topics such as Beyond CMOS device concepts and design, benchmarking and a SWOT analysis of new devices. Progress made so far towards the stated aims will be presented in this tutorial by the different speakers.

About NANO-TEC:

NANO-TEC is led by the Catalan Institute of Nanotechnology and is funded by the ICT theme of the 7$^{th}$ Framework programme of the European Commission. There are 10 partners involved in the NANO-TEC project besides the coordinator: these are Finnish Valtion Teknillinen Tutkimuskeskus, German Edacentrum GmbH and Foschungszentrum Juelich GmbH, Chalmers Technical University of Sweden, Polish Institute of Electron Technology, Delft University of Technology from the Netherlands, Greek National Centre for Scientific Research "Demokritos", Tyndall National Institute from Ireland, the Ecole Politechnique Fédérale de Lausanne and French Centre National de la Recherche Scientifique. All the partners are experienced in working in large consortia distributed over the European Union and contribute their organisational and integrative expertise together with visionary research and ambitious goals. The scientific and social challenges of NANO-TEC can only be achieved with a constellation like NANO-TEC aided by global experts and strong links to industry, which will ensure abroad coverage of its topic at European level.

NANOTEC website: www.fp7-NANOTEC.eu

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### 14:00-14:30 Benchmarking of Beyond CMOS

Jouni Ahopelto, VTT Technical Research Centre of Finland, Helsinki, Finland

Beyond CMOS devices can range from molecular electronics to quantum computing, exploit other state variables than charges and have a very wide span in maturity. This makes benchmarking challenging and direct comparison of devices practically impossible. Semiconductor Research Corporation carried out a few years ago in US benchmarking of emerging devices against state of the art CMOS switches and the results were promising[1]. Within NANO-TEC we have benchmarked devices from the following categories: Molecular Electronics, MEMS, Solid-State Quantum Computing, Spintronics, Nanowires, Memristors and Graphene, and tried to take into account the specific properties of each of the device families. We will describe the methodology used and give

some examples of the outcome. We will also address some of the difficulties identified during the benchmarking exercise.

[1] Bernstein et al., Device and Architecture Outlook for Beyond CMOS Switches, Proc. IEEE 98 (2010) 2169.

### 14:30-15:00 A SWOT Analysis of 'Beyond CMOS'

Mart Graef, DIMES, Delft Institute of Microsystems and Nanoelectronics, Delft University of Technology, The Netherlands

CMOS-based technology has been the backbone for the semiconductor industry for many decades, and over this period it has been the essential enabler for the continuation of Moore's Law. However, the CMOS device architecture has constraints that will limit its applicability in the future. These limitations are associated with physical barriers (entering atomic dimensions), economic considerations (manufacturing costs) and new trends in nanoelectronics (from 'More Moore', i.e. monolithic digital systems to 'More than Moore', i.e. heterogeneous multifunctional systems).

One of the objectives of the NANO-TEC coordination action is to charter the technology landscape that lies 'beyond CMOS'. This is achieved by assessing the requirements for proposed new device concepts, selecting the most promising technologies and designs, benchmarking these against existing devices, and performing a SWOT analysis for the benchmarked devices.

Within the scope of NANO-TEC, a number of workshops have been organized, where specific 'Beyond CMOS' device concepts were presented and discussed by experts in the field. The 3rd of these workshops, held in May 2012, focused on a SWOT analysis of 'Beyond CMOS' options. The topics that were reviewed included the level of maturity of these technologies, design issues, scientific challenges, compatibility with existing semiconductor processing, application perspectives, and infrastructural aspects. The results of this SWOT analysis will be presented and discussed.

### 15:00-15:30 Case study: The case of nanowire transistor

Guilhem Larrieu, LAAS-CNRS, Toulouse, France

The aim of NANOTEC is to explore the potential of the technologies claimed for the "Beyond CMOS" era. The strategy is not to directly compare, to "benchmark", the performance of the emerging devices against the current state-of-the-art CMOS devices but rather more like mapping and identifying the potential for future ICT applications, bearing in mind that some relevant properties are required to be fulfilled. The challenges include, among others, power consumption, speed, integration prospects, flexibility for new architectures and manufacturability. The parameter windows facilitating integration of the selected devices should be estimated and a frame for potential architectures to run a logic application should be sketched, including identification of the possible improvements in device properties and the bottlenecks in fabrication. Several key parameters have been selected and will be discussed.

In order to show our analysis procedure, we will provide an example of candidate in the field of 'Beyond CMOS' devices: the nano-wire transistors. This device will illustrate the benchmarking and integration criteria in particular scalability, manufacturability, reliability and reproducibility.

**15:30-16:00 Coffee Break**

**16:00-16:30 Information processing paradigms of the post CMOS era: devices and architectures.**

Alain Cappy, IEMN-UMR, Villeneuve D'Ascq, France

The energy efficiency becomes an essential criterion used for information processing technologies. It is indeed for energetic reasons that the scaling down rules (R. Dennard, 1974) that guided the evolution of the micro- and nanoelectronics for almost 40 years cannot be any more applied today. The consequences of this change are manyfold: the stagnation of the clock frequency (2-3 GHz since 2004) and the bigger complexity of microprocessor architectures (multicore). The rather bad energy efficiency of the current systems also constitutes a brake in the development of mobile applications and its impact on the environment (electric consumption) becomes more and more significant.
It becomes thus urgent to propose new paradigms of information processing capable of reducing the energy consumption in a drastic way while improving the performances as well. Based on multiple disciplines (thermodynamics, material physics, nanosciences and the nanotechnologies, information theory, computer science, neurosciences) researches on these new paradigms need necessarily a multidisciplinary approach covering, at a minimal level, the material ( devices fabrication) and software aspects (system architecture, circuit design…).
After a presentation of the scientific and technological questions which arise, we will propose some possible ways for information processing of the post CMOS era. We will show in particular the interest of neuromorphic architectures for many applications, in particular, image processing.