Contract N° 257964

NANOTEC
Ecosystems Technology and Design for Nanoelectronics

Coordination Action
Information and Communication Technologies

Deliverable 6.4: Workshop3 report on technology design interactions in Beyond CMOS

Due date of deliverable: M22
Actual submission date: M24

Start date of project: 1 September 2010 Duration: 30 Months

Organisation name of lead contractor for this deliverable: Ecole Polytechnique Fédérale de Lausanne

Revision [ ]

Approval

WP Leader	☒	**Coordinator**	☒

Project co-funded by the European Commission within the Seventh Framework Programme (2007-2012)		
Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission	
CO	Confidential, only for members of the consortium (including the Commission Services)	

Partner	Short description (1-3 sentences) of partners contribution to this deliverable
Chalmers	Discussant
CNRS-LAAS	Rapporteur
EPFL	Local workshop arrangements and preparation of deliverable
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ECN	Rapporteur on the Design and Technology Panel Discussion
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TU-Delft	SWOT analysis
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1. Aim of this Deliverable

The 3rd NANOTEC workshop was jointly organized on May, 30-31, 2012 in Lausanne, Switzerland. Its program included a series of plenary presentations on several selected technologies, followed by a panel discussion on the programmatic and explorative perspectives of these technologies in which the results of the SWOT analysis were assessed. This report gathers the technology - design interactions in the Beyond-CMOS domain discussed at the workshops.

2. Workshop Sessions

2.1. Solid-state Quantum Computing

Over past decades, quantum information science has emerged to seek answers to the question: can we gain some advantage by storing, transmitting and processing information encoded in systems that exhibit unique quantum properties? A number of physical systems, spanning much of modern physics, are being developed for quantum computation. Solid-state quantum computation based on the intrinsic two level dynamics of electron spin in semiconductors has attracted widespread attention because the enormous resources of conventional electronics can in principle be applied to develop a scalable quantum computer (QC). In this context, solid-state spins in an applied magnetic field are attractive qubit candidates since they comprise perfect two level systems with potentially long coherence times. Similar examples of possible QC implementation include: Ion qubits in electrostatic/dynamic traps, Atom qubits in crossed-laser traps, Spin qubits in molecules, Quantum dots (QD), Spin qubits in solids, Superconducting Josephson junction (JJ) qubits and circuits as well as Photonic flying qubit circuits. Declaration of the QC technology scalability is a complex task, because the resources used to define and control a qubit are diverse. They may include space on a microchip, classical microwave electronics, dedicated lasers, cryogenic refrigerators, and so on. For a system to be scalable, these 'classical' resources must be made scalable as well, which invokes complex engineering issues and the infrastructure available for large-scale technologies.

A large-scale quantum computer is certainly an extremely ambitious goal, now appearing as large as, fully programmable classical computers must have seemed a century ago. Ultimately, a valuable comparison must examine complete architectures of quantum computers that enumerate the resources required to finish algorithms of relevant sizes with negligible error.

Important progress has been achieved within last years in US and in Europe in the QC experiments involving 3 and 4 qubits using a Josephson Junction approach, achieving a measurement-based state initialization and measurement-based feedback. However, these experiments required very low, cryogenic temperatures. At present, the possibility to implement a QC concept at a room temperature using a defect structures or QDs in diamonds and in III-V semiconductors is being investigated.

Open Technology-Design issues:

- A simple use of the CMOS technology to implement a QC is not yet possible.
- The coherence time, which makes a real multi qubit QC system, is not long enough.
- The small prospect of implementing a QC in systems operating at room temperature is seen as a major obstacle.
- Development of new algorithms broadening applicability of QC to new domains remains a challenge.

- Engagement of the quantum information science community in design and architecture research collaborations.
- Cost factor of QCs with respect to their present classical counterparts.

2.2. Molecular Electronics

Manipulating and controlling the self-organization of small collections of molecules, as an alternative to investigating individual molecules, has motivated researchers bent on processing and storing information in molecular electronics (ME). Although numerous ingenious examples of single-molecule devices have provided fundamental insights into their molecular electronic properties, ME incorporating hundreds to thousands of molecules trapped between wires in two-dimensional arrays within crossbar architectures offers a glimmer of hope for molecular memory applications. Independently, ME can be divided in three different parts: molecular charge transport, molecular switching and molecular logic.

Several questions were raised about the current status of ME devices, technologies and manufacturability: conductance stability, reproducibility of the system metal-molecule-metal, the relation between organic electronics and molecular electronics, device encapsulation requirements for better stability, the efficiency of the molecule switching stimuli as well as the molecular design, almost inexistent. It was also emphasized that logic is probably not the only application for molecular electronics: molecules show also analog properties that can be used for sensing for instance.

To overcome the CMOS/nanodevice interface problem the co-integration of CMOS circuits and molecular devices, known as hybrid semiconductor-molecular electronics or the CMOL approach, interface is provided by sharp-tipped pins distributed over the circuit area on the CMOS stack. In such circuits, two-terminal nanodevices provide programmable diode functionality for logic circuit operation, and allow circuit mapping and reconfiguration around defective nanodevices, while the CMOS subsystem is used for signal restoration and latching. Using custom-developed design automation tools we have successfully mapped on reconfigurable general-purpose logic fabric (“CMOL FPGA”) reaching ~Tbit/cm^2 benchmark circuits and estimated their performance.

Open Technology-Design issues:

- Potential routes to integration, interconnects and problems related to design and architecture need to be found (low conductivity and interconnects).
- Specific molecular designs, which can benefit from a specific molecular behaviour
- Concerning integration, the exploration of hybrid semiconductor-molecular electronics (CMOL) approach) is a potential option.
- Two-terminal nanodevices would be naturally incorporated into nanowire crossbar fabric, enabling very high function density probably at acceptable fabrication costs.

2.3. Nanowires

Over the last 40 years, the semiconductor industry has been driven by the scaling of CMOS field effect transistors to smaller dimensions. Scaling has increased computing capability densities up to a point where the power dissipation in heat during computation has become a serious limitation. SNWs represent

a unique system with novel properties associated to their one-dimensional (1D) structures. They can potentially provide a strong platform to explore the various scientific aspects in these nanostructures.

Emerging Beyond-CMOS concepts based on silicon nanowires, graphene and CNTs may be potential candidates for replacing or extending CMOS. They have the potential operation up to THz frequencies and individual advantages, e.g. ambipolarity, and the high linearity of CNT devices.

Open Technology-Design issues:

- Contact formation and minimization of contact resistance.
- The absence of a saturation region, e.g., as in graphene FETs, leads to large transconductance, which has to be reduced to improve their poor intrinsic voltage gain to values well above unity.
- Fabrication of large number of parallel wires needed to obtain high currents required by the IC designs remains a challenge for RF-IC design using recently available technologies.

2.4. Spintronics

Spintronics, the technology of control and manipulation of the spin state of electrons and nanomagnets, is a promising approach for Beyond-CMOS logic, memory and analog IC applications. Several spin-based devices have been proposed in the literature with the possibility of logic-no volatility, intrinsic directionality, higher logical efficiency (large fan-in/fan-out) and re-configurability. Combined with novel approaches for memory hierarchy and logic architecture, spintronics may enable high performance, normally-off (with zero standby power) and instantly-on computing systems. Understanding the principles to analyse integrated spintronic circuits and describing the physics of spin transport that can be utilized by SPICE/CAD developers, and subsequently by circuit and system designers, for the exploration of spintronics for Beyond-CMOS computing. Selected examples using classical spintronics in logic devices for information processing comprise transmission, spin torque oscillators as potential radiating antenna for GHz-communication as well as spin-calorimetric and spin-topotronics. The versatility of spintronic devices and emerging applications such as spin transfer torque RAM, heat assisted switching RAM or the race track memory concept have been recently proposed by IBM.
Spintronics as a new concept is facing research challenges and still require new fundamental physics and additional scientific work to fully explore novel spintronic-related discoveries, some of them still in their infancy.

Open Technology-Design issues:

- Interconnects
- Reliable contacts
- Specification of real applications
- Spintronics SPICE/CAD in progress.

2.5. Graphene

Graphene, a layer of carbon atoms arranged in a hexagonal lattice, is being heralded as a promising candidate for future high-speed electronics and radio-frequency (RF) applications because of its high carrier mobility and saturation velocity. The planar structure and the announced feasibility of large-area graphene synthesis would facilitate the adoption of top-down device fabrication techniques. Graphene

transistors, with intrinsic cut-off frequencies above 100 GHz, have been recently achieved by several groups using graphene films synthesized by various methods, including epitaxial growth on SiC, chemical vapor deposition (CVD) on cupper, and mechanical exfoliation. The monolithic integration of graphene transistors with interconnects and other components are an essential requirement for any semiconductor material to achieve a widespread technological impact.

Open Technology-Design issues:

- Material variability at the device level (the mobility depends on host substrate and on the gate oxide used).
- Electrical contacts (more difficult than for Si device)
- Scalable integration into practical circuits (different ohmic contact formation mechanism, poor adhesion with metals and oxides, and its vulnerability to damage in plasma processing).
- Huge gap between a single device and a practical graphene circuit on wafer scale.

2.6. MEMS

Progress in MEMS is driven by increasing number of functions per chip area. The diversity of the MEMS technologies belongs to the More than Moore field. It is a very broad field mainly characterized by diversification, both as it concerns the materials and technologies and the applications. The design of micro systems, MEMS or mechatronic systems is characterized by a variety of design approaches for subsystems and components. Design errors, unclear specification and incompatibilities between subsystems are therefore often identified very late in the design process and cause additional cost and design cycles.
In Beyond CMOS and More than Moore it is switching that makes M/NEMS attractive due to the promised low insertion losses, better non-linearity and control powers three orders of magnitude lower than semiconductor switches. However, the electrostatically driven switches need actuation voltages of about 40 V. Recently, a news form the Fraunhofer Institute for Electronic Nanosystems ENAS[1] reported switching time < 10 microsecond and 1 billion switching cycles.

Open Technology-Design issues:

- Reliability (switch becomes locked in one status when contacts stick or by charging effects in the insulating material.
- Contamination of metal contacts and gradual increase of insertion losses.

2.7. Neuromorphic Computing

Historically, electrical circuits were crafted with three basic building blocks: the capacitor, the resistor, and the inductor. But in 1971, Professor Leon Chua (UCB) has predicted the existence of a fourth: the memristor, short for memory resistor. Like an ordinary resistor, a memristor would create and maintain a safe flow of electrical current across a device, but unlike a resistor, it would “remember” charges even when it lost power. This would allow it to store information, i.e., serve as computer memory. In May

[1] http://www.mikroelektronik.fraunhofer.de/en/press-media/microelectr...ws/article/hf-mems-schalter-mit-niedriger-aktuierungsspannung.html

2008, Hewlett Packard announced that it had built a memristor. One of the potential key applications of memristors is in Neuromorphic Computing. Memristors fall generally under four types including inorganic and organic devices. The latter has time scales that place it within the Beyond-CMOS device concepts.

Open Technology-Design issues:

- Material variability at the device level.
- Defect tolerances and the reversibility of the thermodynamic processes involved.
- Selection of a memristor type for devices for neuromorphic computing applications.
- Test algorithms and their transferability.

2.8. Beyond-CMOS: From Technology to Application – panel discussion

The panel discussion was focused on a few key questions related to the NANO-TEC SWOT analysis [8]. The session chair and the panellist were trying to answer following questions: Which types of applications will be the drivers for Beyond-CMOS? Will they all compete for the same killing application, or will they share the market? Will design challenges be different for different applications? Can design tools be the discriminating factor for the success of one specific technology? Present design tools are a huge legacy: what can trigger the investment needed for new tools? Selected answers are available [9] - [10].

Chair:
Dr. Livio Baldi, Micron Technology Inc., Milan;
Panelists:
Prof. Dr. Wolfgang Rosenstiel, edacentrum and University of Tübingen;
Prof. Dr. Paolo Lugli, Technical University of Munich;
Prof. Dr. Giovanni de Micheli, École Politechnique Fédérale de Lausanne;
Prof. Dr. Sandip Tiwari, Cornell University, Ithaca, N.Y.

Figure 1: Panel discussion. Left: Dr L Baldi. Middle: Profs Dr W Rosenstiel and G de Micheli. Right: Profs Drs S Tiwari and P Lugli.

To begin with, Livio introduced the discussion reminding the audience that it took 50 years and a few hundred billion dollars to go from a few transistors to the present complexity and that despite this effort design is still a limiting factor in CMOS integration density. With this background and looking at the new beyond CMOS technologies he formulated several questions inviting the answers from the panellists and during the discussion:

1. What can a new (beyond CMOS) technology do to improve the situation of CMOS and who is going to pay for it?

2. Which types of applications will be the drivers for ‘Beyond CMOS’?
3. Will they all compete for the same killing application, or will they share the market?
4. Will design challenges be different for different applications?
5. Can design tools be the discriminating factor for the success of one specific technology?
6. Present design tools are a huge legacy: what can trigger the investment needed for new tools?

The panellists took the opportunity to give their point of view on the situation.

Sandip stated that design, as a limitation in CMOS integration density, is a self-inflicted wound. This is because of the steadily growing complexity met only by the introduction of hierarchy and because of the growing number of constraints, e.g. due to energy consumption. As these aspects have not been considered during the creation of the CMOS design process itself a now “creeky infrastructure” has been developed which is hardly able to cover today’s CMOS design problems. Therefore, Sandip demanded a *stronger foundation of the design at system level, in order to be able to stand the design challenges using new technologies*.
With respect to the possible drivers for ‘Beyond CMOS’, Sandip mentioned ultra-low power microsystems, machines with learning or inference capabilities and effective education platforms. Sandip agreed that design challenges depend on the given application although he also sees common aspects. As Apple is now successful with good design, Sandip is convinced that design tools can be the discriminating factor for the success of one specific technology because a design tool is the codification of a design process and it is its mathematical translation which itself makes the difference. Additionally, Sandip named the *energy challenge* and the *application challenge due to the changing society* as triggers of the investment in new tools that could break the huge legacy of present design tools.
Finally, like in the previous NANO-TEC workshop, Sandip demands for a *new open infrastructure* that brings people and things together. He characterizes this as an international national-scale problem that crosses frontiers of many disciplines, that needs a cooperative effort with much thinking at its start and long project duration under a unified leadership.

Wolfgang introduced his position with a characterization of design stating that every circuit being designed today, starts with a computational model at a high level of abstraction, then goes through a sequence of synthesis and optimization transformations, followed by rigorous digital simulation and prototyping, as well as formal and semi-formal verification, before it is finally manufactured via advanced lithographical and chemical processes.
In order to be able to design efficiently, an automation process (Electronic Design Automation) has been established. This came out of one of the earliest inter-disciplinary collaborations: Computer scientists and engineers in EDA collaborated successfully with the electrical engineers to derive various levels of circuit models, physicists and chemists worked together to find manufacturing models, theoretical computer scientists conducted various kinds of complexity analyses while applied mathematics and optimization experts improvised highly scalable simulation and synthesis algorithms and while application domain specialists to develop intellectual property (IP) libraries, etc.
In the end, according to Wolfgang, a design process turned out. Thus, to bring an application to a chip implementation, what design will need are *suitable algorithms*, implement them in a computational model using a language coming to an architecture consisting of functional blocks, containing logic gates implemented by circuits built out of devices that are made of materials in a certain structure following the laws of physics and chemistry. As this design process between application and device is well established in its middle, *the difficulties are to be found at the top, between system and application, and at the bottom, between circuit and device*.

To overcome those difficulties Wolfgang agreed with Prof. Dr. Diederik Verkest (IMEC, presentation in the NANO-TEC 2nd workshop), who proposed a new device property to be the solution, namely, "Systemability". Systemability was defined as "the ability to economically design and manufacture reliable systems from the interaction of devices fabricated in a given technology". He argued that the gap is due to the different approaches to systemability of the technology and design communities.

To be able to design for future applications using new technologies Wolfgang identified:

- Models and abstractions at all levels of the design process as a key issue
- The need for powerful new, physically aware, system-level design science and methodologies at the top of the design process to increase the productivity of designers, otherwise efficient use cannot be made of advanced devices and materials.
- The need for robust optimization methodologies in the middle of the design process, to provide guaranteed performance of integrated systems composed of devices, the characteristics of which are highly variable, operate in several different physical domains and have uncertain reliability.
- The need for a revamped, systematic, and greatly improved interface to manufacturing (Design for manufacturing) at the back end, as well as throughout the flow, to support the design of high-yield systems that obtain maximum utilization of a technology and to assure that products can be produced using new technologies.

Wolfgang agreed with Sandip, that *design challenges will be application-dependent*. As each application has its own specific requirements it is clear, that this leads to different design optimization criteria. While there are criteria like real-time, energy efficiency, productivity, reliability and robustness, safety and security are also mandatory, and all these are of different importance for different applications.
According to Wolfgang, *design tools will definitely be the discriminating factor for the success of one specific technology*, because of the difficulties mentioned before, which have to be overcome by design tools. Furthermore, Wolfgang stated that the need for a new technology, i.e., when CMOS reaches barriers, will trigger the need for appropriate new tools and methods. Hence, a design methodology and tools for a specific technology will pave its way to success.

In the beginning of his statement Paolo asked, if the presented structures and devices, which are definitely different from CMOS, can really be designed and how they can be pushed forward. He mentioned graphene in particular, where the main problem of contacting has not been really solved yet. Starting from that, Paolo stated that in many cases, the solution for an overwhelming problem is *to rethink a whole technology including the way things are approached*. In this manner, for example, a contact could not be a contact the way it is understood in CMOS and that therefore there is a strong need in new design tools and methods. According to Paolo, as design starts from the physics and the chemistry, the nanostructures need to be modeled to get an idea how they work. If you want to create an architecture based on those nanostructures and devices the need for modeling becomes increasingly essential. Paolo repeated the need to rethink things, and argued that this will be a *very creative process, which cannot be done by one person alone*. Finally, he emphasizes his view, that *none of the presented nanostructures will make it alone, they all will be a certain addition to CMOS to start with*.

Giovanni opened his statement stating that, being realistic, *CMOS will be "here to stay as a business"*, because CMOS is so large and so much efforts have been spent on it that it cannot be simply abandoned. However, Giovanni added that there certainly will be space for new things, if they are really at the leading edge regarding, e.g., *low power, high speed or reliability.* He suggested that an integrated combination of

sensing and computing could be of special interest. In short, according to Giovanni, the dimensions of nanostructures offer tremendous opportunities.
From the business point of view, Giovanni predicted a hybridization of technologies, meaning that some of the *new technologies will come together with CMOS, in order to improve specific aspects*. He mentioned examples like 3D and monolithic 3D integration and the mixing of processes. Nevertheless, although industry could take advantages of the new technologies, it will be a huge task to integrate them. According to Giovanni, it will be of particular interest to see the *combination of classical CMOS with some kind of memristor or graphene device* that would lead to a tightly integrated structure, offering a myriad of opportunities.
Giovanni also addressed tools, as they will be needed to build systems in future. But he made clear, that the EDA-Industry, a small 4 billion $ market, with no real new investments in new areas, is driven by three large companies, which will not push design tools for new technologies. To Giovanni, *the critical part is in the backend, where downscaling CMOS already causes enough challenges, while design for new technologies is even harder and needs to have something new*. In his opinion, this will be driven only by new companies, which will come with a new technology together with its design tools. Finally Giovanni send a message to the young generation: electronics is still an extremely vibrant field, interesting and fascinating, with lots of challenges and problems to be solved and that nobody should believe people saying it flattens out.

In the following discussion several topics were addressed. Dr Heike Riel (IBM Zurich) asked, if there will be a solution to design the *variability* into the whole system without loosing its small size. Sandip replied that this will most certainly happen, if design tools will be available to adopt gates accordingly. If systems have to be designed 100 % correctly, Giovanni added, variability has to be considered in the design especially at the physical level, because a system may be locally incorrect.

On a question from Mart Graef from TU Delft *how the design community could be involved in the discussion on new technology*, Giovanni answered that this would only happen because of the *need for a specific application*, which will involve the design community automatically. Wolfgang added that the NANO-TEC project is a good start, but specifically *simulation and modeling has to be implemented in order to make design people be able to do their exercises for building circuits*. In this context Paolo proposed the *universities to work on design for 'Beyond CMOS' technologies* while its educational aspects would create a new kind of young people.

Sandip expressed that companies will not do design for the new technologies on their own because they have to bring products to the market. Therefore, the only way will be *to bring all kinds of people together in order to make decisions how the things shall be done and then people would work on it.*

On another question from the audience *how young people can be attracted*, Paolo and Sandip agreed, that the fascination of technologies will do that, while Giovanni stated that the curiosity about applications will drive the young, because everybody likes to know what inside an iPhone is. According to Giovanni, the young could be attracted by telling them "you can change things".

In the end, the lively discussion showed that a *common sense in which an open mind and new kind of thinking are crucial in the path to be taken*.

3. Conclusions and recommendations

The variety of Beyond CMOS technologies needs to be clustered in terms of the state variable in question and the computation paradigm. A consensus was reached to classify them into:

(a) Technology and Design for devices with charge as state variable,
(b) Technology and Design for devices with non-charge as state variable and
(c) Technology and Design for new computing paradigms.

It is recommended that further discussion on Technology and Design address them in these clusters, in particular for the program of the 4th and final NANO-TEC workshop (November 2012), in order to make meaningful recommendations.

The complexity of the interaction between the communities in the Beyond CMOS field cannot be neglected. The project NANO-TEC has made a start but there is a huge amount of work to be done to reach practical levels that will make a difference in the sense that Europe can capitalize this advantage.

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Annex: Program of the 3rd NANO-TEC Workshop, 30-31 May 2012 in Lausanne, CH.

Wednesday 30 May 2012	
14.00-14.30	Welcome reception
14.30-15.30	**Solid-state Quantum Computing** *Goran Wendin, Chalmers University of Technology, Gothenburg* Discussant: Jouni Ahopelto, VTT Technical Research Centre of Finland, Espoo, Finland Rapporteur: Piotr Grabiec, Institute for Electron Technology, Warsaw, Poland
15.30-16.30	**Molecular Electronics** *Prof. Dr. Sense Jan van der Molen, Leiden University* *Discussant: Paolo Lugli, Technical University of Munich, Germany* *Rapporteur: Alain Cappy, Institute of Electronics, Microelectronics and Nanotechnology, Lille, France*
16.30-17.00	Coffee Break
17.00-18.00	**Nanowires** *Dr. Heike Riel, IBM Zurich* Discussant: Marc Heyns, Imec, Leuven, Belgium Rapporteur: Isabelle Ferain, Tyndall National Institute - University College Cork, Ireland
19.00	Workshop dinner & excursion
Thursday 31 May 2012	
08.30-09.30	**Spintronics** *Prof. Dr. Charles Gould, University of Wuerzburg* Discussant: Thomas Swahn, Chalmers University of Technology, Gothenburg, Sweden Rapporteur: Christian Pithan, Forschungszentrum Juelich, Germany
09.30-10.30	**Graphene** *Prof. Dr. Max Lemme, KTH Royal Institute of Technology, Stockholm* Discussant: Livio Baldi, Micron Technology Inc., Milan, Italy Rapporteur: Guilhem Larrieu, CNRS-LAAS, Toulouse
10.30-11.00	Coffee Break
11.00-12.00	**MEMS** *Dr. Michael Gaitan, NIST, Gaithensburg, MD, U.S.A.* Discussant: Lars Hedrich, University of Frankfurt, Germany Rapporteur: Androula Nassiopoulou, National Centre for Scientific Research 'Demokritos' - IMEL, Athens, Greece
12.00-13.30	Lunch
13.30-14.30	**Neuromorphic Computing** *Dr. Julie Grollier, CNRS-Thales, Palaiseau* Discussant: Dag Winkler, Chalmers Reporter: Clivia M Sotomayor Torres, Catalan Institute of Nanotechnology
14.30-15.30	Panel Discussion: "**Beyond CMOS: from technology to application**" *Chair: Dr. Livio Baldi, Micron Technology Inc., Milan;* *Panelists:* *Prof. Dr. Wolfgang Rosenstiel, edacentrum and University of Tübingen; Prof. Dr. Paolo Lugli, Technical University of Munich;* *Prof. Dr. Giovanni de Micheli, École Politechnique Fédérale de Lausanne; Prof. Dr. Sandip Tiwari, Cornell University, Ithaca, N.Y.*
15.30-16.00	Wrap-up, conclusion and recommendations for the final NANO-TEC workshop