NANOTEC ESSDERC/ESSCIRC Tutorial
on ECOSYSTEMS TECHNOLOGY and DESIGN
for NANOELECTRONICS:
an experience in Europe

Half Day Tutorial (13:30-16:30), Monday, September 17, 2012
"Palais des Congrès" Salle D2, Bordeaux Lac, allée Louis Ratabou, 33000 Bordeaux (F)

Tutorial Aim: This Tutorial will present the outcome of the EU project NANOTEC. The project NANOTEC (Ecosystems Technology and Design for Nanoelectronics) is a support action funded by the European Commission under number 257964. The aim of NANO-TEC is to address the gap between technology and design in Nanoelectronics in the area of Beyond CMOS. Within the scope of NANOTEC, a number of workshops have been organized, where specific 'Beyond CMOS' device concepts were presented and discussed by experts in the field. Some categories of beyond CMOS devices were selected, that were benchmarked and a SWOT analysis was carried out. To this end NANOTEC carries out a continued consultation and analysis of research needs and trends based on a workshop series with invited experts from the Americas, Asia and Europe covering topics such as Beyond CMOS device concepts and design, benchmarking and a SWOT analysis of new devices. Progress made so far towards the stated aims will be presented in this tutorial by the different speakers.

Organizers:

A.G. Nassiopoulou, NCSR Demokritos, Athens, Greece <A.Nassiopoulou@imel.demokritos.gr>
W. Grabinski, EPFL, Lausanne, Switzerland <wladyslaw.grabinski@epfl.ch>

Program Schedule	
13:30-13:45	Welcome and Introduction
13:45-14:00	FP7 Project NANOTEC On Ecosystems Technology & Design For Nanoelectronics: An Experience In Europe **Androula Nassiopoulou**, NCSR Demokritos/IMEL, Athens, Greece
14:00-14:30	Benchmarking of Beyond CMOS **Jouni Ahopelto**, VTT Technical Research Centre of Finland, Helsinki, Finland
14:30-15:00	A SWOT Analysis of 'Beyond CMOS' **Mart Graef**, DIMES, Delft Institute of Microsystems and Nanoelectronics, Delft University of Technology, The Netherlands
15:00-15:30	Case study: The case of nanowire transistor **Guilhem Larrieu**, LAAS-CNRS, Toulouse, France
15:30-16:00	Coffee Break
16:00-16:30	Information processing paradigms of the post CMOS era: devices and architectures. **Alain Cappy**, IEMN-UMR, Villeneuve D'Ascq, France

NANOTEC website: www.fp7-NANOTEC.eu
Prof. Dr. Clivia M. Sotomayor Torres
(Project Coordinator)
E-mail: clivia.sotomayor@icn.cat