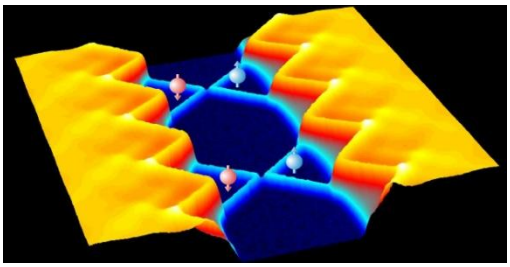
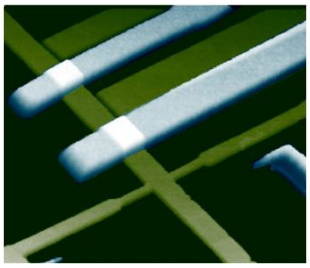
NANO-TEC

Workshop 2:

Benchmarking of new beyond CMOS device/design concepts

13-14 October 2011, Divani Caravel Hotel, Athens, Greece.

Welcome Booklet

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Laura Camarero, Catalan Institute of Nanotechnology, Barcelona

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SPEAKER'S BIOGRAPHIES

JOHAN ÅKERMAN, University of Gothenburg & NanoSC, Sweden

Johan Åkerman was born in Malmö and graduated with a degree of Ingénieur Physicien Diplômé from Ecole Polytechnique Federale de Lausanne in Switzerland, and later with a master's degree in Engineering Physics from the Faculty of Technology at Lund University. He received his PhD in 1998 from the Royal Institute of Technology in Stockholm. He was a postdoctoral research fellow at the University of California, San Diego from 1999 to 2001, and then employed to manage research in magnetic computer memories by Motorola in Phoenix. In 2005 he was nominated as research manager of the future by the Swedish Foundation for Strategic Research. He has been appointed to a special research post by the Royal Swedish Academy of Sciences and since 1 October 2008 has been professor of experimental physics at the Faculty of Science at the University of Gothenburg.

JULIE GROLLIER, Centre National de la Recherche Scientifique, Thales, Palaiseau, France

Julie Grollier, born in 1975, first graduated from the engineering institute Ecole Supérieure d'Electricité before obtaining a diploma from the Ecole Normale Superieure de Cachan. Her Ph.D., obtained in 2003 and supervised by Albert Fert, focused on "Spin transfer induced magnetization switching". This spintronic phenomena allows to manipulate the magnetization of nano-objects simply by current injection, without the help of an applied external magnetic field. As a post-doc, first in Groningen University (Netherlands, group of B.J. van Wees), then in the Institut d'Electronique Fondamentale (France, group of C. Chappert), she studied the magnetization dynamics of nano-magnets. In 2005, she received a permanent position as a researcher in the Joint Unit CNRS/Thales, where she is leading the Spin Transfer Nano-Oscillators team together with her colleague Vincent Cros.
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DANIEL HERR, Semiconductor Research Corporation, Palo Alto, CA, U.S.A.

Dr. Herr is Semiconductor Research Corporation's Director of Nanomanufacturing Science Research. He leads an international team that provides vision, guidance, and leveraged support for a number of the top collaborative interdisciplinary university research programs on emerging nanoelectronics related materials and assembly methods, environmentally benign high performance manufacturing, and enabling nano-characterization technology options. He also is exploring the potential of emerging research opportunities in bioelectronics, ultra low power systems, and energy harvesting. He held senior engineering positions at Honeywell

Corporation, during the VHSIC program, and Shipley Company, in Japan, where he helped bring up a new R&D facility. He also founded AR&D Corporation, a material design-consulting firm.

ADRIAN IONESCU, École Politechnique Fédérale de Lausanne, Switzerland-TO BE SUBSTITED BY WLADYSLAW GRABINSKI

Adrian M. Ionescu is an Associate Professor at the Swiss Federal Institute of Technology Lausanne (Ecole Polytechnique Fédérale de Lausanne – EPFL), Switzerland. He received the B.S./M.S. and Ph.D. degrees from the Polytechnic Institute of Bucharest, Romania and the National Polytechnic Institute of Grenoble, France, in 1989 and 1997, respectively. He held staff and/or visiting positions at LETI-Commissariat à l'Énergie Atomique, Grenoble, CNRS, Grenoble, and Stanford University, Stanford, CA, in 1998 and 1999. He is currently the Director of the Nanoelectronic Devices Laboratory and Director of the Doctoral School of Microsystems and Microelectronics of EPFL. He served on the International Electron Devices Meeting (IEDM) and European Solid-State Device Research Conference (ESSDERC) technical committees and was the Technical Program Committee Chair of the ESSDERC in 2006. He is a member of the Scientific Committee of the Cluster for Application and Technology Research in Europe on Nanoelectronics (CATRENE) and was appointed as the national representative of Switzerland to the European Nanoelectronics Initiative Advisory Council (ENIAC).

JARI KINARET, Chalmers University of Technology, Gothenburg, Sweden

Jari Kinaret was born in Kokkola, Finlan, in 1962. He studied at the University of Oulu in Finland and received his M.Sc. degree in Theoretical Physics in 1986, and a M.Sc. in Electrical Engineering in 1987. In 1987-1992 he studied at the Massachusetts Institute of Technology in the USA, and graduated with a Ph.D. in Physics in 1992. Upon graduation he worked at the Nordic Institute of Theoretical Physics (Nordita) in Copenhagen, first as a post-doctoral fellow and later as a Nordic Assistant Professor. In 1995 he moved to Sweden and took a position as Assistant Professor at the University of Gothenburg, in the condensed matter theory group at the Department of Applied Physics. Since 1998 he is employed by Chalmers, and currently heads the Division of Condensed Matter Theory. Professor Kinaret is also the coordinator of the Chalmers Nanotechnology Center established in 2009.

HEIKE RIEL, IBM, Zurich, Switzerland

H. Riel received her M.S. degree in Physics from the University of Erlangen-Nuremberg, Erlangen-Nuremberg, Germany, in 1998 and followinglt a Ph.D. degree in physics from the University of Bayreuth, Germany, in 2003.
After an internship with the Hewlett–Packard Research Laboratory, Palo Alto, CA, she joined the IBM Zurich Research Laboratory, Zurich, Switzerland, as a Student, pursuing her research on organic light-emitting devices. In 2003 she became a research staff member, and since 2008 she has lead the Nanoscale Electronics Group at the IBM Zurich Research Laboratory. Her main research interests include organic and inorganic semiconductors motivated by the quest for future electronic and optoelectronic devices. Her current research interests include the exploration of the fundamental properties of Si and III/V nanowires and their application for steep-slope devices.
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LINA SARRO, Technical University of Delft, The Netherlands

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JAW-SHEN TSAI, NEC & The Riken Institute for Physical and Chemical Research, Ibaraki, Japan

Jaw-Shen Tsai was born in 1952. He graduated from the department of Physics at the University of California at Berkeley in 1975 and received his Ph.D. in Physics from the State University of New York at Stony Brook in 1983. His research life has been devoted to the study of macroscopic quantum effect in superconductors, especially associated with Josephson junctions. He has contributed to the area of condensed matter physics in both fundamental physics and their technological potential. His most celebrated work is the demonstration of quantum coherent oscillations in a solid state system. He is a Fellow at NEC Nano Electronics Research Laboratories, where he leads the Josephson junction based qubit project. He is also the Laboratory Head of Macroscopic Quantum Coherence Research laboratory, Advanced Science Institute, RIKEN. He joined NEC R&D unit in 1983, and since 1996 he has been working on the experiments connected quantum coherence in the Josephson systems. In this direction, his group has been pioneering the science and technology of superconducting quantum computing. His group has demonstrated the first solid-state based qubit in 1999, and subsequently demonstrated the first solid state CNOT gate in 2003, a switchable coupling between qubits required for a quantum universal gate in 2007. He received Nishina Memorial Prize in 2004 and Simon Memorial Prize in 2008. He is a fellow of American Physical Society and is an Honorary Professor of National Chiao Tung University, Taiwan.

DOMINIQUE VUILLAUME, Centre National de la Recherche Scientifique, Thales, Palaiseau, France

Dominique Vuillaume was born in 1956. He received a degree in Electronics Engineering from the Institut Supérieur d'Electronique du Nord, Lille, France, 1981 and the PhD degree and Habilitation diploma in Solid-State Physics, from the University of Lille, France in 1984 and 1992, respectively. He is research director at CNRS (Centre National de la Recherche Scientifique) and he works at the Institute for Electronics, Microelectronics and Nanotechnology (IEMN), University of Lille. He created and leads the Molecular Nanostructures & Devices » research group at IEMN.
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- study of functional molecular devices and integrated molecular systems,
- exploration of new computing paradigms using molecules and nanostructures. He was scientific advisor for industrial companies (Bull R&D center) and is currently scientific advisor for the CEA "Chimtronique" research program.

PRESENTATION OF ABSTRACTS

SESSION 1- MOLECULAR ELECTRONICS

Dominique Vuillaume, Centre National de la Recherche Scientifique, Thales, Palaiseau, France

Prospects in self-assembled molecular electronics devices

Self-assembly of organic molecules on solid substrates is a powerful "bottom-up" approach for the fabrication of devices for molecular-scale electronics. More than a possible answer to ultimate miniaturization problem in nano-electronics, self-assembled molecular electronics is foreseen as a possible and reasonable way to assemble a large numbers of nanoscale objects (molecules, nanoparticules, nanotubes and nanowires) to form new devices and circuit architectures, beyond the von-Neumann paradigm. It is also an interesting approach to significantly reduce the fabrication costs, as well as the energetical costs of computation, compared to usual semiconductor technologies. Moreover, molecular electronics is a field with a large spectrum of investigations: from quantum objects, for testing new paradigms, to hybrid molecular-silicon CMOS devices. This presentation will briefly describe recent results about electron transport through molecules, ensemble of molecules, organic monolayers and molecular devices mandatory to understand the realistic electron transport in these molecular devices. Some progress on “molecular technologies” useful to make these organic nano-devices will be discussed, and specific problems encountered when working with molecules will be pinpointed. Moreover, recent results dedicated to the applications towards some information technology functions (e.g. molecular memories, switches, transistors, molecular spintronic, etc…) will be reviewed, and perspectives and challenges will be discussed.

SESSION 2- MEMS

Lina Sarro, Technical University of Delft, The Netherlands

There is a wide consensus on the relevance, applicability and need for MEMS in several applications areas, ranging from automotive to health, from industrial processes to consumer electronics. A significant amount of progress has been achieved over the past 20 years, but a number of issues still need to be addressed to move to a wider implementation of MEMS based devices and systems. The progress in silicon based MEMS has been relying heavily on the mainstream IC technology and benefitting from both technological findings as well as manufacturing equipment developments, for the definition and structuring of its components. However, the introduction of new functions, other than electrical, in (or on top of) a silicon chip, requires a different perspective/approach to design as well. The lack of a “basic cell”, a different concept of “mainstream” technology, and the requirement of interconnects to other physical domains makes it a very different case as compared to ICs. These are major challenges to be addressed in the coming years, especially considering the level of “standardization” that can be achieved without jeopardizing flexibility and diversity as demanded by specific application areas.

SESSION 3- SOLID-STATE QUANTUM COMPUTING

Jaw-Shen Tsai , NEC & The Riken Institute for Physical and Chemical Research, Ibaraki, Japan

In quest of superconducting quantum computer

We have been searching a path that leads to the realization of superconducting quantum computer. While decoherence time in Josephson qubit has been increasing steadily over the past decade, several scalable coupling schemes were also devised. The fabrication technology for multi-layer superconducting qubit large scale integrated circuit (LSI) is also being developed. Those issues will be discussed at the presentation.

SESSION 4-SPINTRONICS

Johan Åkerman, University of Gothenburg & Nano SC, Sweden

While spintronic devices are already in use in commercial products, e.g. in read-heads in hard disk drives and in magnetic tunnel junction (MTJ) based memory bits in Magnetic Random Access Memory (MRAM), there are a number of emerging spintronic devices and technologies on the horizon. Some of these, such as Spin Transfer Torque (STT) MRAM, are currently heavily investigated by both industry and academia, while others, such as Spin Torque Oscillators, Spin Torque Microwave Detectors, MTJ logic, Nanomagnet logic, All-spin logic, Spin Wave logic, Magnetic automata, and Race Track memory still require substantial development and optimization until they reach a similar level of maturity. In my talk I will try to shed light on the potential of these spintronic technologies for future use in ICT applications, with particular focus on challenges such as power consumption, speed, integration, manufacturability, and reliability.

SESSION 5-NANOWIRES

Heike Riel, IBM, Zurich, Switzerland

Semiconductor Nanowires for Future Field-Effect Transistors

The scaling of semiconductor technology (CMOS) has been the driving force for the success of information technology. However, as device dimensions continue to shrink into the nanometer length-scale regime, conventional semiconductor technology is approaching fundamental physical limits. New strategies, including the use of novel materials and 1D-device concepts, innovative device architectures, and smart integration schemes need to be explored and assessed. They are crucial to extend the current capabilities and maintain momentum beyond the time frame of the silicon technology roadmap. The increasing power dissipation on the chip level is one of the key challenges today. Rising leakage currents and the increasing difficulty to further reduce the supply voltage have impacted the passive and active power dissipation, limiting the overall performance. Therefore a key attribute of any new device that may be considered for replacing the conventional FET is a reduced power dissipation. In the power performance trade-off, the supply voltage is the largest lever to tweak because the power is almost proportional to the cube of the supply voltage. In that respect, semiconductor nanowires have attracted considerable attention. They are regarded as one of the most promising candidates for future logic devices, owing to their cylindrical geometry and the possibility to integrate III-V materials on a silicon platform. These characteristics are
especially important for tunnel field-effect transistors (TFETs). TFETs are so called steep-slope devices that can achieve a subthreshold swing of less than 60 mV/dec and are thus attractive for low-voltage operation to reduce power dissipation in electronic circuits. The first part of this presentation presents the possible benefits and the current challenges of grown and etched silicon nanowires for conventional MOSFET applications. In the second part, the focus is on steep-slope devices. Physical approaches to achieve this attribute will be briefly outlined and assessed. In particular, the TFET, currently the most prominent candidate for becoming the next nanoelectronic switch, is evaluated in more detail.

SESSION 6-MEMRISTORS-Artificial Synapses

Jullie Grollier, Unité Mixte de Physique, Centre National de la Recherche Scientifique, Thales, Palaiseau, France

The announcement by Hewlett-Packard in 2008 that they had fabricated a new type of component, the "memristor", created a lot of buzz [1,2]. Indeed, these electronic nano-devices have a number of extremely promising applications, such as digital memories, switches and latches for advanced logic functions etc. One of the most fascinating properties of memristors is that they intrinsically behave like synapses, which could be a key to the future development of hardware Artificial Neural Networks (ANNs), and revolutionize non-conventional neuromorphic computing. Research on memristors immediately became a hot topic in the US, with the DARPA "SyNAPSE" program hugely funding several teams to develop such components and integrate them in ANNs. Several related projects are now starting in Europe and France. A memristor is a tiny non-volatile analog tuneable resistance. The more intense is the current through the structure, and the longer it is injected, the more the resistance changes. This property directly implements the fact that the synapse transmission depends on the information it has formerly processed (plasticity). The HP discovery has motivated several research and industrial groups to develop their own memristors. Most of these devices belong to the class of memories called Resistive Random Access Memories (RAMs), and are based on very different physical effects. This talk will be a review of the state of the art of memristor devices and their applications, with a special focus on their implementation as artificial synapses for on-chip neural networks.

[1] Strukov, D. B., *et al*., "The missing memristor found", *Nature*, 453, pp. 80-83, 2008.

[2] Yang, J.J., *et al*., "Memristive switching mechanism for metal/oxide/metal nanodevices", *Nature Nanotechnology*, 3, pp. 429-433, 2008.

SESSION 7- GRAPHENE

Jari Kinaret, Chalmers University of Technology, Gothenburg, Sweden

Graphene research has grown exponentially since the groundbreakning discoveries by Andre Geim and Konstantin Novoselov in 2004 that were recognized with the Nobel Prize in Physics in 2010. Soon after the seminal work by Geim and Novoselov, graphene's potential for electronic applications was realized. In this talk I will review the progress on graphene electronics in the seven years after the first graphene transistor, and address some of the key possibilities offered by graphene but also some of the remaining challenges.

PANEL DISCUSSION ON DESIGN

Diederik Verkest, Interuniversity Microelectronics Center, Leuven, Belgium

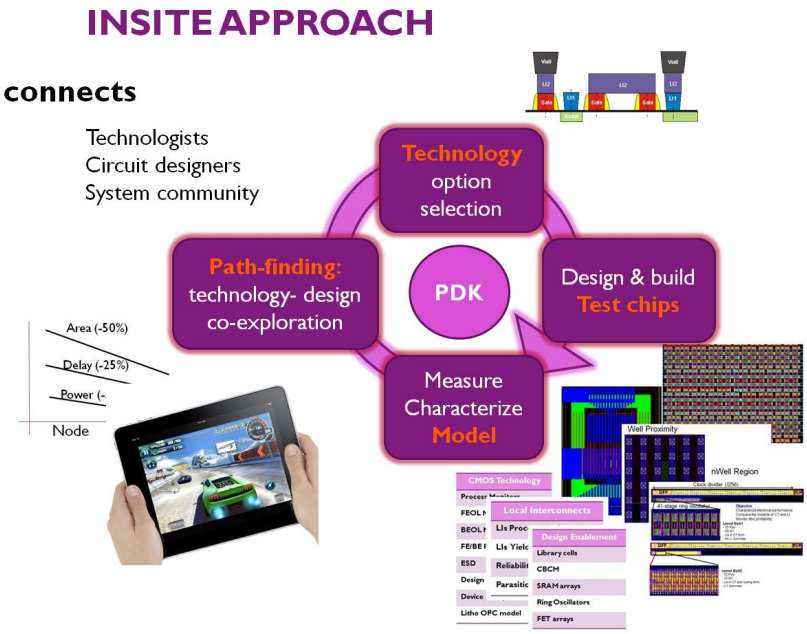
Enabling assessment of advanced process technology for future products.

D. Verkest

Both system design and process technology grow increasingly complex. Designing with advanced technology becomes ever more difficult and this adds risks and delays the introduction of new technology into products. As part of imec's research program on advanced process technologies, the INSITE program aims specifically at bridging the gap between technology and design.

The INSITE program makes information from imec's advanced process technology research programs available in formats that can be used by product designers for early assessment of the impact and potential of those technologies for product roadmaps. Additionally, it helps in setting targets for technology, starting from system specifications.

The key is the use of so-called "path-finding" PDKs, which capture the key elements of a new technology in a format that is compatible with current design flows. This allows the creation of virtual designs, which allow assessing area, power, performance, and cost of a new technology option. The models that are embedded in the path-finding framework are calibrated on test-chips processed in imec's clean rooms.



The program covers N+2 technologies in the logic, memory, stacking, and optical interconnect domains.

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HEIKE RIEL, IBM, Zurich, Switzerland

Heike Riel received her M.S. degree in Physics from the University of Erlangen-Nuremberg, Erlangen-Nuremberg, Germany, in 1998 and followingly a Ph.D. degree in Physics from the University of Bayreuth, Germany, in 2003.

After an internship with the Hewlett–Packard Research Laboratory, Palo Alto, CA, she joined the IBM Zurich Research Laboratory, Zurich, Switzerland, as a Student, pursuing her research on organic light-emitting devices. In 2003 she became a research staff member, and since 2008 she has lead the Nanoscale Electronics Group at the IBM Zurich Research Laboratory. Her main research interests include organic and inorganic semiconductors motivated by the quest for future electronic and optoelectronic devices. Her current research interests include the exploration of the fundamental properties of Si and III/V nanowires and their application for steep-slope devices.

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ADRIAN IONESCU, École Politechnique Fédérale de Lausanne, Switzerland

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Jari Kinaret was born in Kokkola in Finland in 1962. He studied at the University of Oulu in Finland and received his M.Sc. degree in Theoretical Physics in 1986, and a M.Sc. in Electrical Engineering in 1987. In 1987-1992 he studied at the Massachusetts Institute of Technology in the USA, and graduated with a Ph.D. in Physics in 1992. Upon graduation he worked at the Nordic Institute of Theoretical Physics (Nordita) in Copenhagen, first as a post-doctoral fellow and later as a Nordic Assistant Professor. In 1995 he moved to Sweden and took a position as Assistant Professor at the University of Gothenburg, in the condensed matter theory group at the Department of Applied Physics. Since 1998 he is employed by Chalmers, and currently heads the Division of Condensed Matter Theory. Professor Kinaret is also the coordinator of the Chalmers Nanotechnology Center established in 2009.

DANIEL HERR, Semiconductor Research Corporation, Palo Alto, CA, U.S.A.

Dr. Herr is Semiconductor Research Corporation's Director of Nanomanufacturing Science Research. He leads an international team that provides vision, guidance, and leveraged support for a number of the top collaborative interdisciplinary university research programs on emerging nanoelectronics related materials and assembly methods, environmentally benign high performance manufacturing, and enabling nano-characterization technology options. He also is exploring the potential of emerging research opportunities in bioelectronics, ultra low power systems, and energy harvesting. He held senior engineering positions at Honeywell Corporation, during the VHSIC program, and Shipley Company, in Japan, where he helped bring up a new R&D facility. He also founded AR&D Corporation, a material design-consulting firm.

PRESENTATION OF ABSTRACTS

SESSION 1- MOLECULAR ELECTRONICS

Dominique Vuillaume, Centre National de la Recherche Scientifique, Thales, Palaiseau, France

Prospects in self-assembled molecular electronics devices

Self-assembly of organic molecules on solid substrates is a powerful "bottom-up" approach for the fabrication of devices for molecular-scale electronics. More than a possible answer to ultimate miniaturization problem in nano-electronics, self-assembled molecular electronics is foreseen as a possible and reasonable way to assemble a large numbers of nanoscale objects (molecules, nanoparticules, nanotubes and nanowires) to form new devices and circuit architectures, beyond the von-Neumann paradigm. It is also an interesting approach to significantly reduce the fabrication costs, as well as the energetical costs of computation, compared to usual semiconductor technologies. Moreover, molecular electronics is a field with a large spectrum of investigations: from quantum objects, for testing new paradigms, to hybrid molecular-silicon CMOS devices. This presentation will briefly describe recent results about electron transport through molecules, ensemble of molecules, organic monolayers and molecular devices mandatory to understand the realistic electron transport in these molecular devices. Some progress on “molecular technologies” useful to make these organic nano-devices will be discussed, and specific problems encountered when working with molecules will be pinpointed. Moreover, recent results dedicated to the applications towards some information technology functions (e.g. molecular memories, switches, transistors, molecular spintronic, etc…) will be reviewed, and perspectives and challenges will be discussed.

SESSION 2- MEMS

Lina Sarro, Technical University of Delft, The Netherlands

There is a wide consensus on the relevance, applicability and need for MEMS in several applications areas, ranging from automotive to health, from industrial processes to consumer electronics. A significant amount of progress has been achieved over the past 20 years, but a number of issues still need to be addressed to move to a wider implementation of MEMS based devices and systems. The progress in silicon based MEMS has been relying heavily on the mainstream IC technology and benefitting from both technological findings as well as manufacturing equipment developments, for the definition and structuring of its components. However, the introduction of new functions, other than electrical, in (or on top of) a silicon chip, requires a different perspective/approach to design as well. The lack of a “basic cell”, a different concept of “mainstream” technology, and the requirement of interconnects to other physical domains makes it a very different case as compared to ICs. These are major challenges to be addressed in the coming years, especially considering the level of “standardization” that can be achieved without jeopardizing flexibility and diversity as demanded by specific application areas.

SESSION 3- SOLID-STATE QUANTUM COMPUTING

Jaw-Shen Tsai , NEC & The Riken Institute for Physical and Chemical Research, Ibaraki, Japan

In quest of superconducting quantum computer

We have been searching a path that leads to the realization of superconducting quantum computer. While decoherence time in Josephson qubit has been increasing steadily over the past decade, several scalable coupling schemes were also devised. The fabrication technology for multi-layer superconducting qubit large scale integrated circuit (LSI) is also being developed. Those issues will be discussed at the presentation.

SESSION 4-SPINTRONICS

Johan Åkerman, University of Gothenburg & Nano SC, Sweden

While spintronic devices are already in use in commercial products, e.g. in read-heads in hard disk drives and in magnetic tunnel junction (MTJ) based memory bits in Magnetic Random Access Memory (MRAM), there are a number of emerging spintronic devices and technologies on the horizon. Some of these, such as Spin Transfer Torque (STT) MRAM, are currently heavily investigated by both industry and academia, while others, such as Spin Torque Oscillators, Spin Torque Microwave Detectors, MTJ logic, Nanomagnet logic, All-spin logic, Spin Wave logic, Magnetic automata, and Race Track memory still require substantial development and optimization until they reach a similar level of maturity. In my talk I will try to shed light on the potential of these spintronic technologies for future use in ICT applications, with particular focus on challenges such as power consumption, speed, integration, manufacturability, and reliability.

SESSION 5-NANOWIRES

Heike Riel, IBM, Zurich, Switzerland

Semiconductor Nanowires for Future Field-Effect Transistors

The scaling of semiconductor technology (CMOS) has been the driving force for the success of information technology. However, as device dimensions continue to shrink into the nanometer length-scale regime, conventional semiconductor technology is approaching fundamental physical limits. New strategies, including the use of novel materials and 1D-device concepts, innovative device architectures, and smart integration schemes need to be explored and assessed. They are crucial to extend the current capabilities and maintain momentum beyond the time frame of the silicon technology roadmap. The increasing power dissipation on the chip level is one of the key challenges today. Rising leakage currents and the increasing difficulty to further reduce the supply voltage have impacted the passive and active power dissipation, limiting the overall performance. Therefore a key attribute of any new device that may be considered for replacing the conventional FET is a reduced power dissipation. In the power performance trade-off, the supply voltage is the largest lever to tweak because the power is almost proportional to the cube of the supply voltage. In that respect, semiconductor nanowires have attracted considerable attention. They are regarded as one of the most promising candidates for future logic devices, owing to their cylindrical geometry and the possibility to integrate III-V materials on a silicon platform. These characteristics are
especially important for tunnel field-effect transistors (TFETs). TFETs are so called steep-slope devices that can achieve a subthreshold swing of less than 60 mV/dec and are thus attractive for low-voltage operation to reduce power dissipation in electronic circuits. The first part of

this presentation presents the possible benefits and the current challenges of grown and etched silicon nanowires for conventional MOSFET applications. In the second part, the focus is on steep-slope devices. Physical approaches to achieve this attribute will be briefly outlined and assessed. In particular, the TFET, currently the most prominent candidate for becoming the next nanoelectronic switch, is evaluated in more detail.

SESSION 6-MEMRISTORS-Artificial Synapses

Jullie Grollier, Julie Grollier, Unité Mixte de Physique, Centre National de la Recherche Scientifique, Thales, Palaiseau, France

The announcement by Hewlett-Packard in 2008 that they had fabricated a new type of component, the "memristor", created a lot of buzz [1,2]. Indeed, these electronic nano-devices have a number of extremely promising applications, such as digital memories, switches and latches for advanced logic functions etc. One of the most fascinating properties of memristors is that they intrinsically behave like synapses, which could be a key to the future development of hardware Artificial Neural Networks (ANNs), and revolutionize non-conventional neuromorphic computing. Research on memristors immediately became a hot topic in the US, with the DARPA "SyNAPSE" program hugely funding several teams to develop such components and integrate them in ANNs. Several related projects are now starting in Europe and France. A memristor is a tiny non-volatile analog tuneable resistance. The more intense is the current through the structure, and the longer it is injected, the more the resistance changes. This property directly implements the fact that the synapse transmission depends on the information it has formerly processed (plasticity). The HP discovery has motivated several research and industrial groups to develop their own memristors. Most of these devices belong to the class of memories called Resistive Random Access Memories (RAMs), and are based on very different physical effects. This talk will be a review of the state of the art of memristor devices and their applications, with a special focus on their implementation as artificial synapses for on-chip neural networks.

[1] Strukov, D. B., et al., "The missing memristor found", Nature, 453, pp. 80-83, 2008.

[2] Yang, J.J., et al., "Memristive switching mechanism for metal/oxide/metal nanodevices", Nature Nanotechnology, 3, pp. 429-433, 2008.

SESSION 7- GRAPHENE

Jari Kinaret, Chalmers University of Technology , Gothenburg, Sweden

Graphene research has grown exponentially since the groundbreakning discoveries by Andre Geim and Konstantin Novoselov in 2004 that were recognized with the Nobel Prize in Physics in 2010. Soon after the seminal work by Geim and Novoselov, graphene's potential for electronic applications was realized. In this talk I will review the progress on graphene electronics in the seven years after the first graphene transistor, and address some of the key possibilities offered by graphene but also some of the remaining challenges.

PANEL DISCUSSION ON DESIGN

Diederik Verkest, Interuniversity Microelectronics Center, Leuven, Belgium

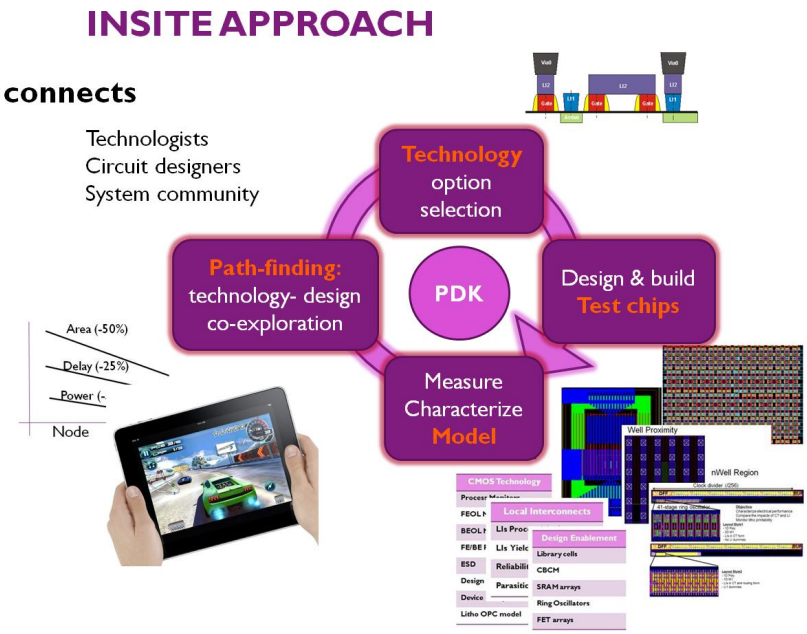
Enabling assessment of advanced process technology for future products

Both system design and process technology grow increasingly complex. Designing with advanced technology becomes ever more difficult and this adds risks and delays the

introduction of new technology into products. As part of imec's research program on advanced process technologies, the INSITE program aims specifically at bridging the gap between technology and design.

The INSITE program makes information from imec's advanced process technology research programs available in formats that can be used by product designers for early assessment of the impact and potential of those technologies for product roadmaps. Additionally, it helps in setting targets for technology, starting from system specifications.

The key is the use of so-called "path-finding" PDKs, which capture the key elements of a new technology in a format that is compatible with current design flows. This allows the creation of virtual designs, which allow assessing area, power, performance, and cost of a new technology option. The models that are embedded in the path-finding framework are calibrated on test-chips processed in imec's clean rooms.



The program covers N+2 technologies in the logic, memory, stacking, and optical interconnect domains.

Workshop 2, Benchmarking of new Beyond CMOS device/design concepts

13-14 October 2011
Hotel Divani Caravel,
Vassileos Alexandrou Av. 2, Athens, Greece

Program

Wednesday 12 October 2011

20.30 **Welcome reception and workshop introduction**
Clivia M Sotomayor Torres - Catalan Institute of Nanotechnology, Barcelona, Spain, Coordinator of NANOTEC, and Androula Nassiopoulou - National Centre for Scientific Research "Demokritos", Athens, Greece

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Thursday 13 October 2011

08.30-09.00 **Registration**

09.00-09.05 **Introduction to day 1**
Jouni Ahopelto - VTT Technical Research Centre of Finland, and Mart Graef - Technical University of Delft, The Netherlands

09.05-10.05 **Session 1 – Molecular Electronics**
Speaker: Dominique Vuillaume - CNRS, Lille, France (35 minutes)
Discussant: Clivia M Sotomayor Torres - Catalan Institute of Nanotechnology, Barcelona, Spain (5 minutes)
Rapporteur: Jouni Ahopelto - VTT Technical Research Centre of Finland
Group discussion (20 minutes)

10.05-11.05 **Session 2 – Mems**
Speaker: Lina Sarro - Technical University of Delft, The Netherlands (35 minutes)
Discussant: Piotr Grabiec - Institute of Electron Technology, Warsaw, Poland (5 minutes)
Rapporteur: tba
Group discussion (20 minutes)

11.05-11.30 **Coffee Break**

11.30-12.30 **Session 3 – Solid-State Quantum Computing**
Speaker: Jaw-Shen Tsai - NEC &The Riken Institute for Physical and Chemical Research, Ibaraki, Japan (35 minutes)
Discussant: Wolfgang Porod - University of Notre Dame, IN, U.S.A. (5 minutes)
Rapporteur: Isabelle Ferain - Tyndall National Institute-University College Cork, Ireland
Group discussion (20 minutes)

12.30-13.30 **Session 4 – Spintronics**
Speaker: Johan Åkerman - University of Gothenburg & NanoSC, Sweden (35 minutes)
Discussant: Christian Pithan - Forschungszentrum Juelich GmbH, Germany (5 minutes)
Rapporteur: Mart Graef - Technical University of Delft, The Netherlands
Group discussion (20 minutes)

13.30-15.00 **Lunch and networking**

15.00-16.00 **Session 5 – Nanowires**
Speaker: Heike Riel - IBM, Zurich, Switzerland (35 minutes)
Discussant: Isabelle Ferain- Tyndall National Institute at University College Cork, Ireland (5 minutes)

Rapporteur: Androula Nassiopoulou - National Centre for Scientific Research "Demokritos", Athens, Greece
Group discussion (20 minutes)

16.00-17.00 **Session 6 – Memristors**
Speaker: Julie Grollier - Centre National de la Recherche Cientifique-Thales, Palaiseau, France (35 minutes)
Discussant: Dag Winkler - Chalmers University of Technology, Gothenburg, Sweden (5 minutes)
Rapporteur: Adrian Ionescu, École Politechnique Fédérale de Lausanne, Switzerland
Group discussion (20 minutes)

17.00-17.30 **Coffee Break**

17.30-17.40 **"Guardian Angels" - a short introduction to the Flagship pilot coordination action**
Speaker: Adrian Ionescu, École Politechnique Fédérale de Lausanne, Switzerland

17.40-17.50 **"Graphene-CA" - a short introduction to the Flagship pilot coordination action**
Speaker: Jari Kinaret - Chalmers University of Technology, Gothenburg, Sweden

17.50-18.50 **Session 7 – Graphene**
Speaker: Jari Kinaret - Chalmers University of Technology, Gothenburg, Sweden (35 minutes)
Discussant: Dimitris Pavlidis- Centre National de la Recherche Scientifique-IEMN- Université de Lille, France (5 minutes)
Rapporteur: Lars Hedrich - Johann Wolfgang Goethe-Universität, Frankfurt, Germany
Group discussion (20 minutes)

18.50-19.25 **Wrap-up and conclusion of the day. All rapporteurs (5 minutes each)**

20.30 **Workshop Dinner at restaurant "Strofi",** Address : Rovertou Galli 25 P.C. : 117 42, Athens
Phone : 210- 9214130 (see map and indications on how to get there)

Friday 14 October 2011

09.00-10.30 **Panel Discussion on Design**
Chair person: Dan Herr - Semiconductor research Corporation, Palo Alto, CA, U.S.A
Panelists: Diederik Verkest, Interuniversity Microelectronics Center – Leuven, Belgium; Paolo Lugli – Technical University of Munich, Germany; Sandip Tiwari - University of Cornell, NY, U.S.A; Lars Hedrich – Johann Wolfgang Goethe-Universität, Frankfurt, Germany

10.30-11.30 **Parallel working groups on Molecular Electronics, Mems, and Solid State Quantum Computing**
Three separate rooms, maximum 15 participants per session, chair persons: Dominique Vuillaume - CNRS, Lille, France; Lina Sarro - Technical University of Delft, The Netherlands; Jaw-Shen Tsai - NEC &The Riken Institute for Physical and Chemical Research, Ibaraki, Japan

11.30-11.50 **Coffee Break**

11.50-12.50 **Parallel working groups on Spintronics and Nanowires**
Two separate rooms, maximum 15 participants per session, chair persons**:** Johan Åkerman - University of Gothenburg & NanoSC, Sweden; Heike Riel - IBM, Zurich, Switzerland

12.50-13.50 **Parallel discussion on Memristors and graphene**
Two separate rooms, maximum 15 participants per session, chair persons: Julie Grollier - Centre National de la Recherche Cientifique-Thales, Palaiseau, France; Jari Kinaret - Chalmers University of Technology, Gothenburg, Sweden

13.50-14.25 **Conclusions of working groups by rapporteurs (about 3 minutes each)**

14.25-14.40 **Closing remarks of workshop 2, Next steps and announcement of Workshop 3**
Jouni Ahopelto - VTT Technical Research Centre of Finland, and Mart Graef - Technical University of Delft

14.40 **Lunch**

15.40 **Excursion to Cape Sounion archeological site, departure from Divani Caravel Hotel at 15.30, return to the same location around 20.00**

PRACTICAL INFORMATION

How to reach the Divani Caravel from the hotel

THE DISTANCE FROM THE AIRPORT TO THE DIVANI CARAVEL HOTEL IS 35 KM

- ✓ BY BUS. Bus no. X95 leaves approximately every 20 minutes, its cost is 5€ and the duration of the journey is about 1 hour. The name of the stop where you must get off is the 'Evangelismos stop", located next to the Hilton Hotel, and at 5 minutes walking distance from the Divani Caravel Hotel.

- ✓ BY TAXI. It has a fixed cost of 35 Euros from 06.00 – 22.00 and 50 Euros from 22.00 – 06.00; the duration of the journey is about 30 minutes.

- ✓ BY METRO. Underground runs every 30 minutes, from 05.54 a.m. to 23.30p.m. The duration of the journey is 40 minutes and it costs 8€. The nearest station to the hotel is Evangelismos Station, at 5-7 minutes walking distance from the hotel.

See further details on detailed maps and indications in the next pages

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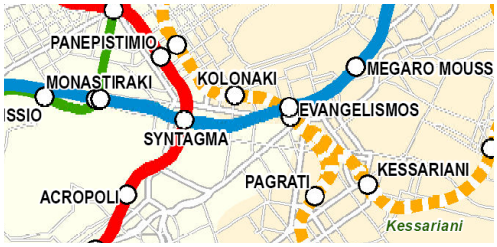
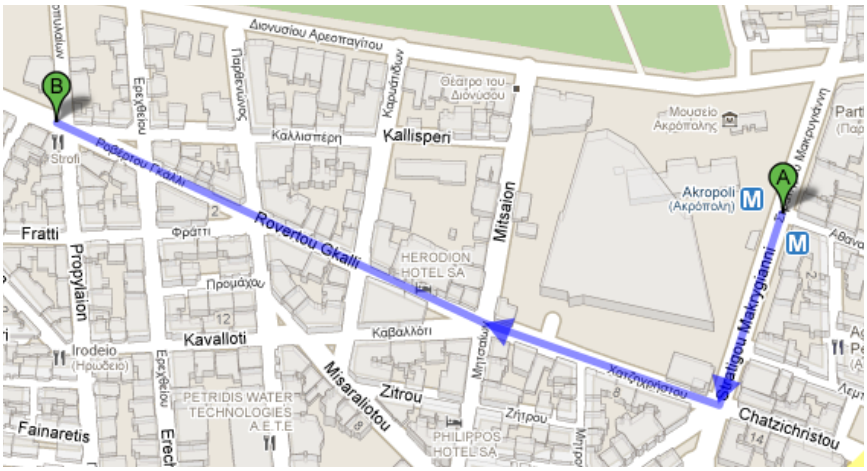
How to reach the Restaurant "Strofi" from the Divani Caravel Hotel

Divani Caravel Hotel (A) is near the metro station "Evangelismos" (B – 400m).

Take the blue line towards Aigaleo and get off at "Evangelismos" station. Then take the red line towards Aghios Dimitrios and get off at "Acropolis" station.





The restaurant "Strofi" (B) is near the metro station "Acropoli" (A - 550m). Head south on Stratigou Makrygianni, turn right onto Chatzichristou and continue onto Rovertou Gkalli.

Restaurant STROFI
Address : Rovertou Galli 25, 117 42, Athens
Phone : 210 9214130

HOW TO GET TO YOUR HOTEL
DIVANI CARAVEL

2, Vas. Alexandrou Avenue,
16121 Athens – Greece
T: +30 210 7207000
F: +30 210 7253750
E: sales@divanicaravel.gr
W: www.divanis.com/caravel

General:
The hotel has a bus shuttle service to/from Syntagma Square (Constitution Square) to hotel and vice versa. Please consult with our reception Desk for the detailed schedule.

FROM ATHENS INTERNATIONAL AIRPORT

By Taxi
There is a Taxi Station right outside the arrivals at airport. Ask the driver to get you to CARAVEL hotel. An average journey time on normal traffic is approx. 20-30 minutes drive.

By Metro
You take the blue line from the Airport. Get off the train at **EVANGELISMOS** Station. While in the station, take the left exit towards VAS. SOFIAS street. Walk pass the Hilton hotel (on your left hand side), cross Michalakopoulou Street, continue straight on Vas. Alexandrou Street. You will see **DIVANI CARAVEL** hotel on your right. If you do not want to walk (approximately 5-7 minutes walk), you may take the 224 bus (the stop is across the metro station exit), and get off at "CARAVEL Bus Stop", right in front of the hotel.

By car (driving directions)
- Exit the airport taking **Attiki Odos** highway following the signs **Ymittos Ring**.
- Take the exit toward **Dimitriou Karamolegkou**
- Keep right at the fork, follow signs for **Athina**
- Turn right at **Dimitriou Karamolegkou**
- Continue onto **Leoforos Ethnikis Antistaseos** & turn left at **Ymittou**
- Turn right to stay on **Ymittou**
- Turn right at **Eftychidou**
- Take the 3rd right onto **Spyrou Merkouri**
- Turn right at **Leoforos Vasileos Alexandrou**
- Take the 1st right onto **Niriidon**
- Take the 1st left onto **Leoforos Vasileos Alexandrou**
- Destination will be on the right - Divani Caravel -Vasileos Alexandrou 2, Kesariani

FROM LARISSIS TRAIN STATION

By Taxi

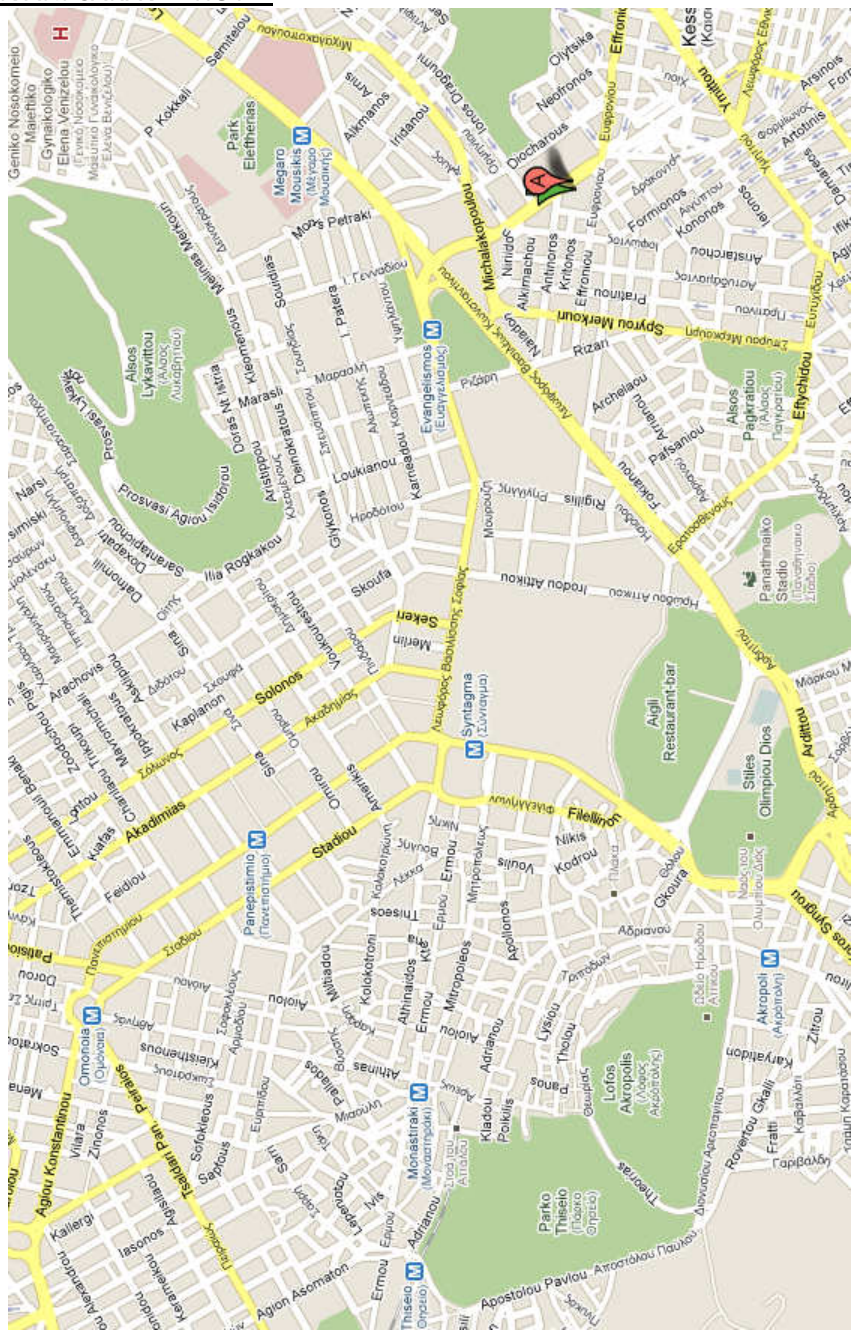
There is a Taxi station right outside the Train Station. Ask the driver to get you to CARAVEL hotel. An average time on normal traffic is approx. 20 minutes drive.

By Metro

There is a Metro station at Larissis Station. You take the **RED** line with direction to AGIOS DIMITRIOS. Change line at SYNTAGMA station and take the **BLUE** line with direction to Airport. Get off the train at **EVANGELISMOS** Station. While in the station, take the left exit towards VAS. SOFIAS street. Walk pass the Hilton hotel (on your left hand side), cross Michalakopoulou Street, continue straight on Vas. Alexandrou Street. You will see **DIVANI CARAVEL** hotel on your right.

If you do not want to walk (approximately 5-7 minutes walk), you may take the 224 bus (the stop is across the metro station exit), and get oof at “CARAVEL Bus Stop”, right in front of the hotel.

A: DIVANI CARAVEL HOTEL



Molecular electronics

D. Vuillaume

Molecular Nanostructures & Devices group

http://ncm.iemn.univ-lille1.fr

Institute for Electronics Microelectronics and Nanotechnology (IEMN)

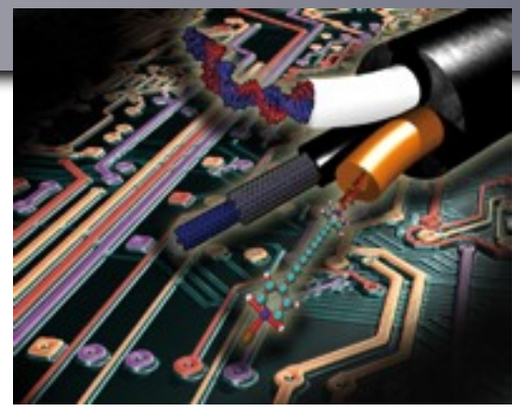
CNRS & University of Lille

France

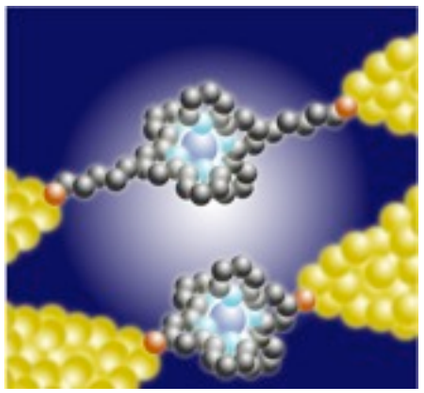
Outline

- What is molecular electronic?
- Nanodielectrics
- Monolayer transistors
- Monolayer memories and switches
- Molecular spintronics
- Molecular approaches for non conventional computing

What is molecular electronics?



single molecule electronics

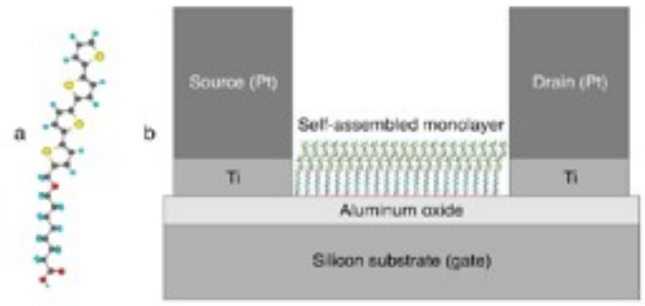


L < a few nm
t < a few nm

basic science
knowledge development

no foreseen applications
in a reasonable time-scale

self-assembled molecular electronics



L ~ hundred nm - µm
t < a few nm

basic science
knowledge development

possible applications
foreseen

thin-film molecular electronics

L > µm
t > few 10 nm

plastic electronics
(OLED, OFET, OPV)

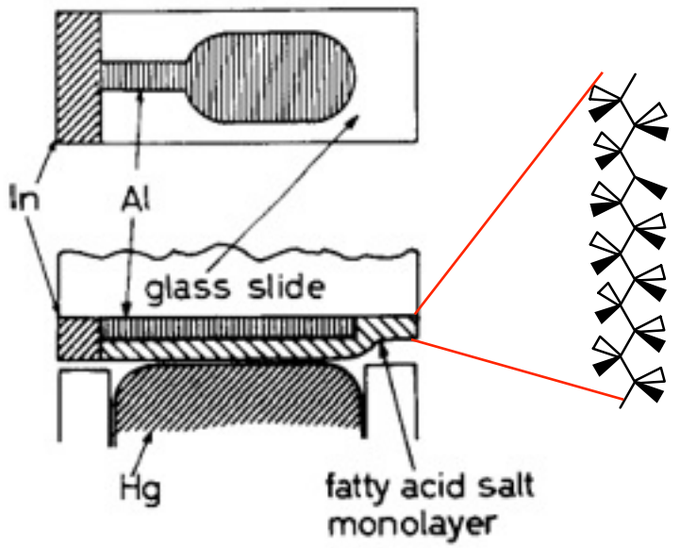
some products already
commercialized

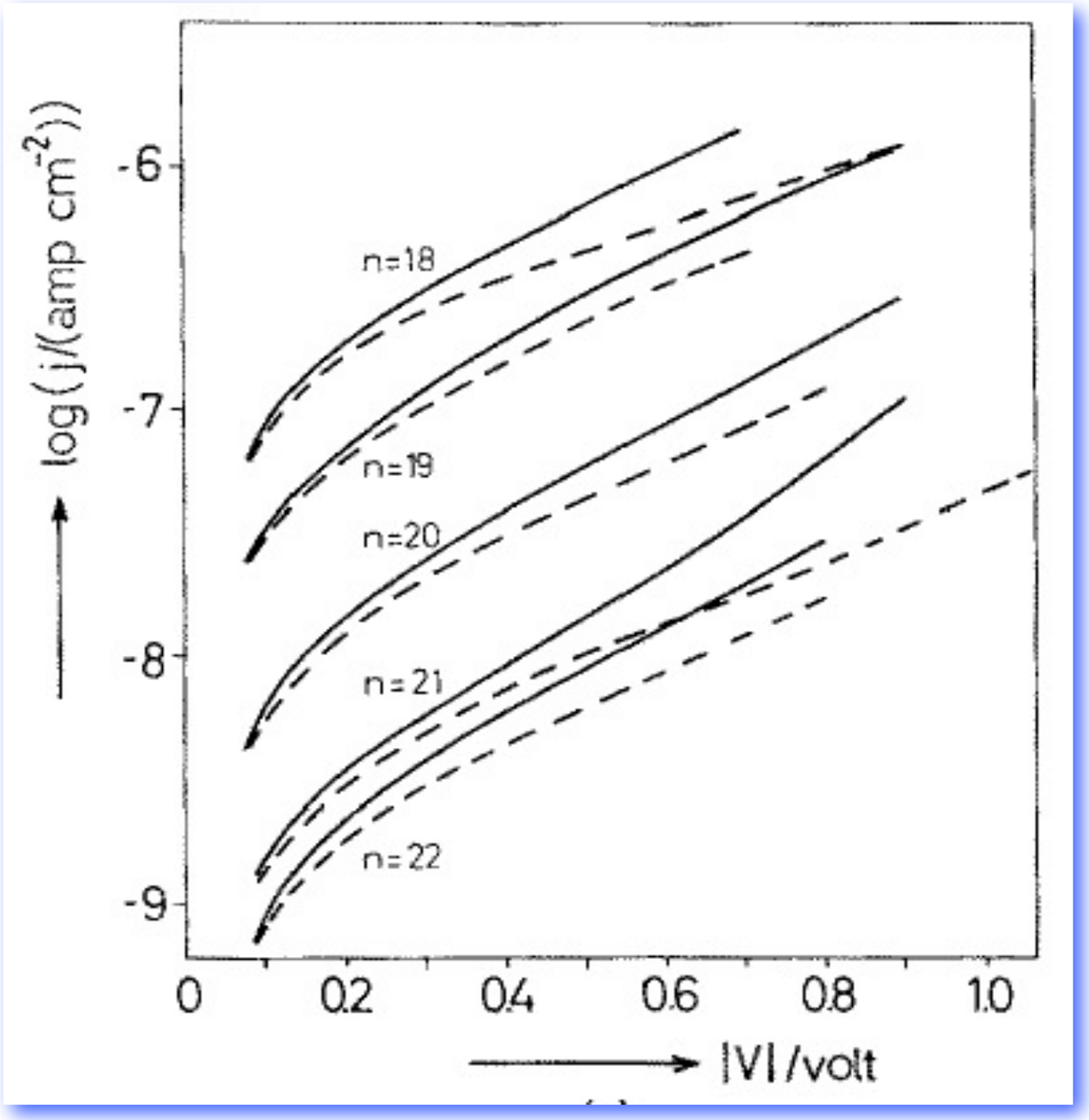
The first organic nanodielectrics

Not a recent story

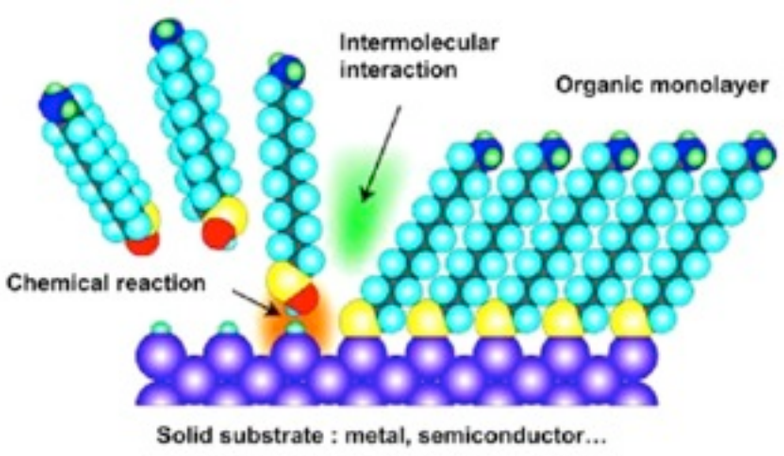
Mann & Kuhn, J. Appl. Phys. (1971)

1rst evidence of tunneling through a fatty acid LB monolayer sandwiched between metal electrodes





organic monolayer tunnel barrier



Métaux

Au	R–SH, R–SS–R, R–S–R, R–NH_2, R–CN, R–S–$COCH_3$, R–SeH, R–TeH, R–PO_3^{2-}, R–PO_4^{2-}, R–$S_2O_3^{2-}$
Ag	R–SH, R–SS–R, R–CO_2H, R–CN, R–SeH
Pt	R–SH, R–NC
Pd	R–SH, R–SS–R, R-N_2^+
Cu	R–SH, R–$S_2O_3^{2-}$
Hg	R–SH
Zn	R–SH

Semiconducteurs

Si ou Si-H	R–CH=CH_2, R–C≡CH, R–OH, R-N_2^+
Ge	R–SH
GaAs	R–SH, R-N_2^+, R–PO_3^{2-}
InP	R–SH
CdSe	R–SH
CdS	R–SH, R–SeH
ZnSe	R–SH

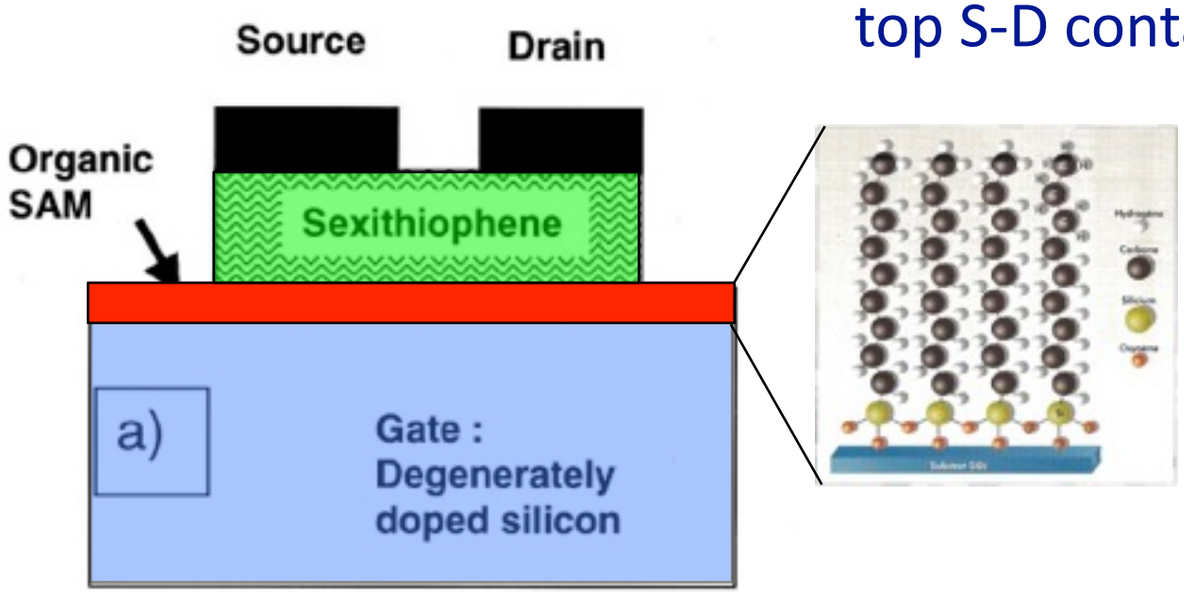
Oxydes

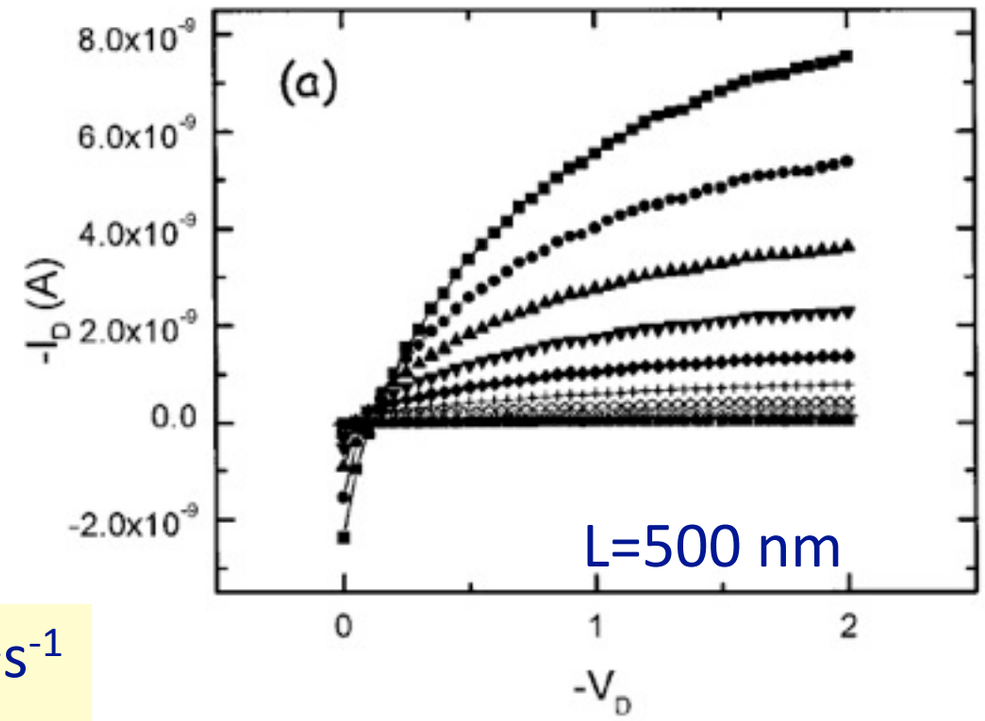
Al_2O_3 ou Al-OH	R–CO_2H, R–PO_3^{2-}, R–PO_4^{2-}
TiO_2	R–CO_2H, R–PO_3^{2-}, R–$Si(X)_3$
ZrO_2	R–$Si(X)_3$, R–PO_3^{2-}
$YBa_2Cu_3O_7$	R–NH_2, R–SH
ITO	R–CO_2H, R–$Si(X)_3$, R–PO_3^{2-}
SiO_2	R–$Si(X)_3$

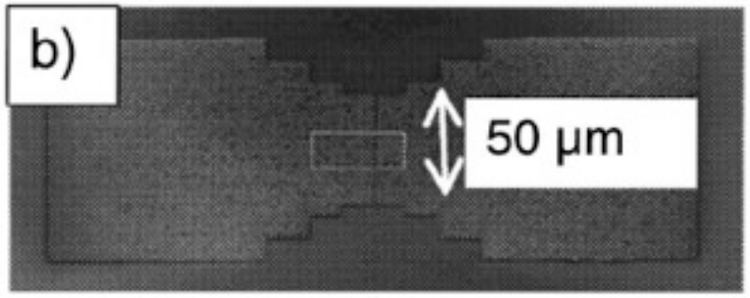
Réf : Love et al., *Chem. Rev.* **2005**, *105*, 1103
R.K. Smith et al., *Progress in Surface Science* **2004**

nano-scale organic transistors

top S-D contacts

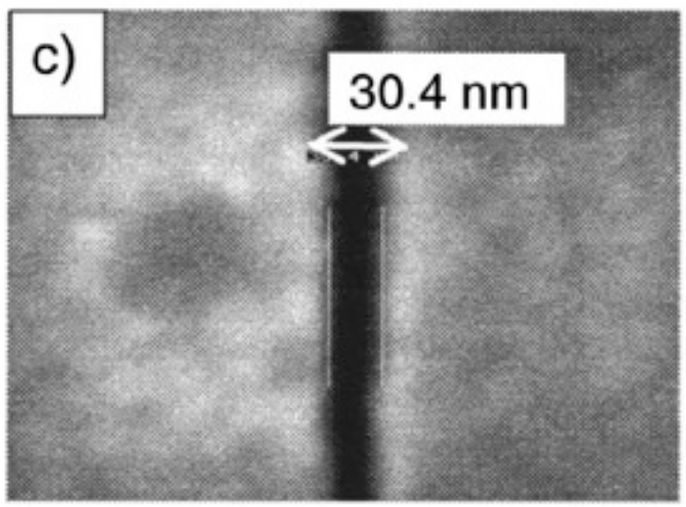


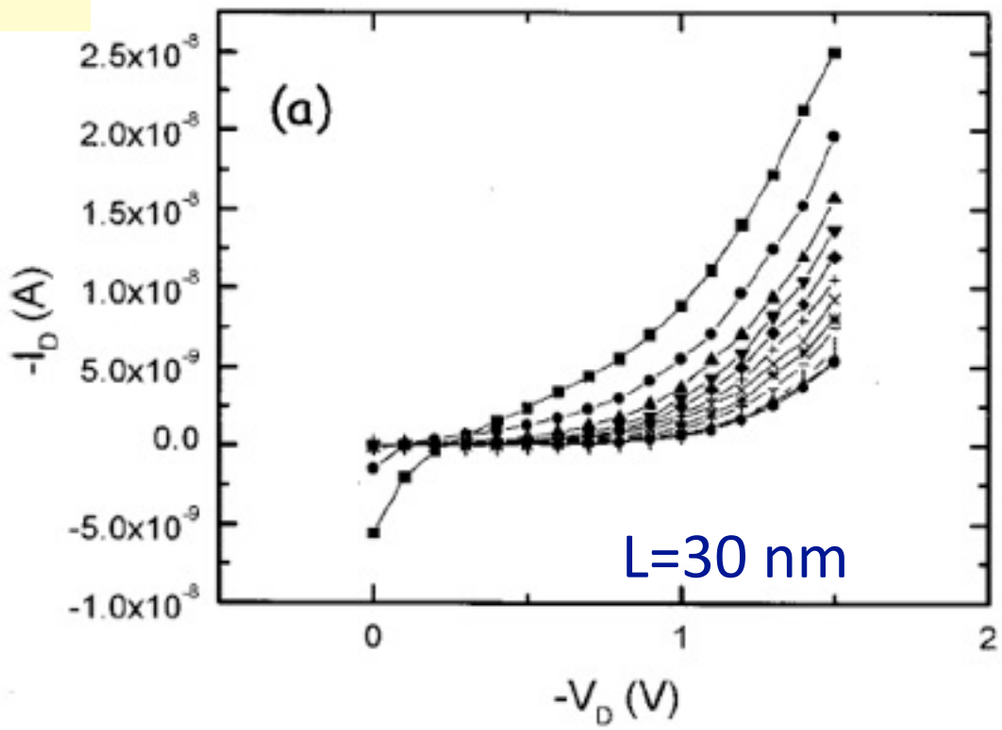




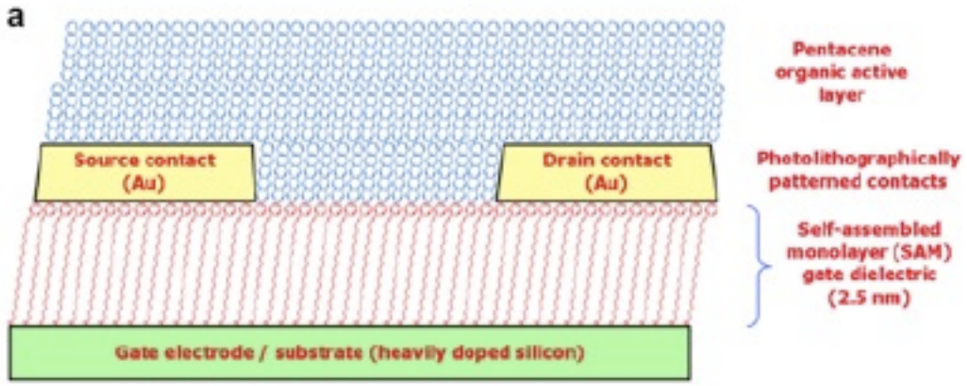
$\mu \approx 10^{-3}\ cm^2V^{-1}s^{-1}$

on/off $\approx 10^4$

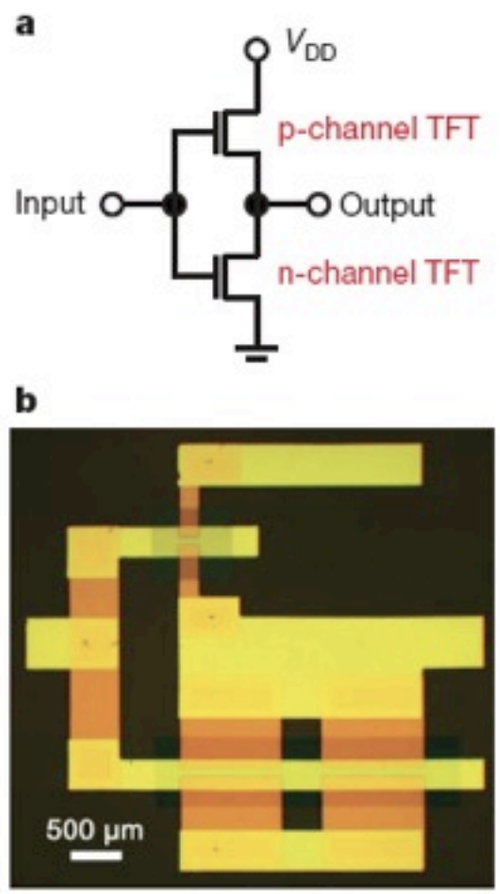


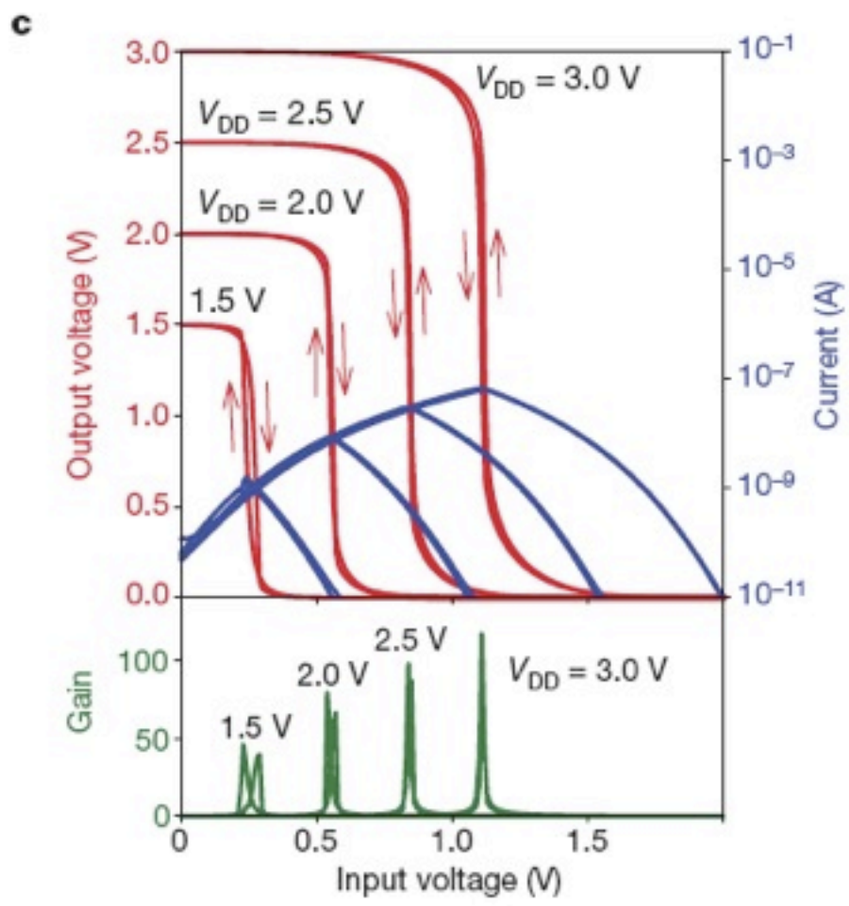


Collet, Vuillaume et al., Appl. Phys. Lett. (2000)



bottom S-D contacts





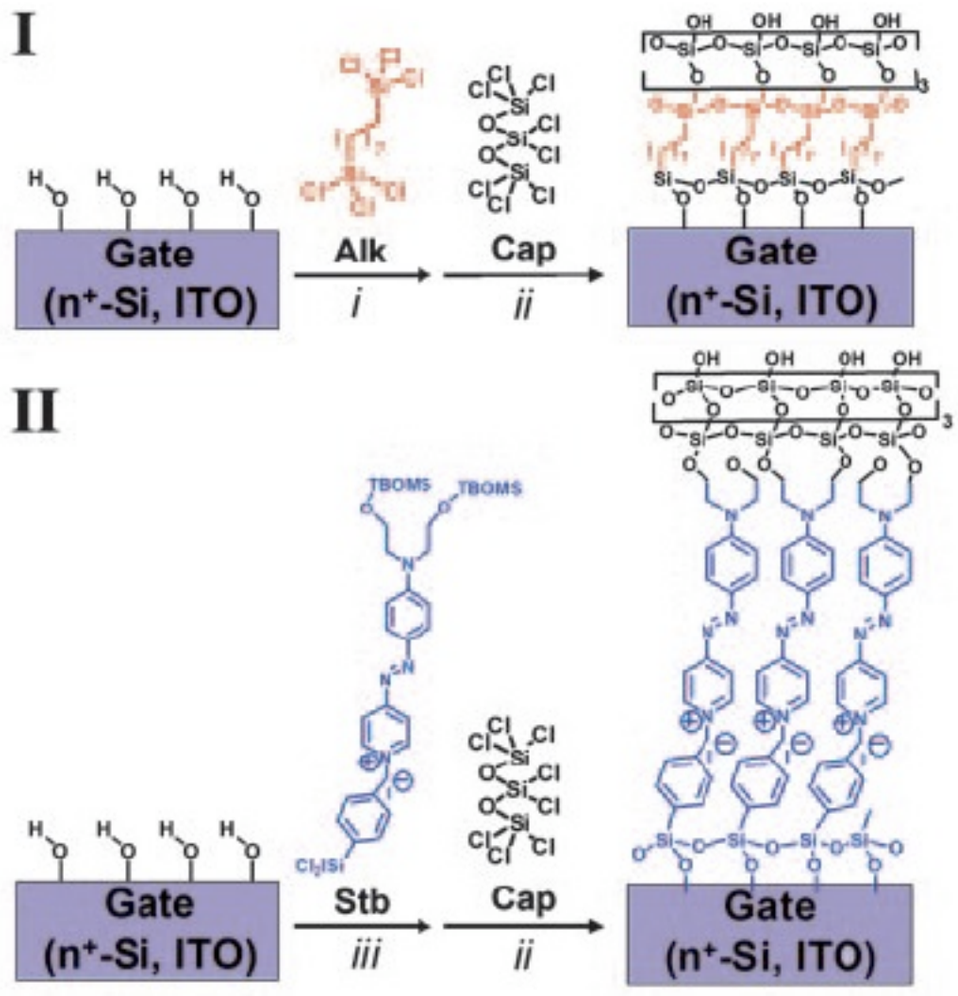
Halik et al. Nature (2004, 2007)

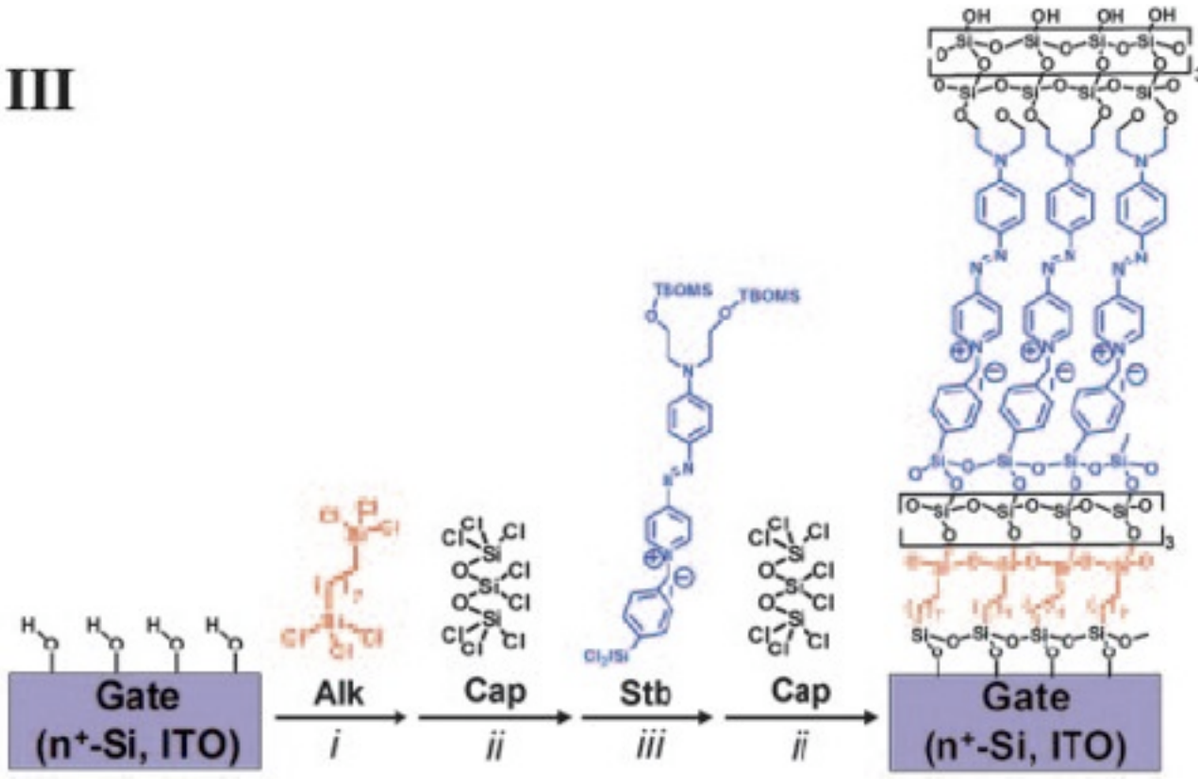
alkyl chains -(CH_2)- : low-k, $\varepsilon_R \approx 2 - 2.5$, $I_{leak} \approx 10^{-8}$ A/cm^2 , E_{BD} up to 15 MV/cm

high-k SANDs : $\varepsilon_R \approx 5\text{-}10$

$I_{leak} \approx 10^{-7}$ A/cm^1 @ 1V

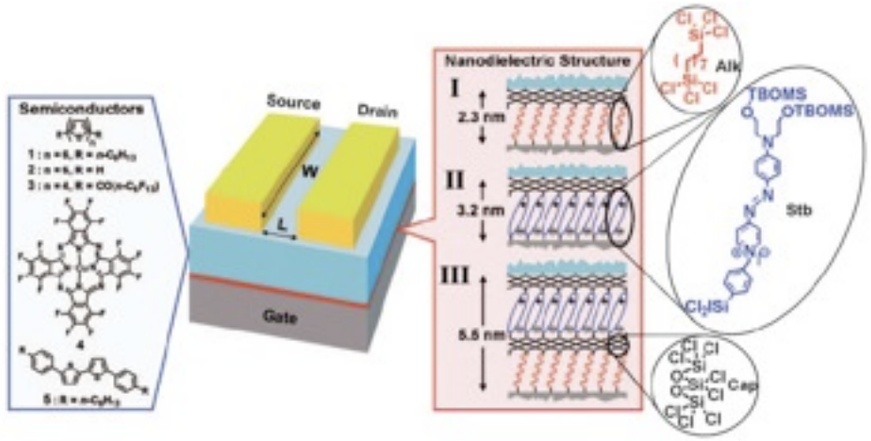
$E_{BD} \approx 7 - 10$ MV/cm





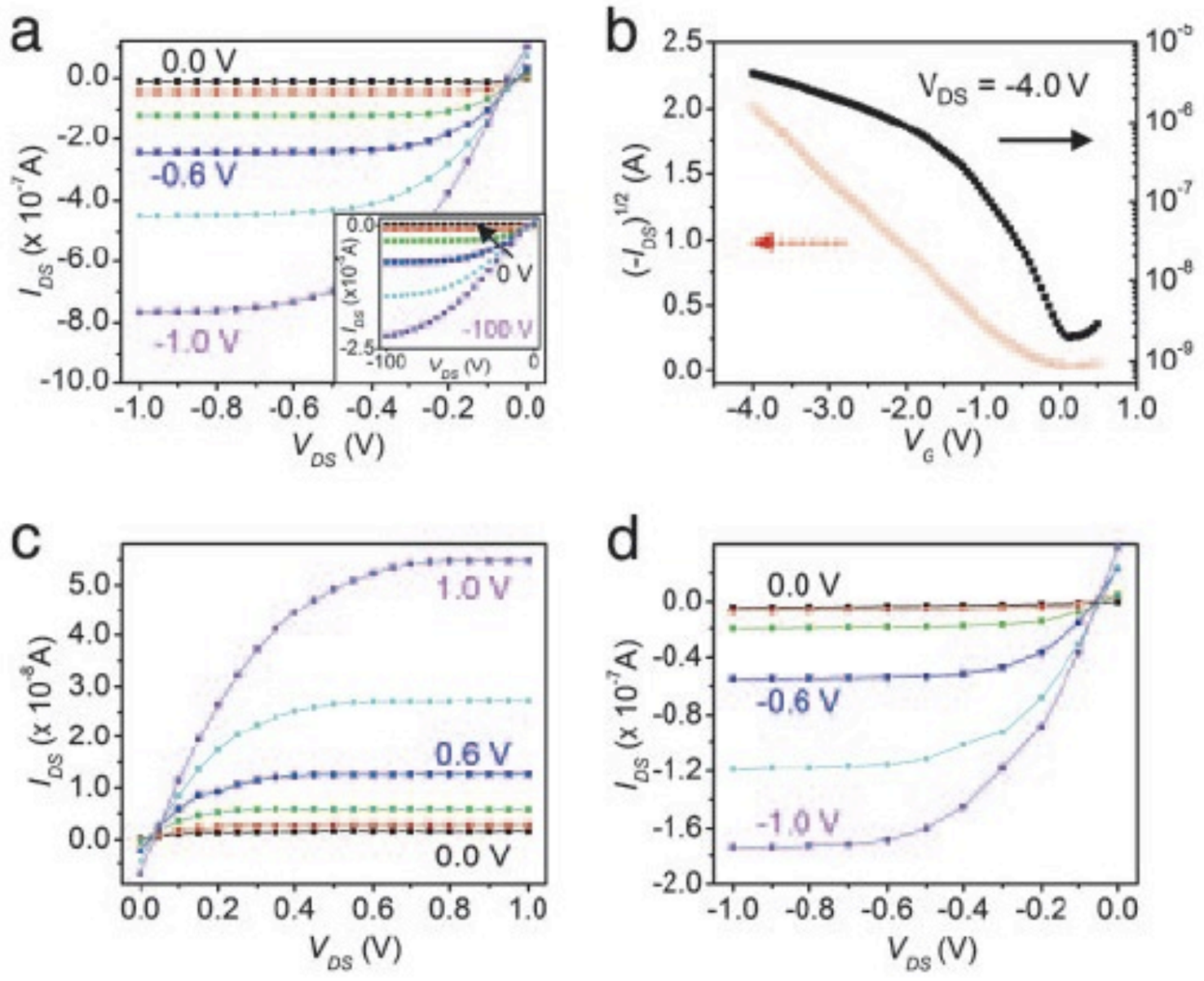
Facchetti, Marks et al. Adv. Func. Mater. (2005)

organic transistors



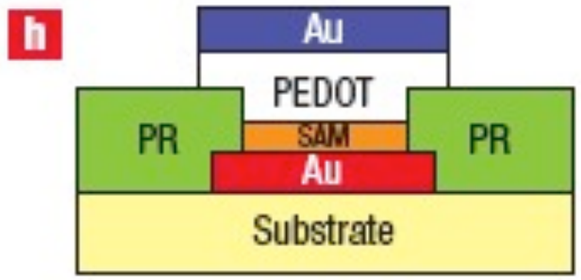
n- and p-type OSC
μ : up to 10^{-2} $cm^2V^{-1}s^{-1}$
on/off : up to 10^5

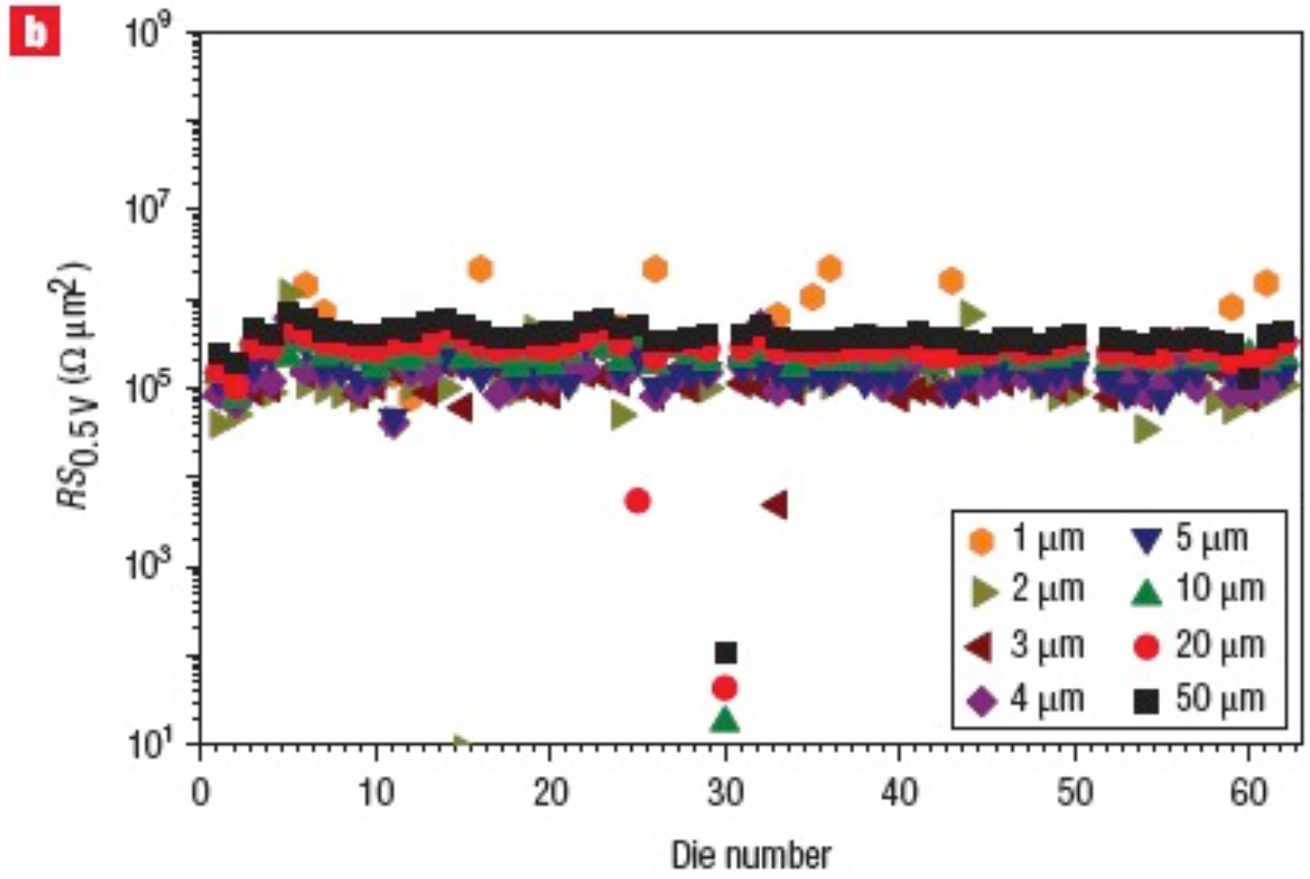
also with CNT 2D network FET

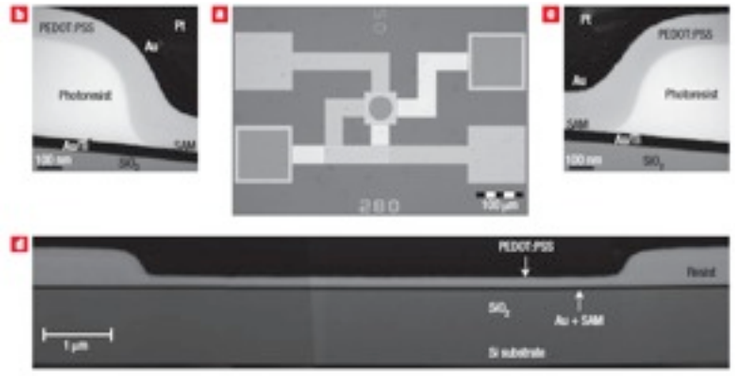


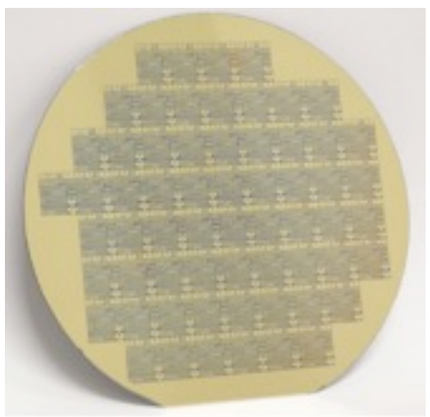
Facchetti, Marks et al., PNAS (2005)

large area molecular junctions @ wafer level



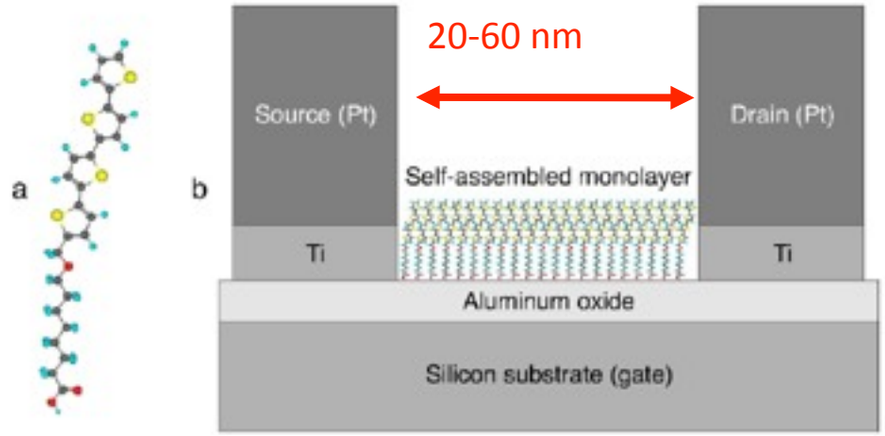


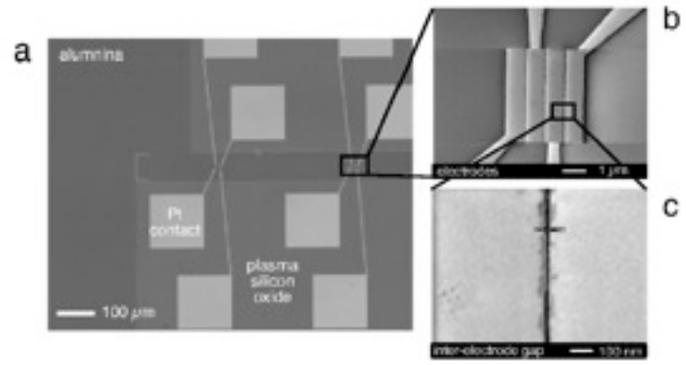


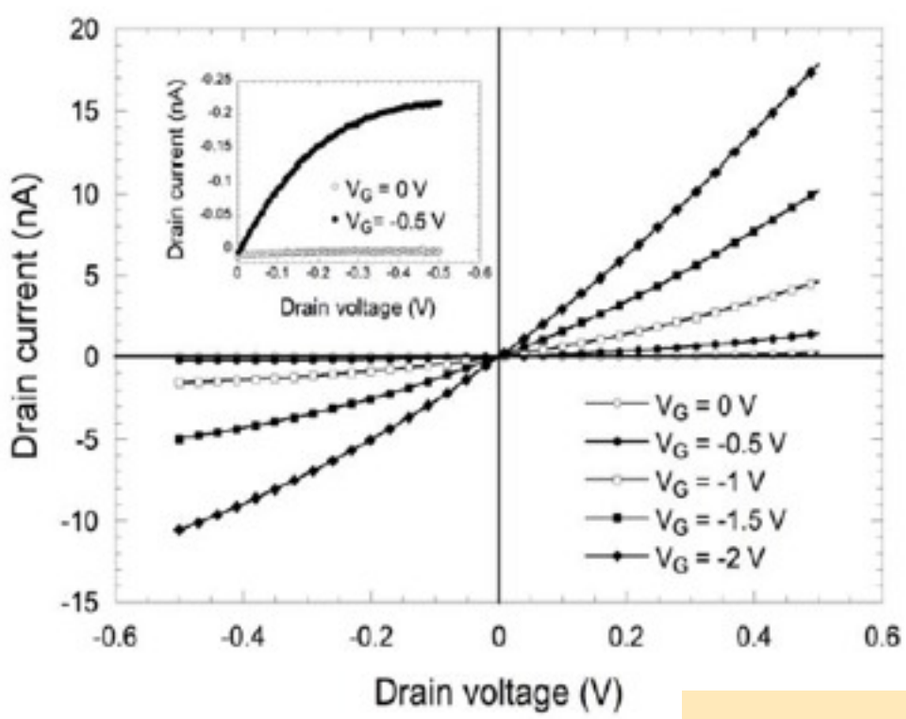


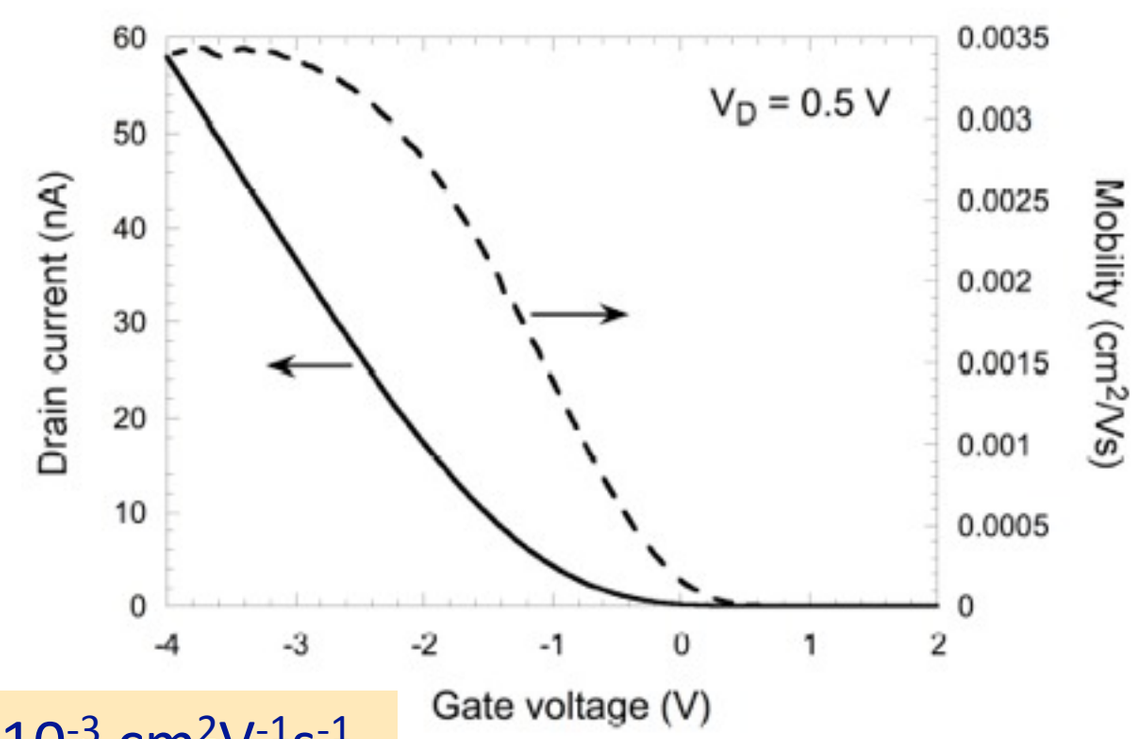
van Hal et al., Nature Nanotech. (2008)

SAM Field Effect Transistor





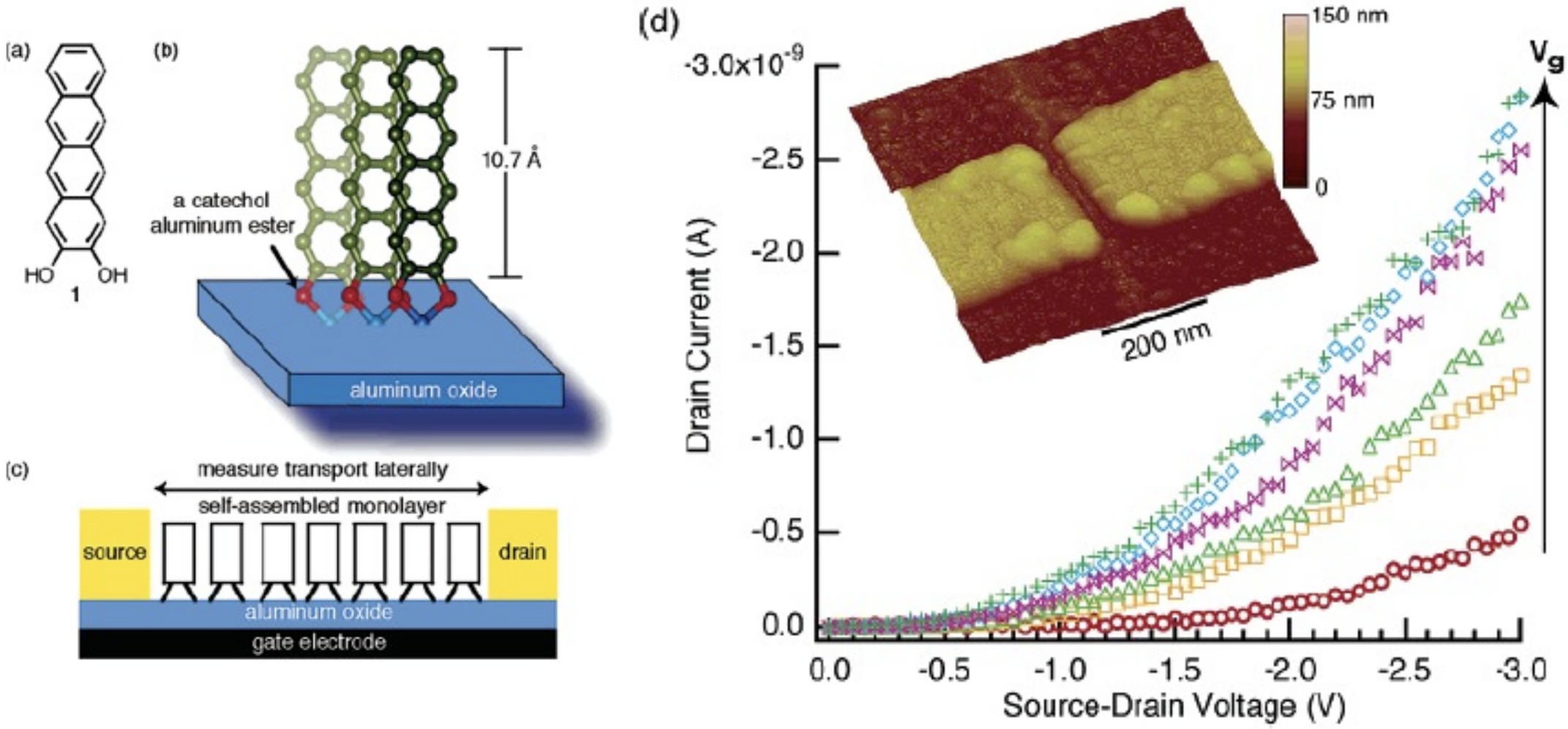




$\mu_{max}=3.5x10^{-3}\ cm^2V^{-1}s^{-1}$

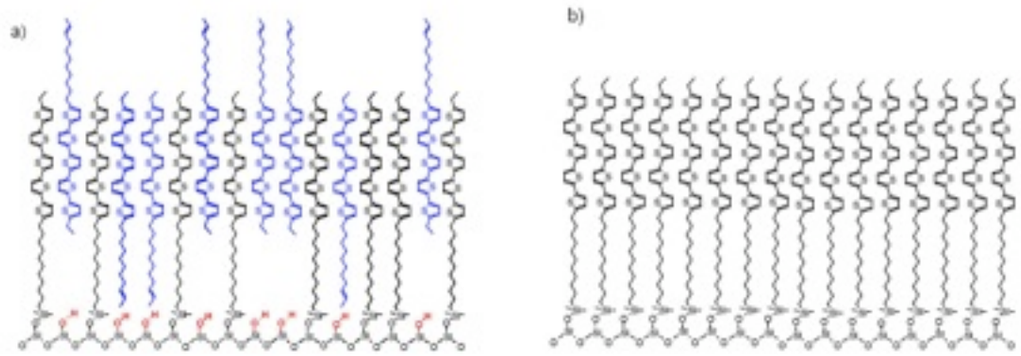
$I_{on}/I_{off} \sim 1800\ (V_D=-0.5V)$

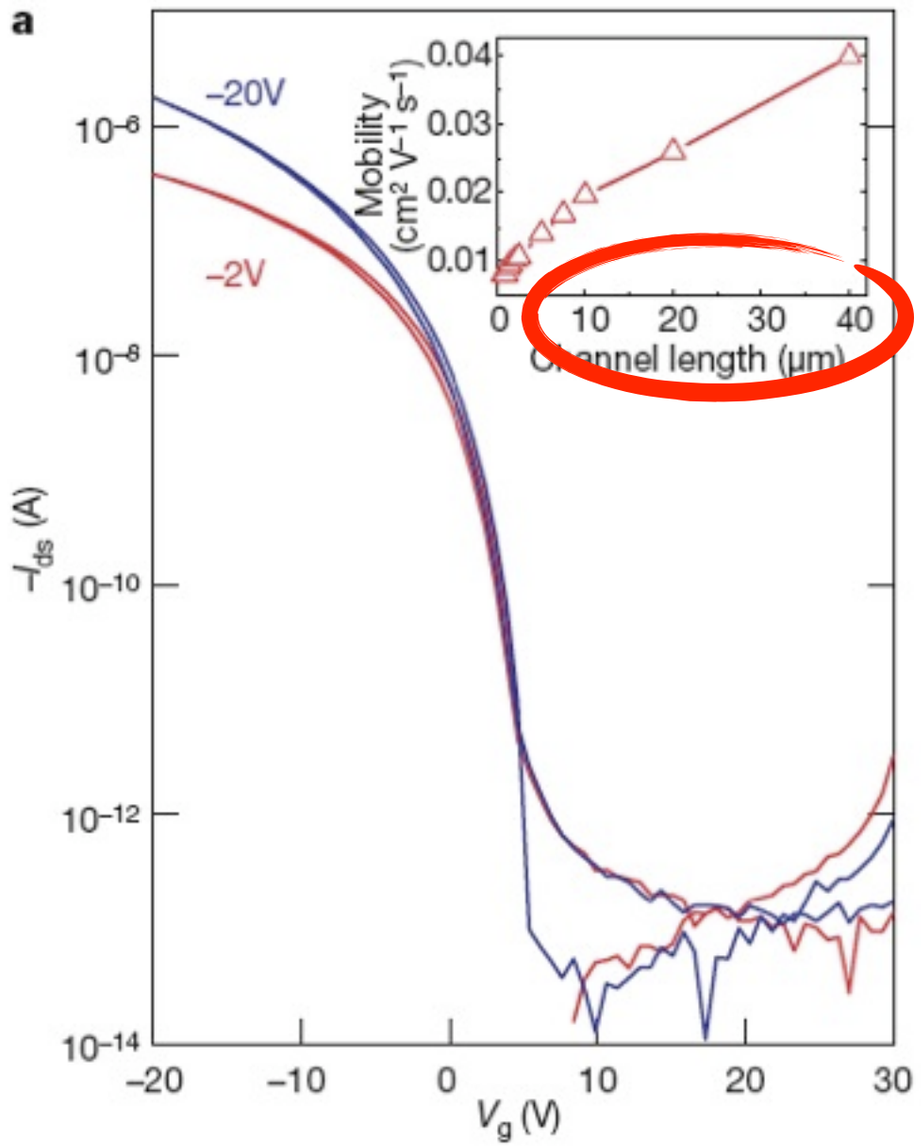
Mottaghi et al., Adv. Func. Mater. (2007)



in the two cases, L ≤ 200 nm

Tulevski et al., J. Am. Chem. Soc. (2004)





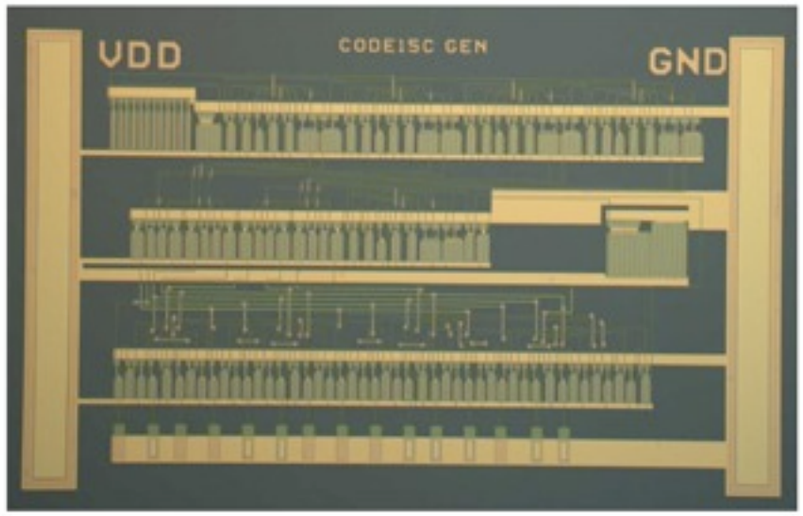
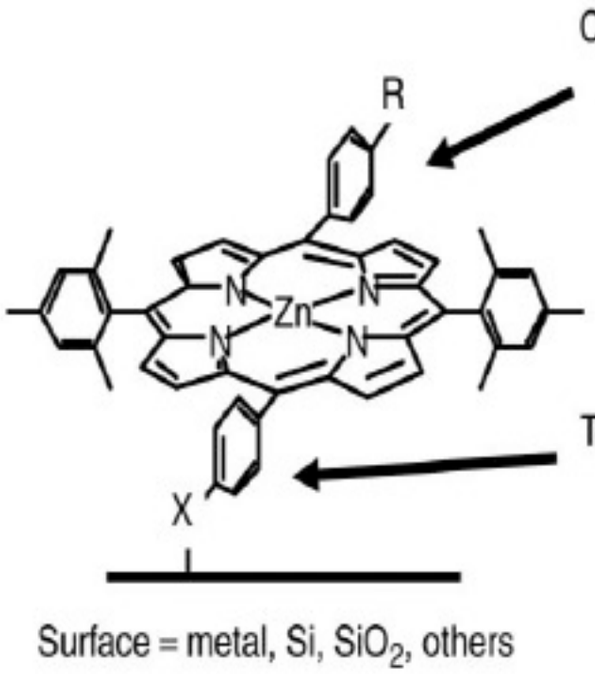


Fig. S31. Optical photograph of a functional 15-bit SAMFET code generator. The circuit combines over 300 SAMFETs.

15-bit code generator
300 SAMFETs

Smits et al., Nature (2008)

Molecular memories & switches



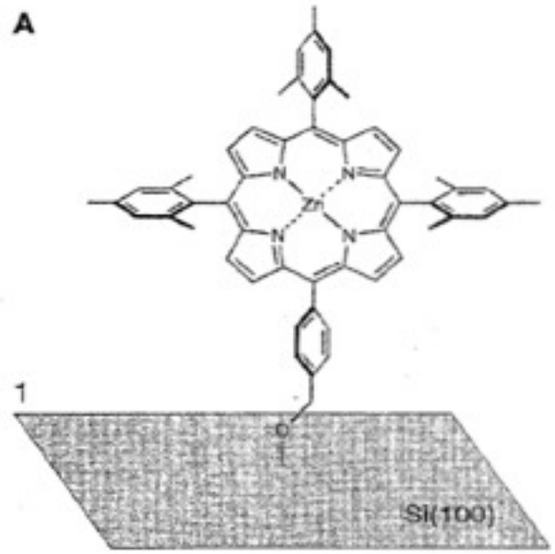
porphyrins

Principle 1 : charge storage on a redox molecule

Table I: Criteria for Incorporation of Molecules in CMOS Storage Devices.

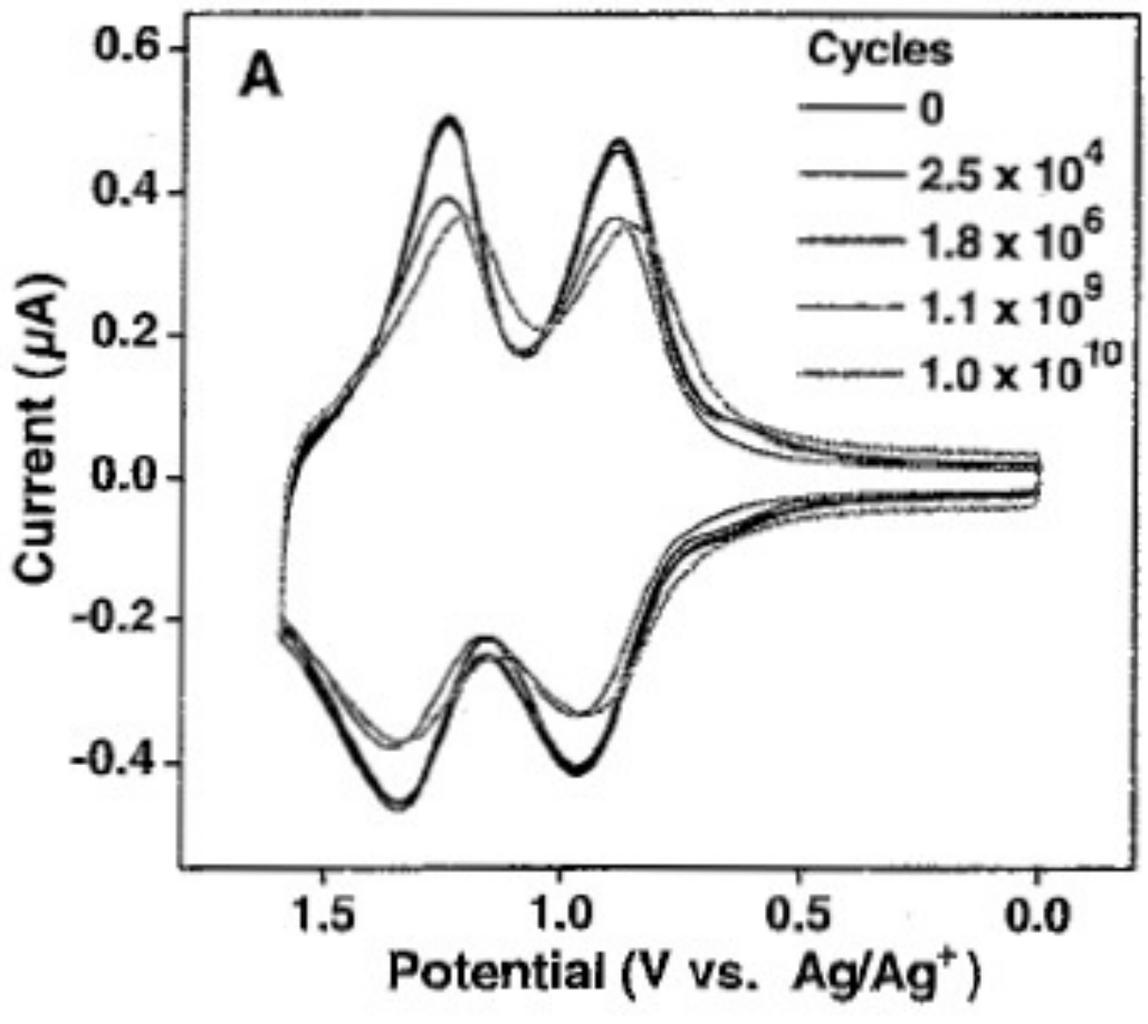
Property	Implementation
Chemical stability	Delocalized cationic charge
Thermal stability	$T_{decomposition} > 400°C$.
Endurance	$>10^{15}$ cycles
Read/write speed	$t_{R/W} = 1/k_{eff} < 10$ ns
Charge retention half-life	$t_{1/2} > 10$ s
Charge density	μ =10 $\mu C/cm^2$ or higher
Self-assembly and self-alignment	Selective covalent bond formation of molecules to specific substrate

W. Kuhr, Mat Res Soc (2004)

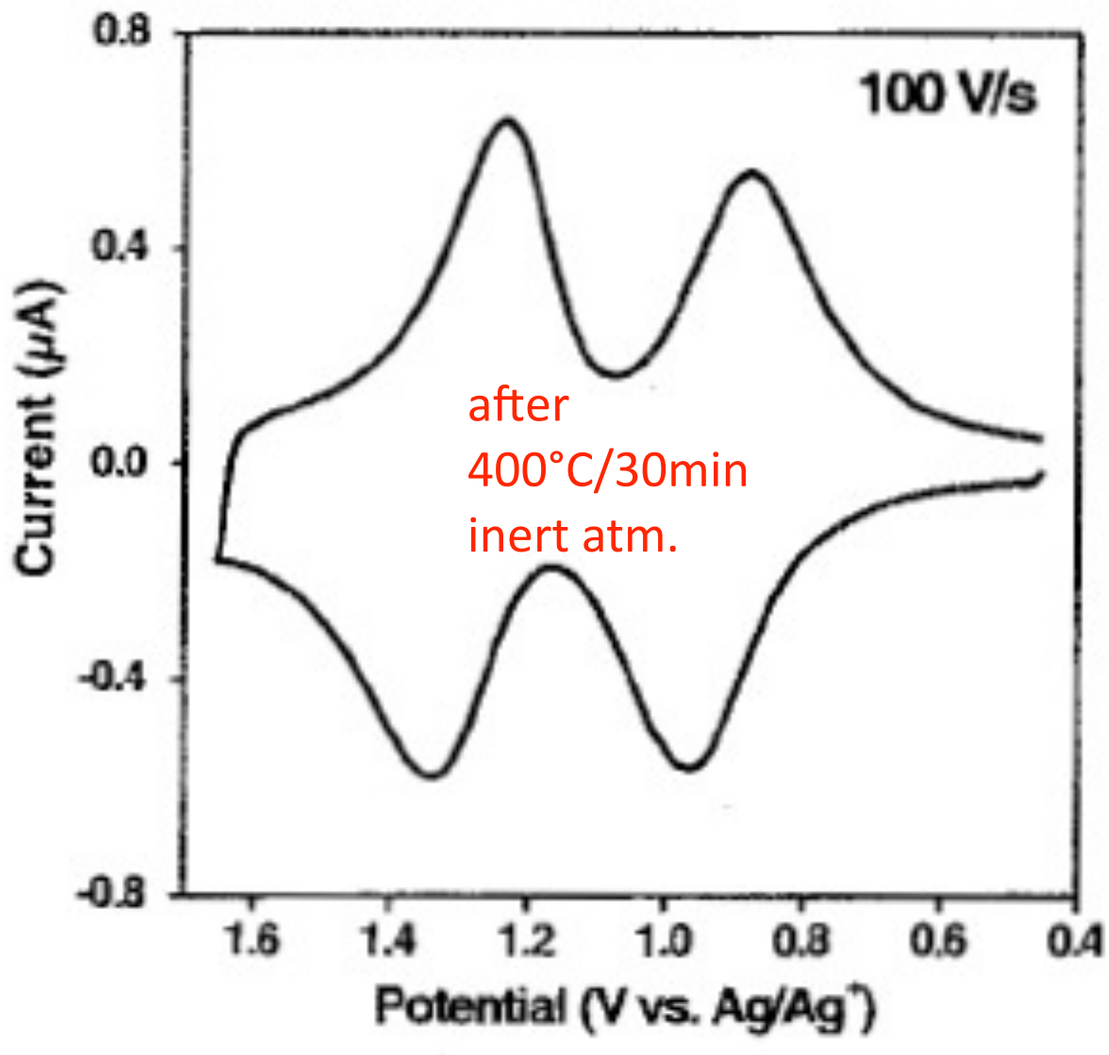


direct grafting on Si-H
CMOS compatible

survive a 400°C process

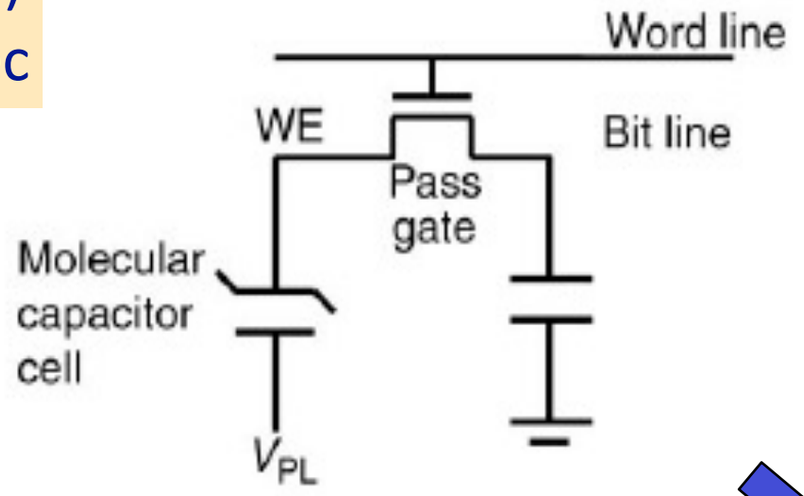


working stability: up to 10^{12} cycles



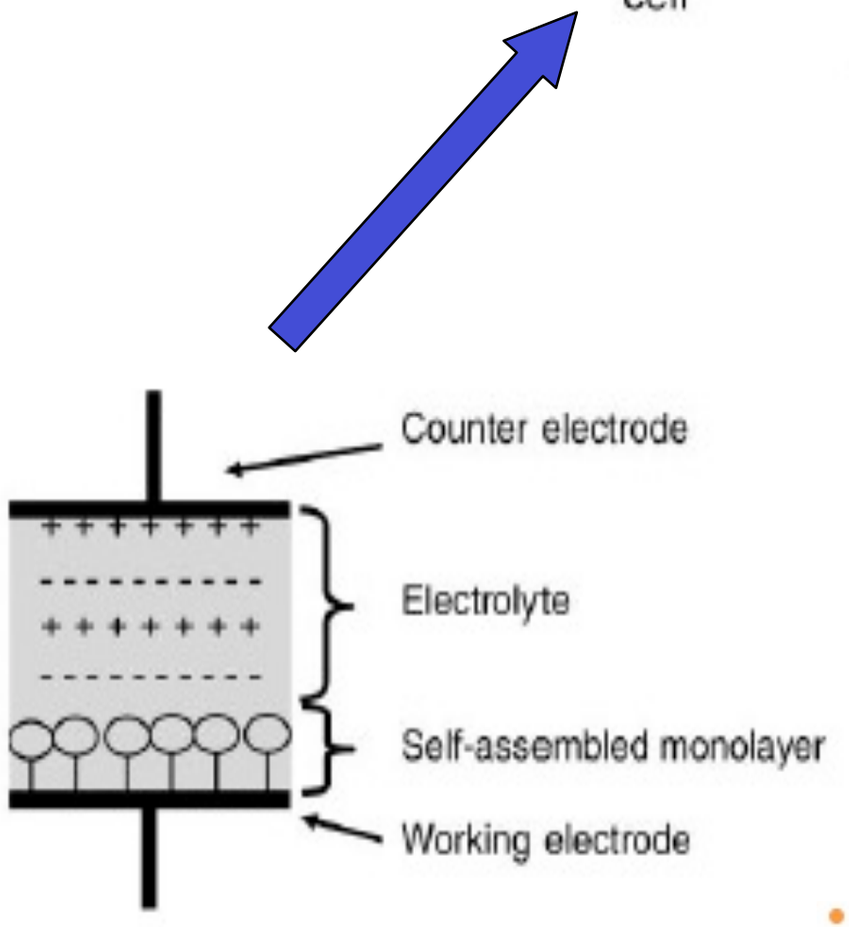
Liu et al., *Science* (2003)

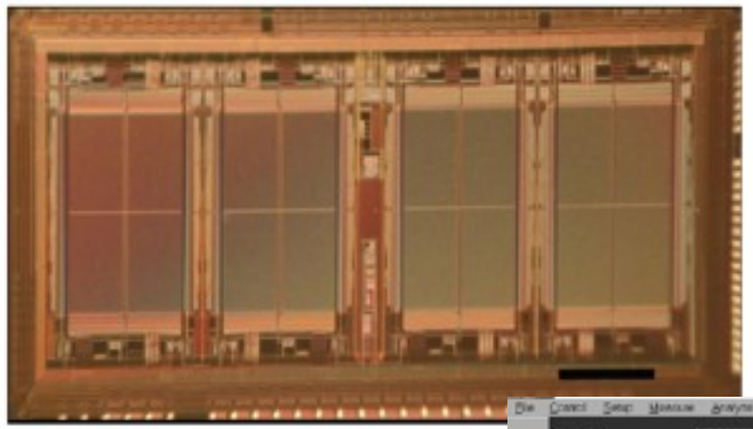
write : 10 µs (theory: 10 ns)
retention : few hundred sec



1Mbit / molDRAM
Zettacore

planar (no trench, no stack)
10% steps/Si DRAM



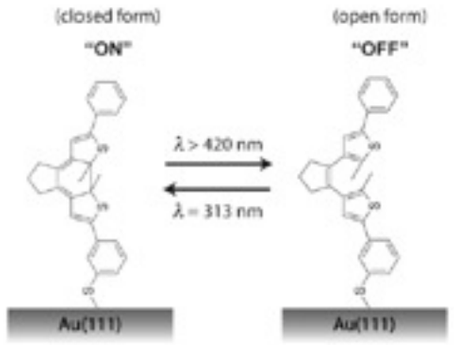


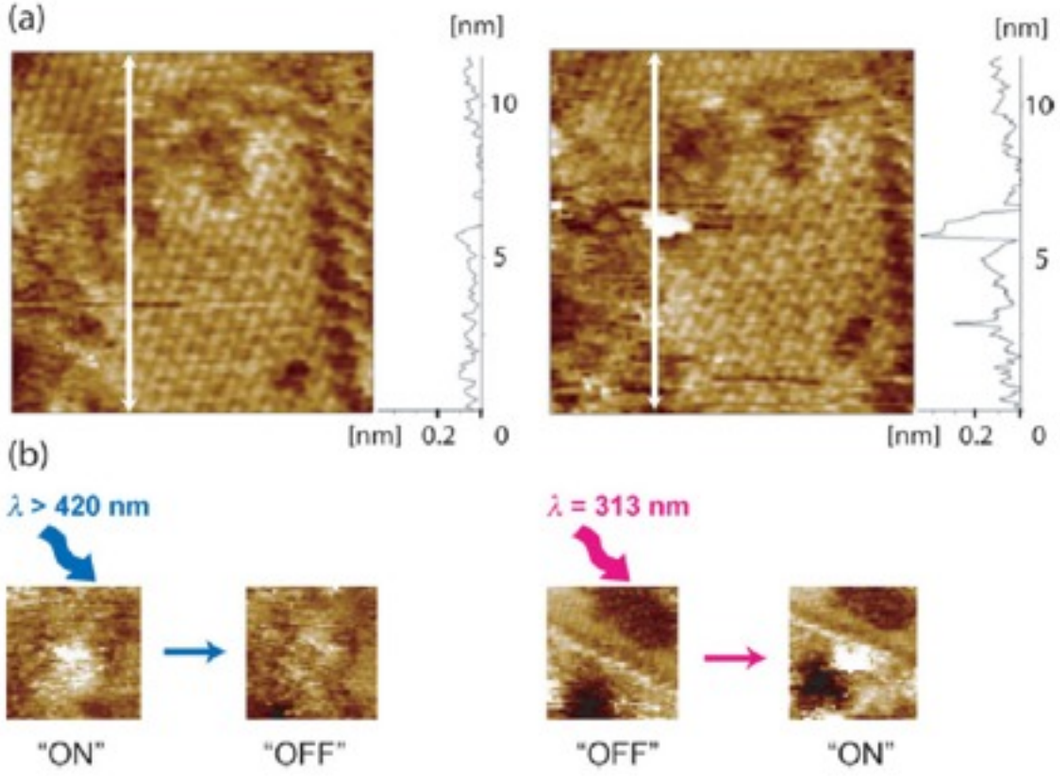
- Evaluations performed to confirm circuit functionality
- Write, read, addressing capability

www.zettacore.com (2005)

Principle 2 : change of molecular conformation, conductance switching

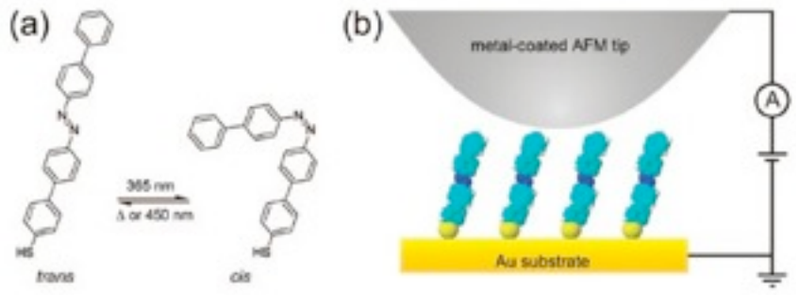
diarylethene

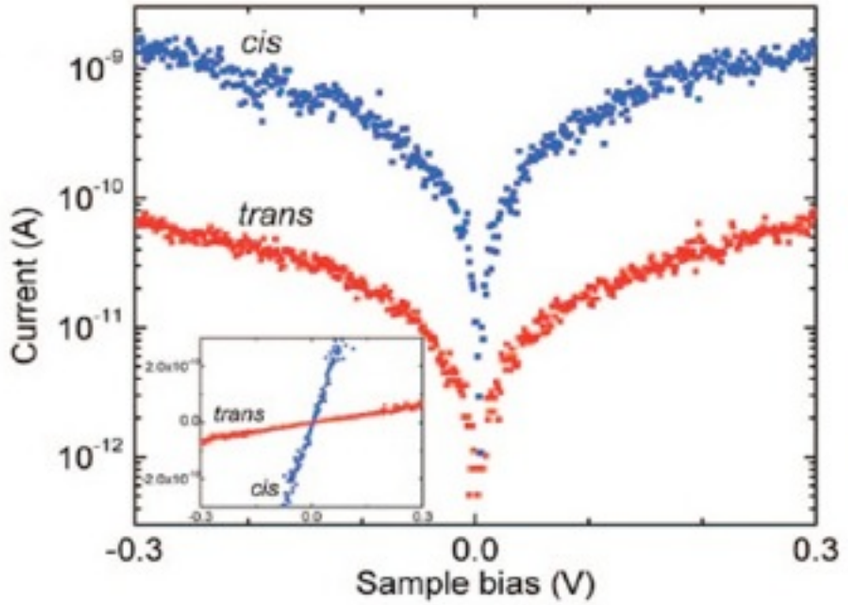




B. Feringa et al., Adv Mater (2006)

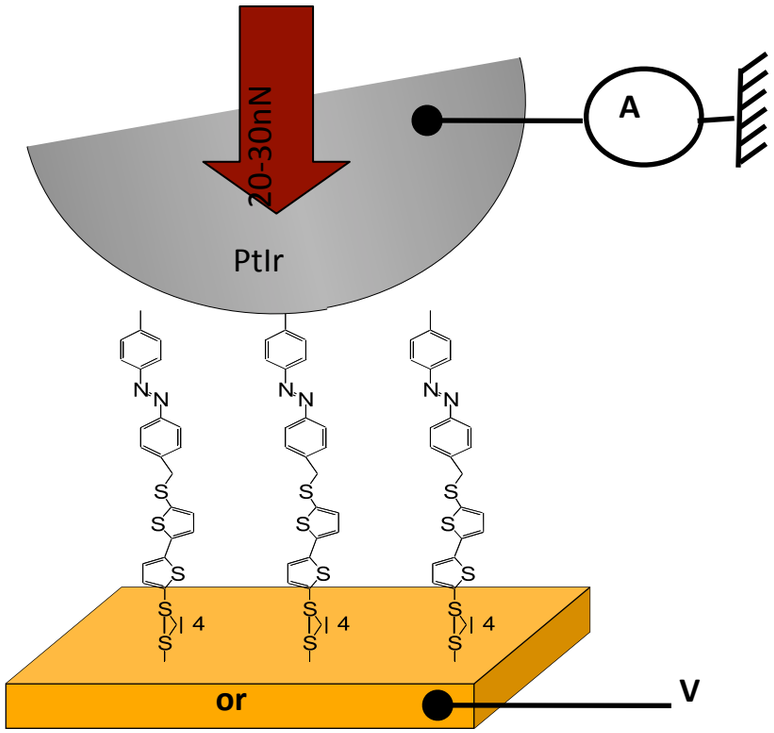
azobenzene derivative

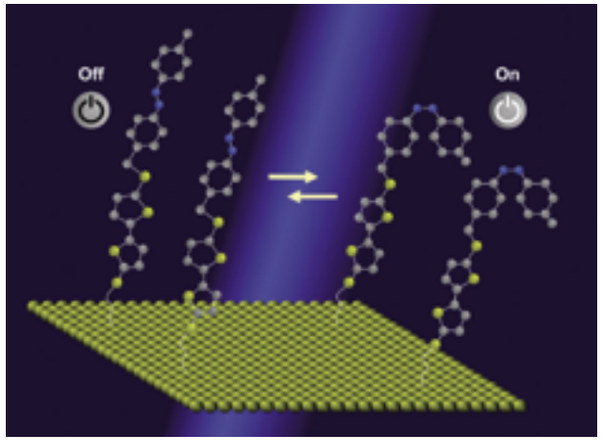


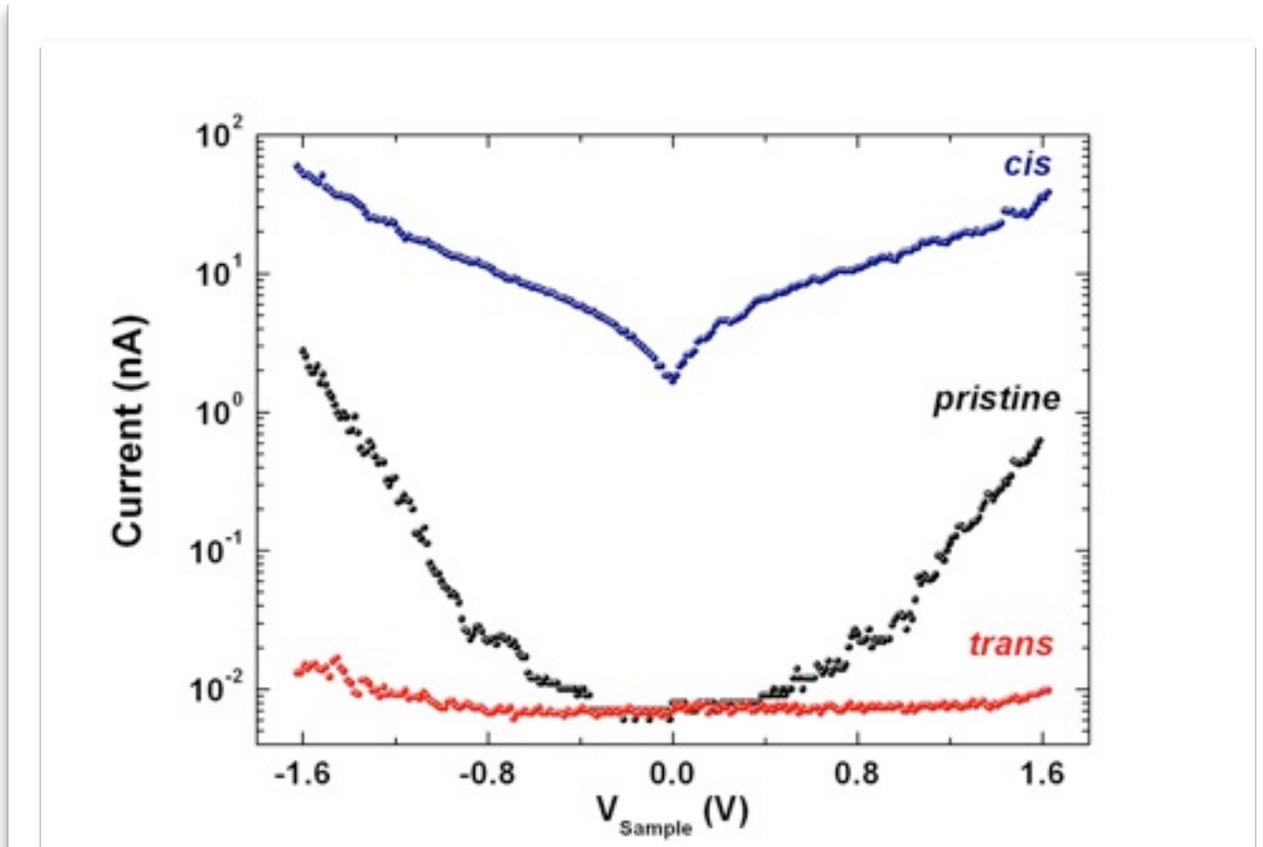


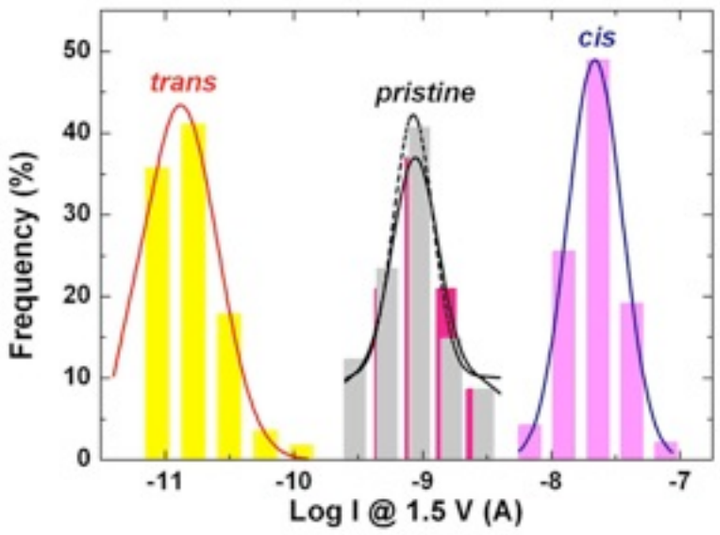
J.M. Mativetsky et al., JACS 2008

on/off ratio < 100









G_{cis}/G_{trans}= 1.5x10^3

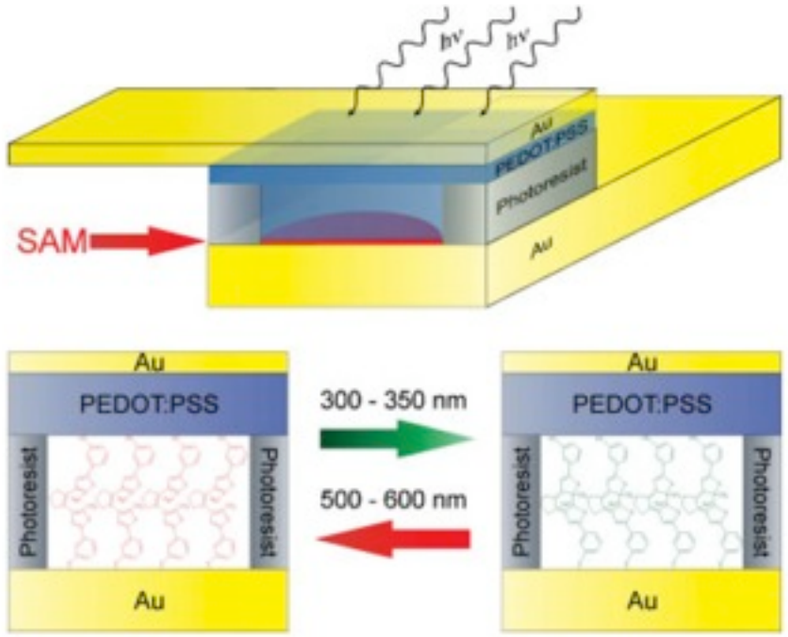
Switching time : $\tau = (\sigma\phi)^{-1}$

$\sigma = 1.5x10^{-18}$

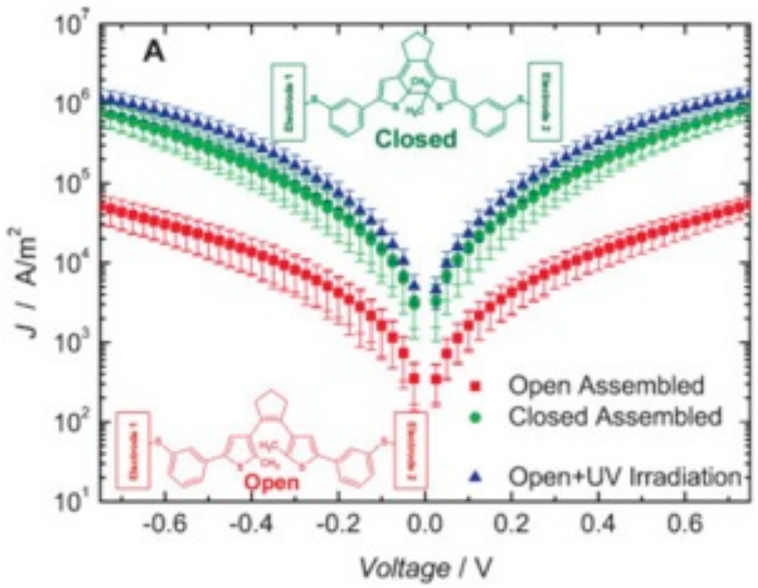
1-10 µs if intense light

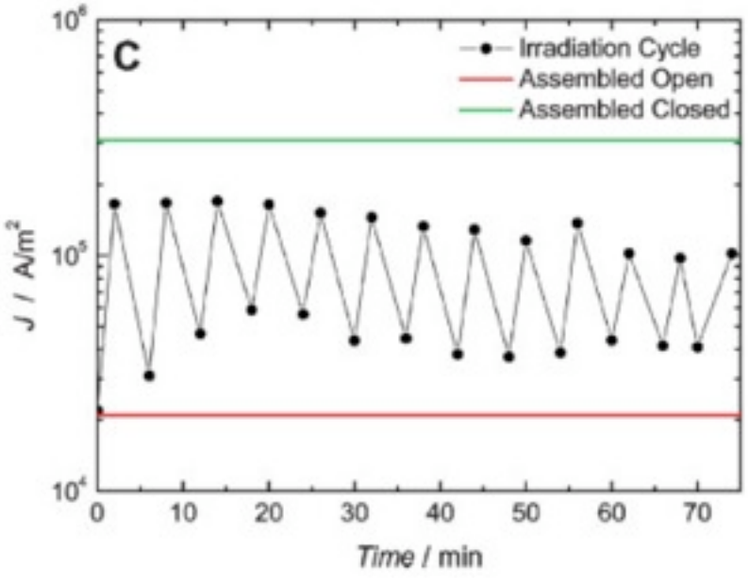
Smaali et al., ACS Nano (2010)

Towards a useful "solid-state" device



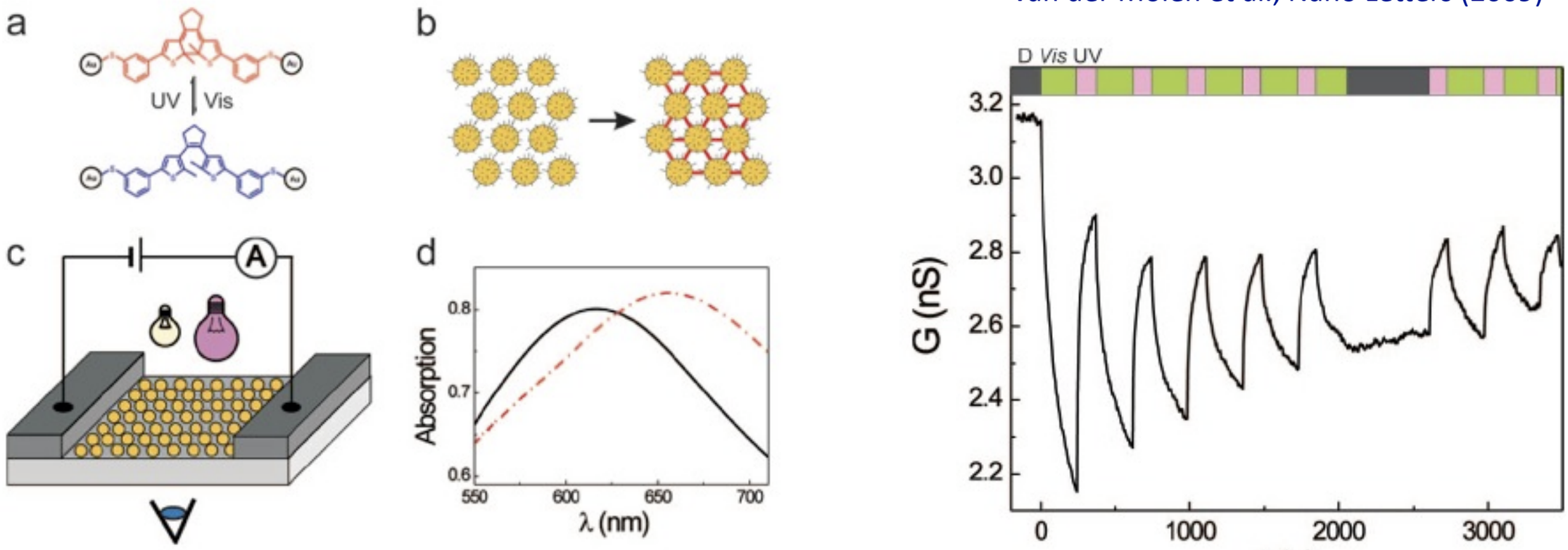
suitable for large-area electronics





Kronenmeijer et al., Adv. Mater. (2008)

Van der Molen et al., Nano Letters (2009)



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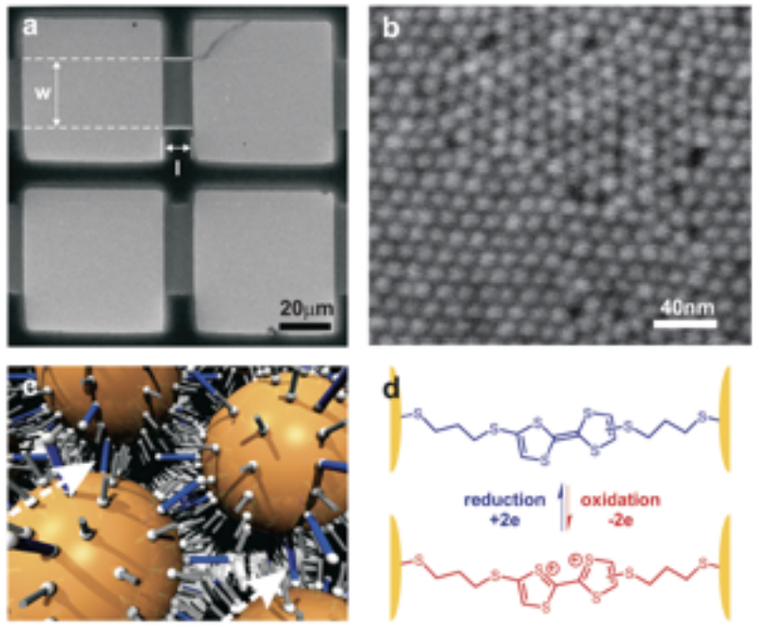
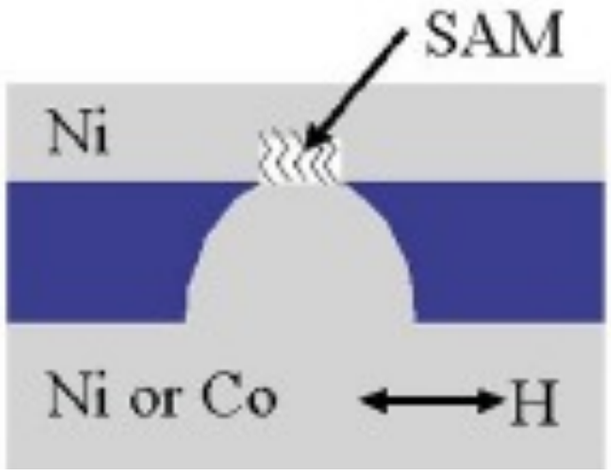
off=open



Liaoet al., Nano Letters (2011)

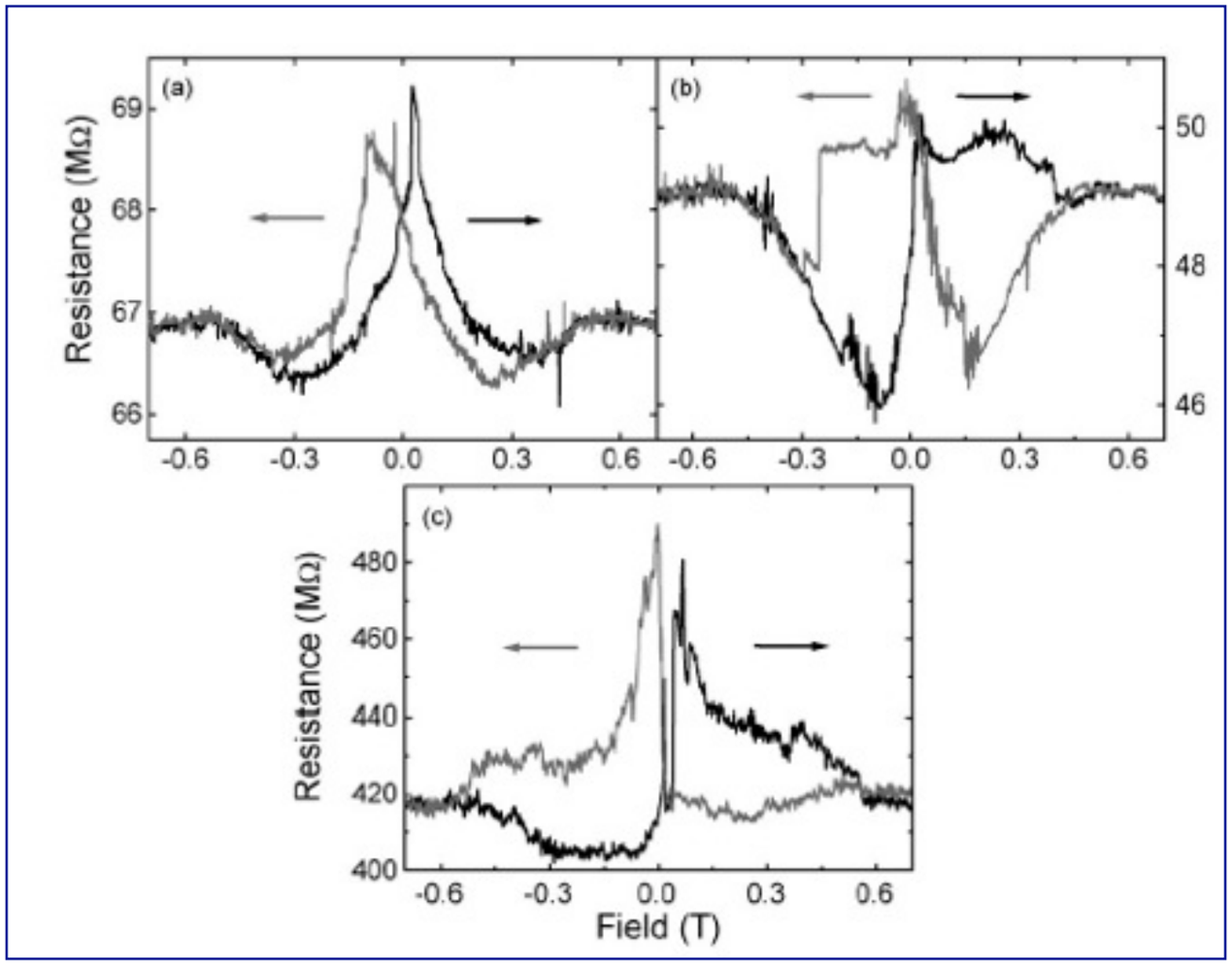
Molecular spintronics

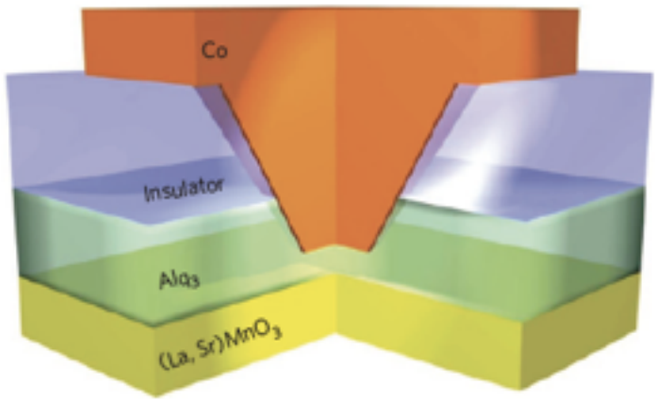


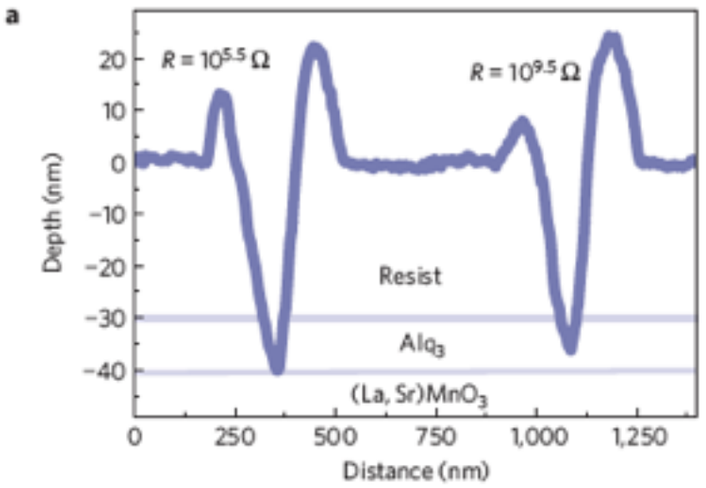
J.R. Petta et al., *Phys. Rev. Lett.* (2004)

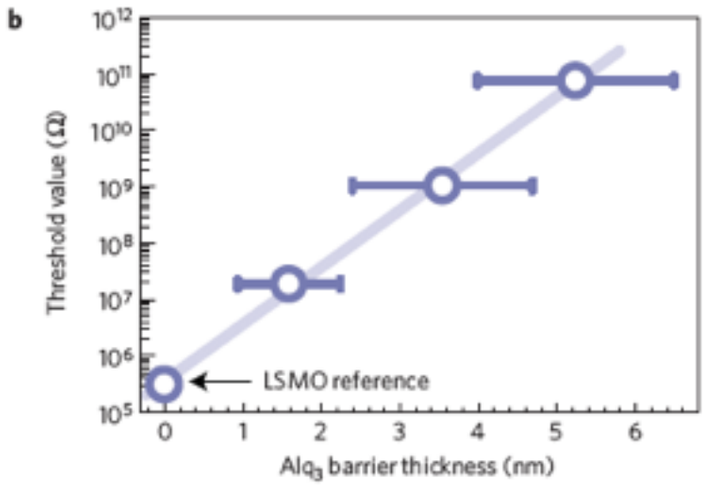
1rst demonstration of TMR through a SAM junction

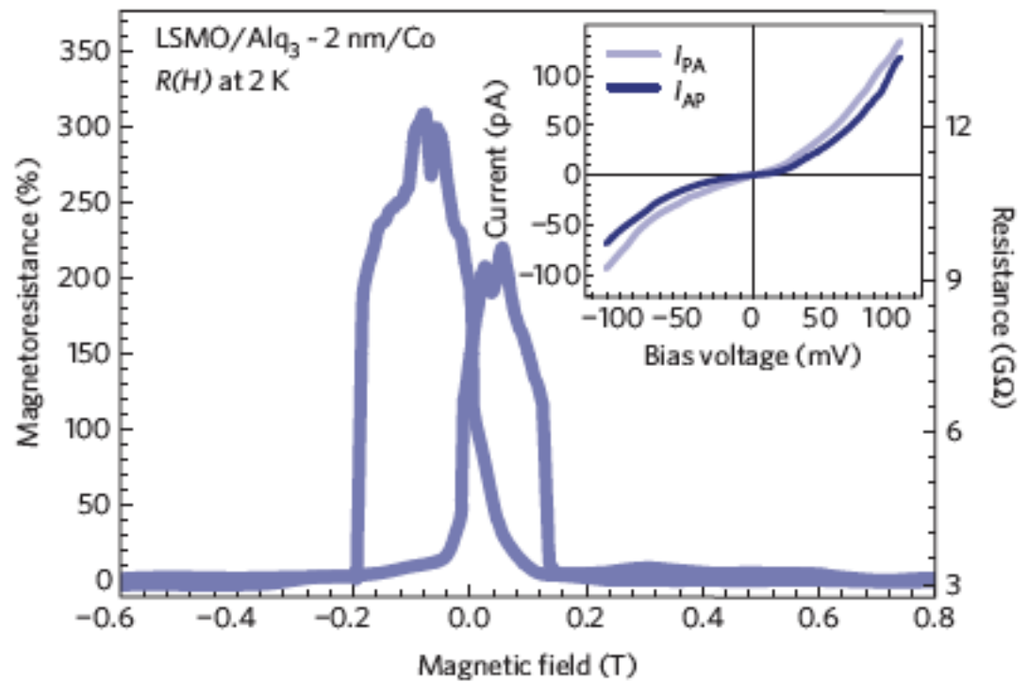
≠ samples









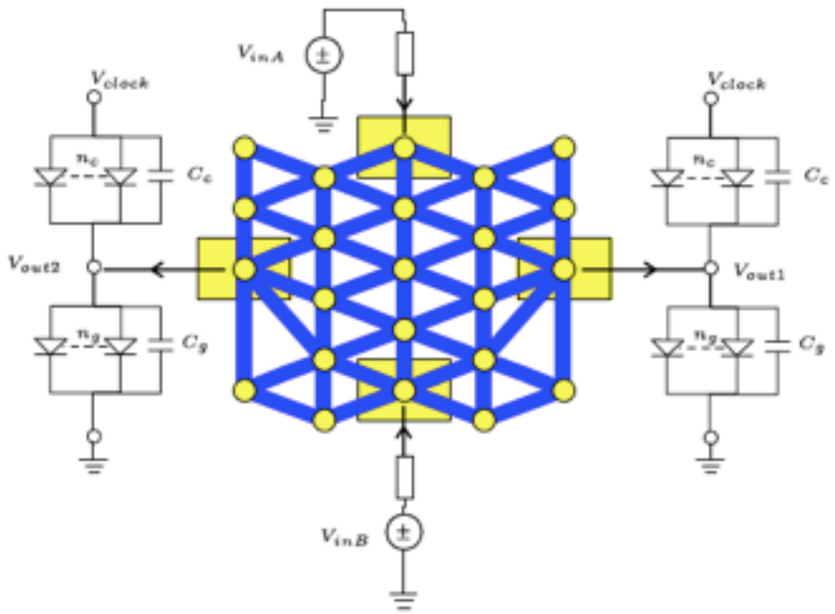


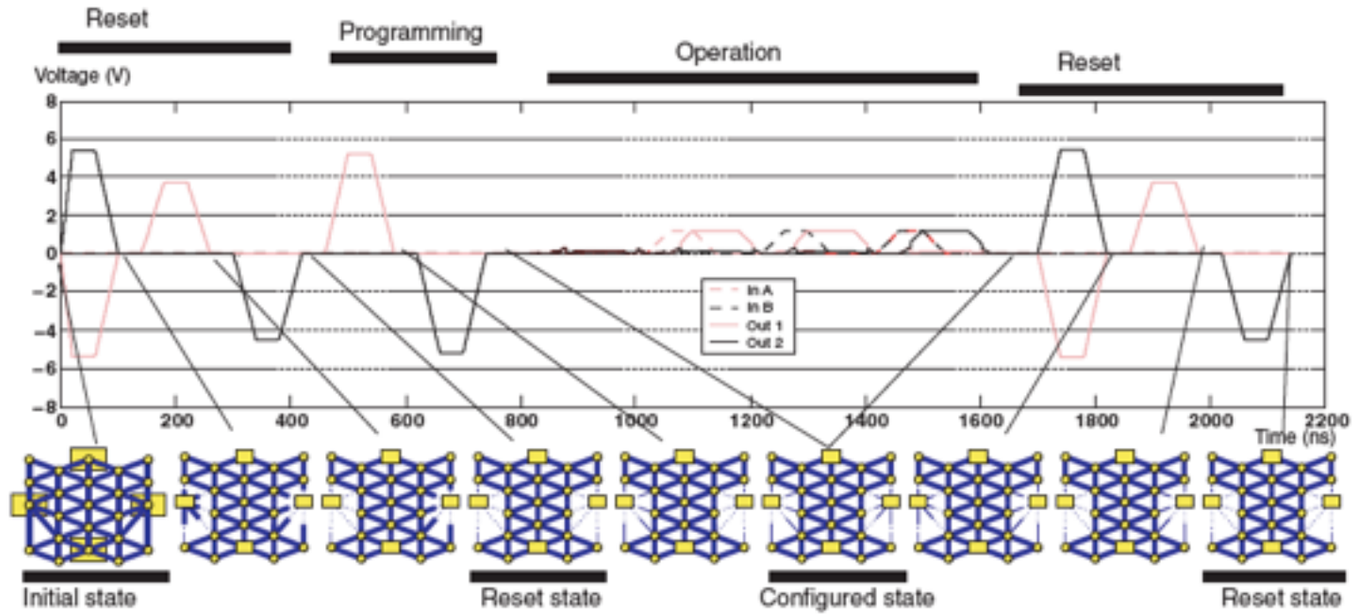
65% of working devices
Among those, 20% with TMR 10-300%

Barraud et al., Nature Physics (2010)

Molecular approaches for non-conventional computing

reconfigurable logic in molecular switching ntework





Skölberg & Wendin, Nanotechnology (2007)

Thank you for your attention

MEMS
design ← → technology

Lina Sarro

DIMES

(**D**elft **I**nstitute **M**icrosystems & nano**E**lectronic**s**)

Delft University of Technology

NANO-TEC

Athens, 13-14 Oct 2011

dimes

TU Delft

MEMS:

Micro-Electro-Mechanical-Systems

Microsystems employ **miniaturization** to achieve high complexity in a small space

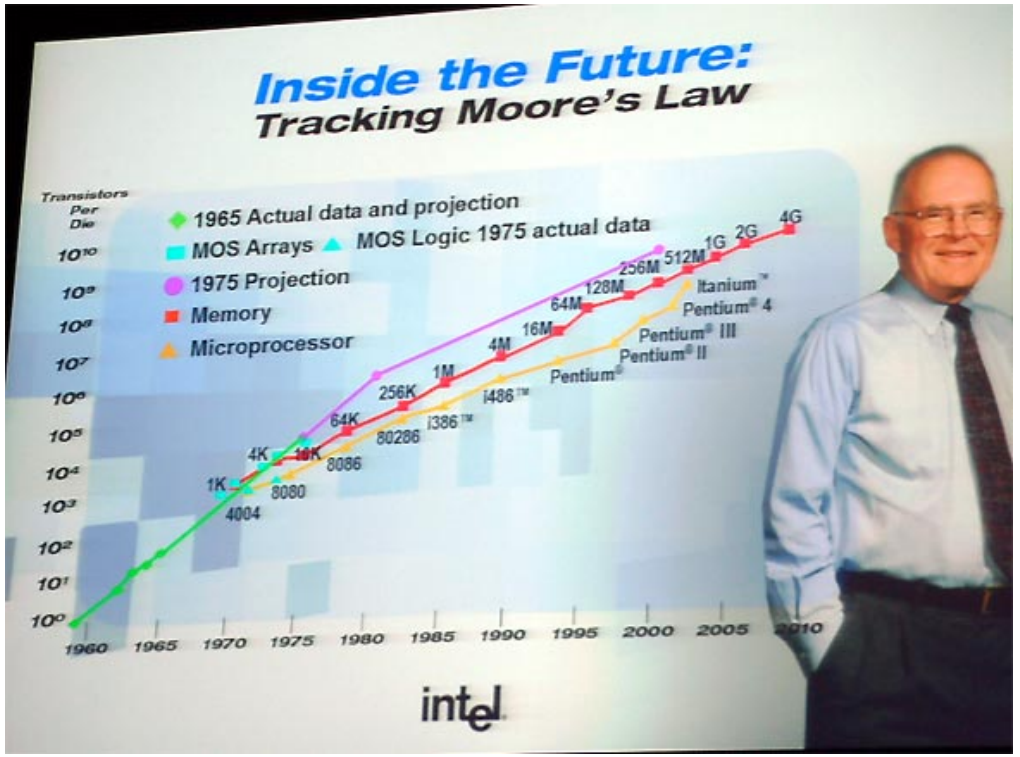
Generally fabricated using modified integrated circuit (IC) fabrication techniques and materials ➔ Si-based

NANO-TEC

TU Delft

Microelectronics ➔Moore's Law

Miniaturization: More transistors per chip area



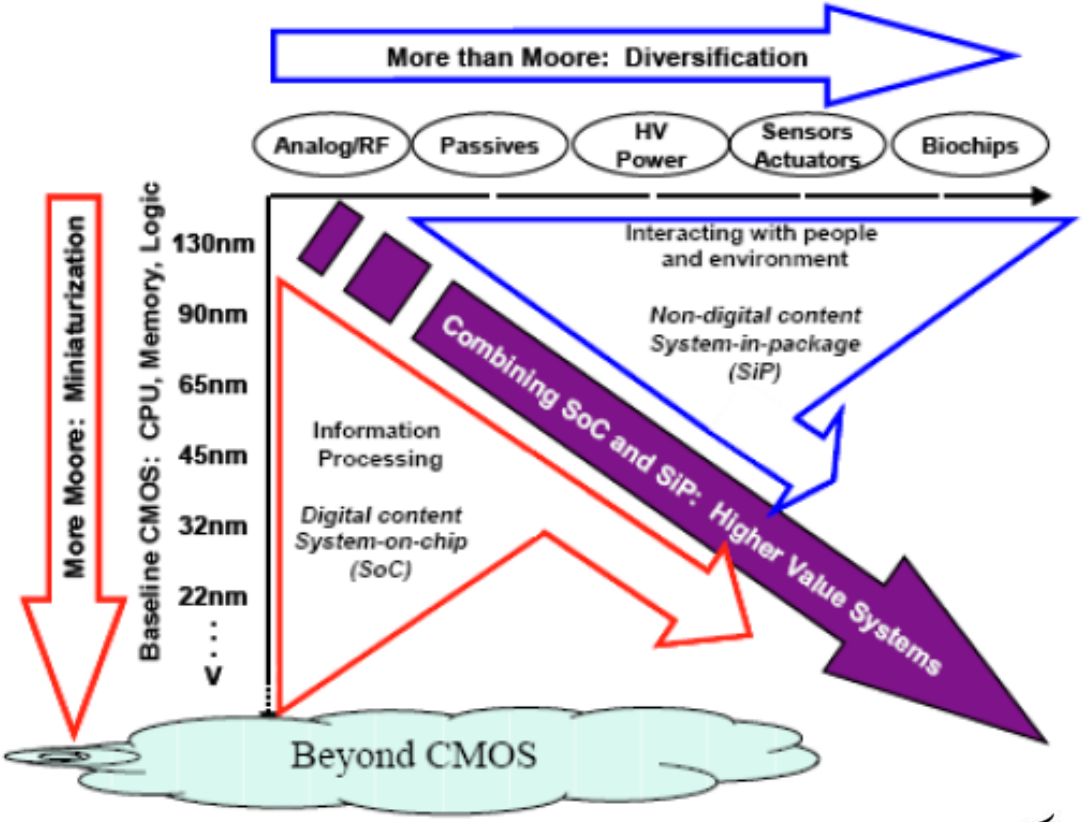
NANO-TEC

dimes

TU Delft

MEMS ➔More than Moore

Miniaturization: More functions per chip area



NANO-TEC

TU Delft

Generic / Application related Requirements for MEMS

- *High sensitivity/High resolution*
- *Low noise*
- *Stable/robust*
- *Fast response*
- *Small*
- *Low cost*
- *Low power*
- *Non contaminant/non invasive*
- *Non contaminable*
- *Compatible with meso and nanoelectronics*

“Ingredients” for MEMS development

- *Physics, Material science,Chemistry*
- *Technological Processes: IC* $^{++}$ and more
- (Biology)
- Dedicated CAD
- “Dedicated” packaging

MEMS ⟷ IC

Many Similarities as well as Differences

- Technology
- Design
- Testing/Reliability
- Applications

  - » How much “standardization” possible/desirable/feasible?

MEMS ⟺ IC

No unit cell

No single "front end" technology, 3D

Multidimensional Interaction space

Very Multidisciplinary

Generally low volume

Application specific ➔ design & technology

Unit cell: transistor

CMOS, 2D

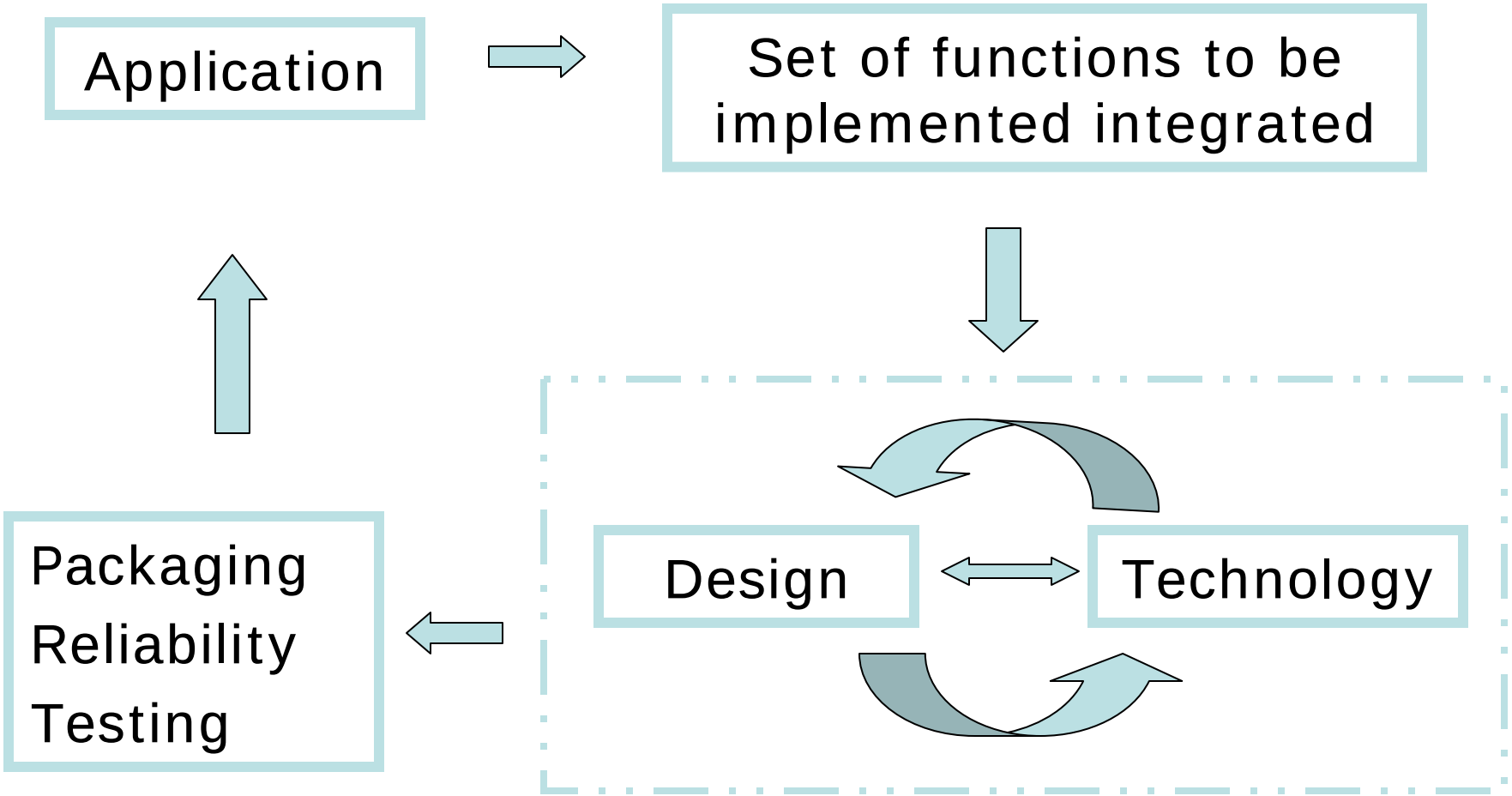
Electrical Connections

Physics & Engineering

Generally large volume

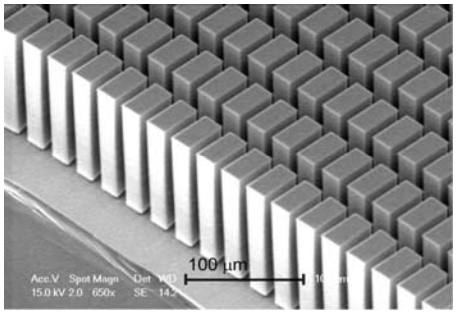
Application specific ➔ design

MEMS

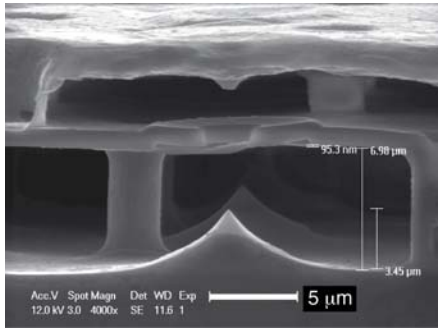

Application
Set of functions to be implemented integrated
Design
Technology
Packaging
Reliability
Testing

Technologies

- (Bi)CMOS
- Bulk Micromachining
- Surface Micromachining
- High-aspect ratio machining
- Wafer-to-wafer bonding
- Thin-film encapsulation
- ……



HAR fin-channel structure for microevaporator



SMM double cavity

3D micro / nano structuring

3D structures needed

to integrate specific functions

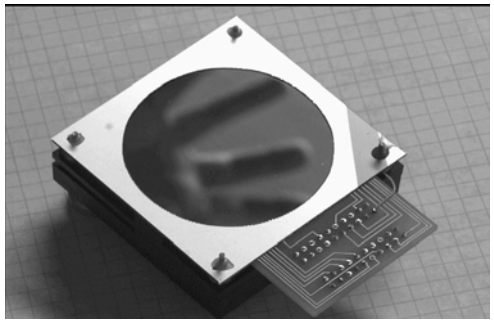
to enhance performance

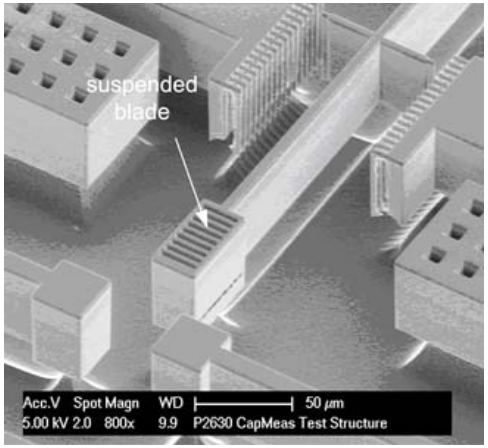
to miniaturize complete system

"Main" Technology:

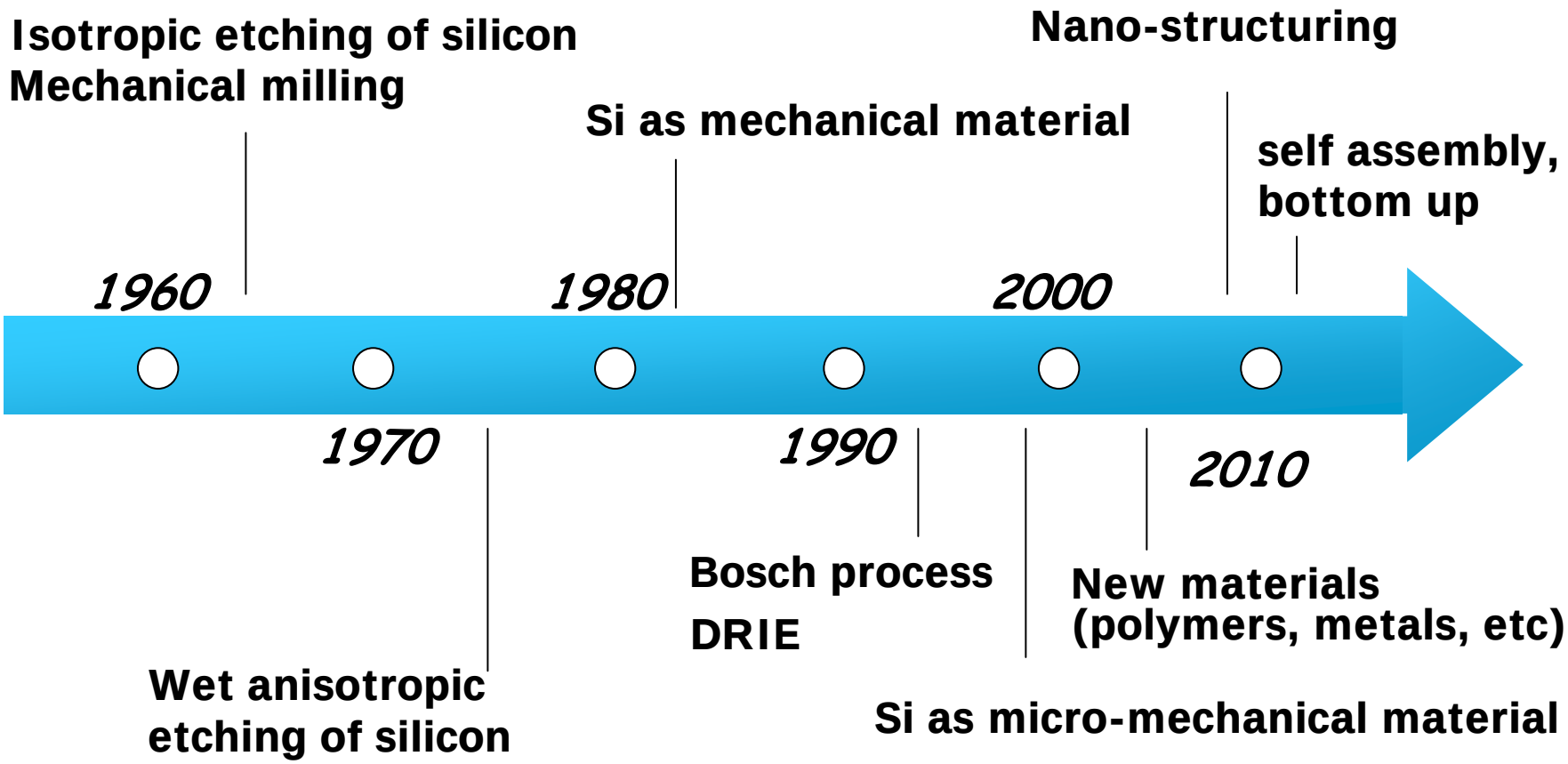
Bulk Micromachining

Surface Micromachining

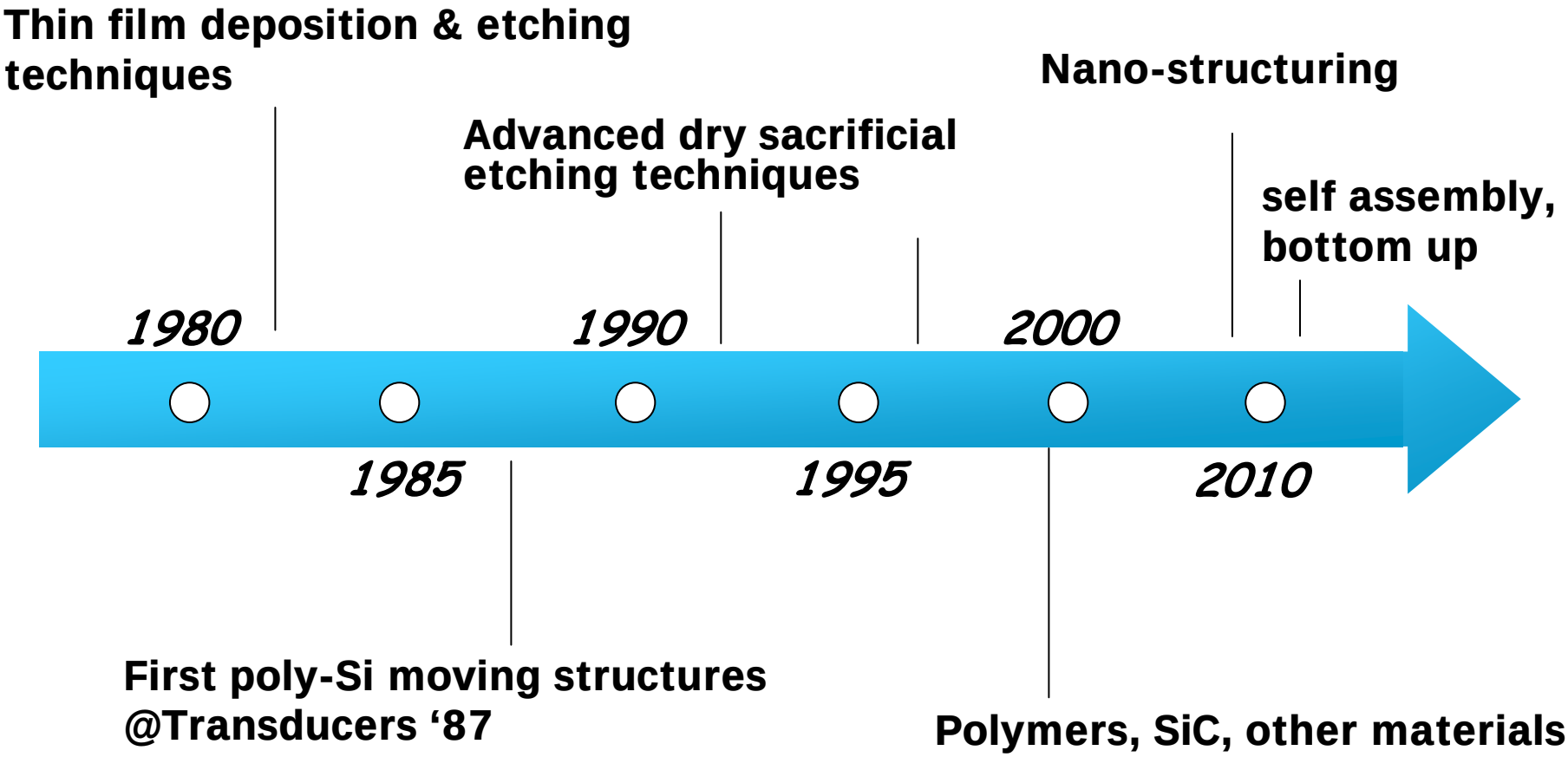




Silicon Bulk Micromachining
…>40 years of development…..

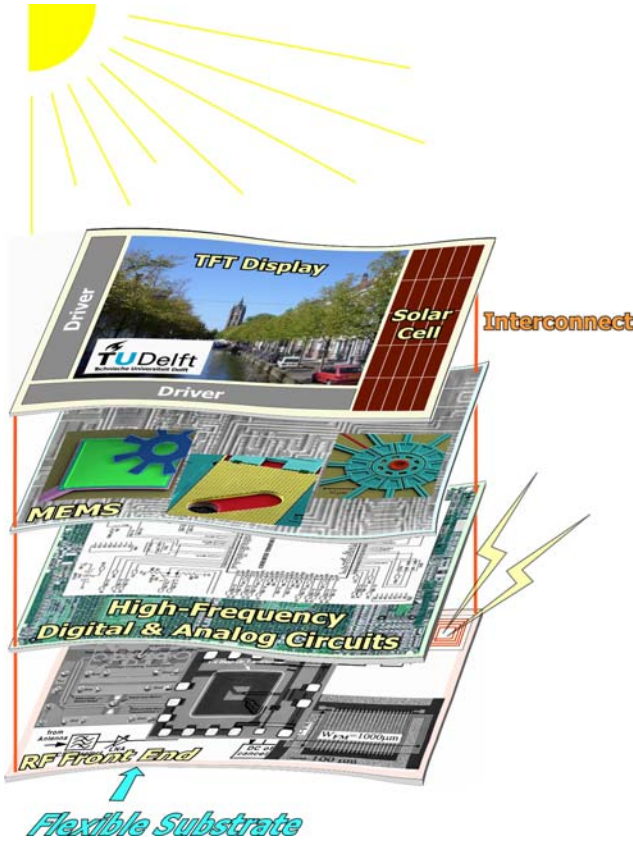


Silicon Surface Micromachining
…>25 years of development…..



Technology Trends

- **Top down & Bottom up**
  - **BMM & SMM ➔”merge”**
- **Functional multi-layers**
  - **hetereogenous intgration**
- **System approach**
- **Harsh environment**
  - **SiC, Diamond, Graphene**
- **Biocompatible**
- **“Flexible”**

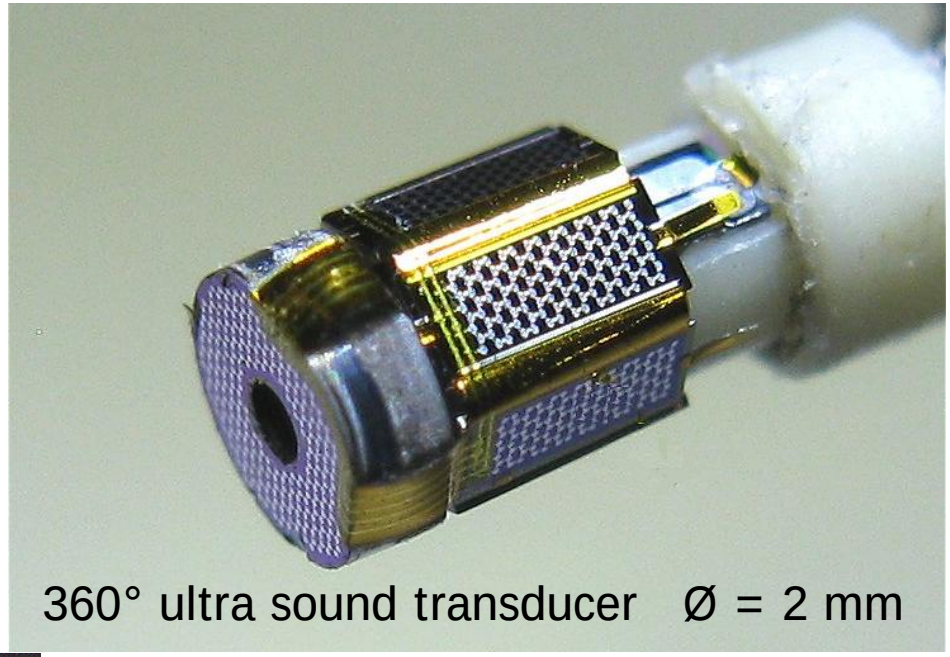


An example: “Living Chips”

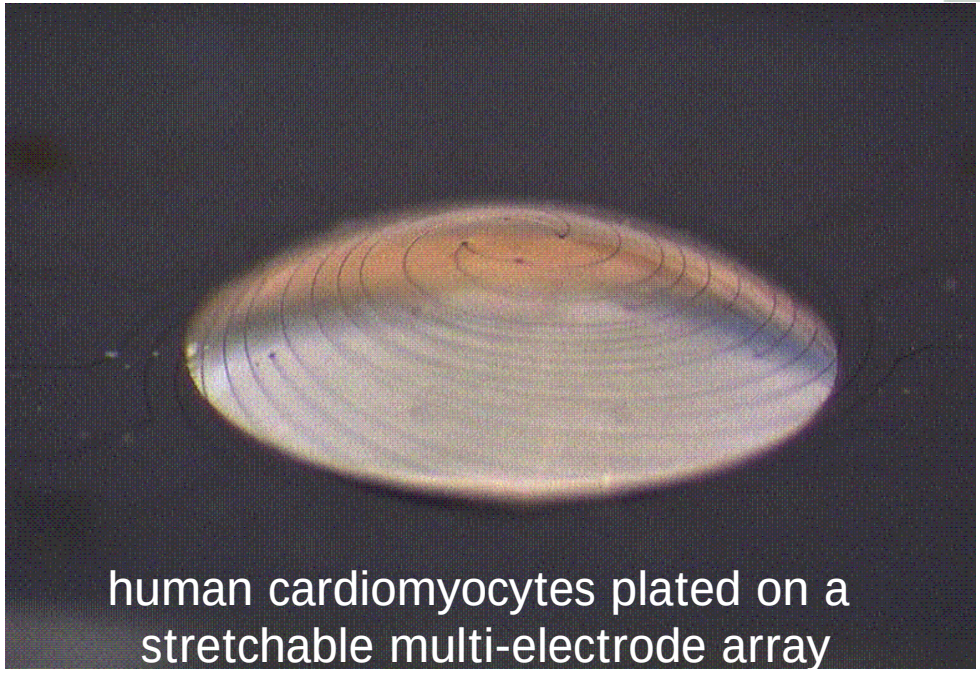
Chips for the Living

bring electronics and sensors
to the tip of catheters and guidewires

cooperations:
Philips Medical Systems, St Jude Medical,
BmechE (3mE), Cardiovascular Biomechanics (TU/e)



360° ultra sound transducer Ø = 2 mm



human cardiomyocytes plated on a stretchable multi-electrode array

Life on a Chip

integration of living cells on chips
as a functional layer

cooperations:
prof. C. Mummery (LUMC), Pluriomics (spin-off),
Philips Research

prof. Ronald Dekker
TUD & Philips

Design

Design of Device/Component

(package/system considerations)

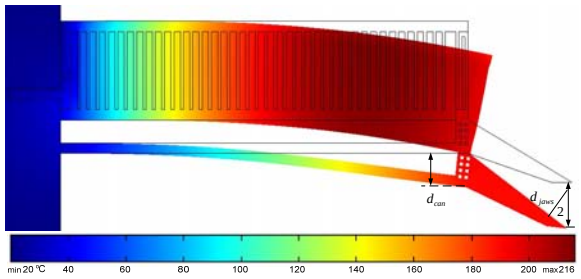
Modeling/Simulation:

specific features, several tools available

New device/new process

New device/existing process

Existing device/new process



Design Rules

"Design rules" for basic MEMS components
[mechanical structures and/or building blocks]

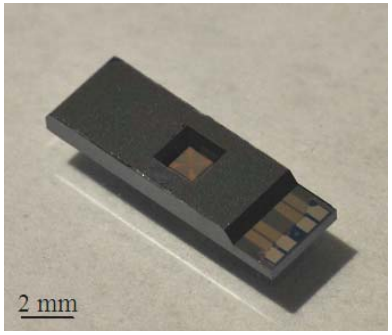
Membranes
Cantilevers
Beams
Comb Drives
Piezoresistors, Electrodes, ...

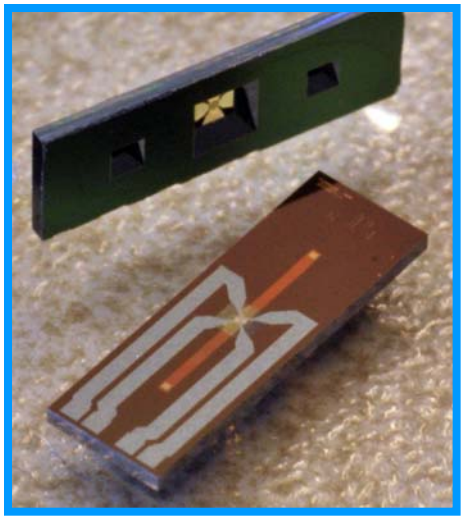
Possible/necessary?

Strong link to technology & application

System Integration

- Monolithic vs Hybrid
- Wafer level
- Packaging level



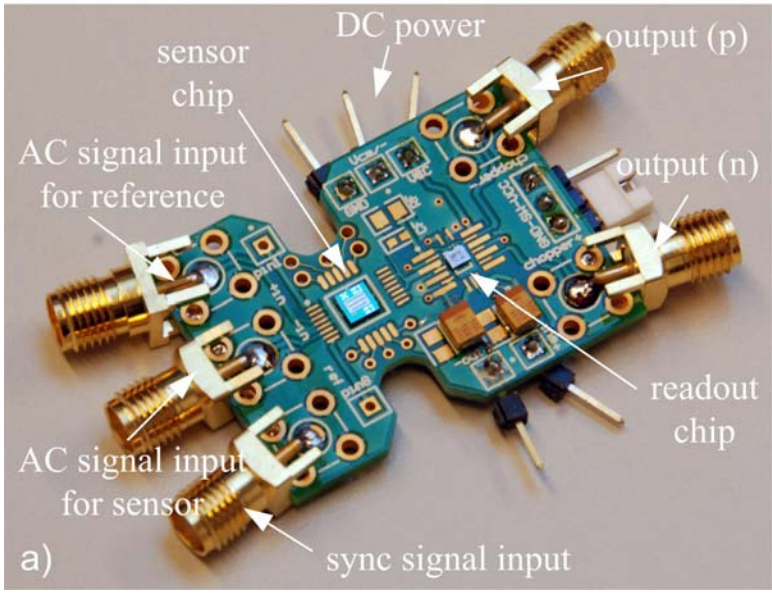


System integration:

➔ controls performance,

➔ >70% costs,

➔ >90% size and reliability

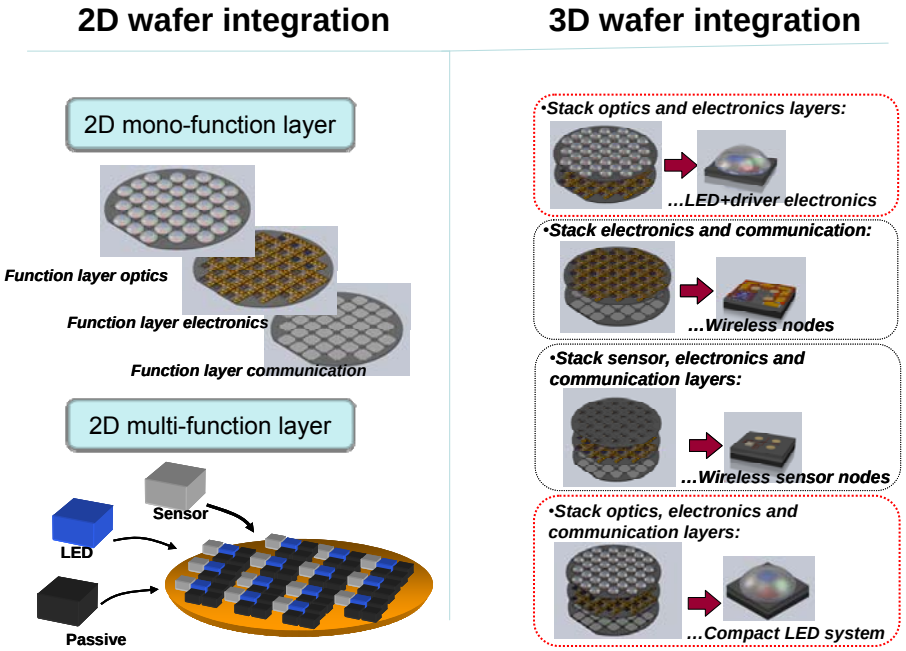


Wafer Level Integration

Wafer level, 3D, multi-function, smart and cost effective heterogeneous integration processes and technologies

Research subjects

- Polymer interposer technologies
- Hybrid interposer stacking for multi-function wafers
- 3D processes
- Design for X (reliability, yield, testability, cost, etc.)



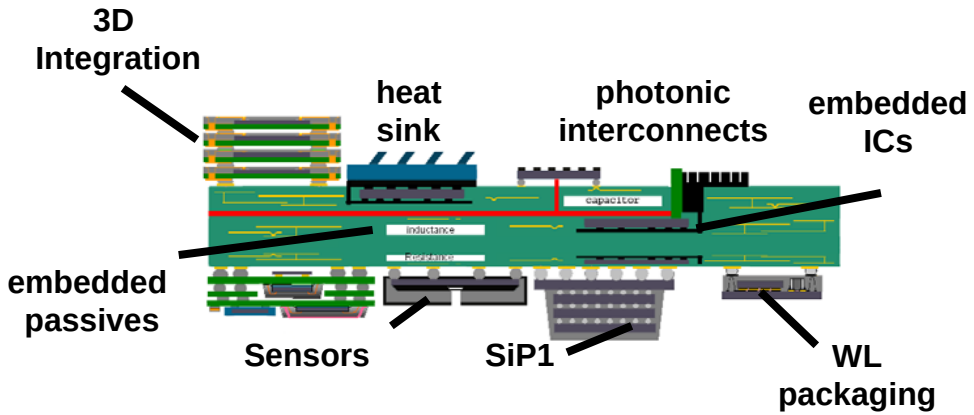
G.Q.Zhang, TUD & Philips

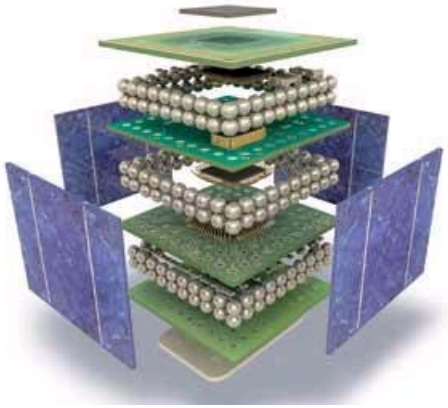
Package Level Integration (SiP)

Package level, 3D, multi-function, smart and cost effective heterogeneous integration processes and technologies

Research subjects

- Package architecture
- Integration processes for multi-functional modules & devices
- 3D and novel interconnect
- Design for X (reliability, yield, testability, green, etc.)
- Cost model





G.Q.Zhang, TUD & Philips

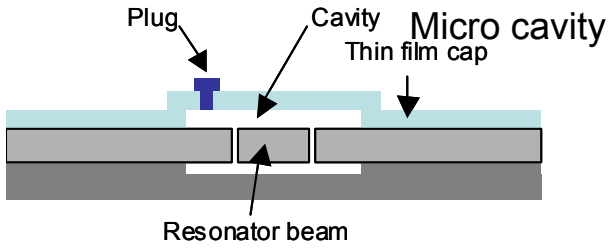
An example

- Thin film encapsulation for MEMS
  - Design for reliability
  - Mechanical design and modeling
  - IC compatible fabrication process
  - “pre-packaging” at wafer level

Design for Reliability of MEMS Packages

Motivations

- **During MEMS design assembly and packaging influences on micro cavities should be considered as they can threat the product or influence the performance.**



Objectives

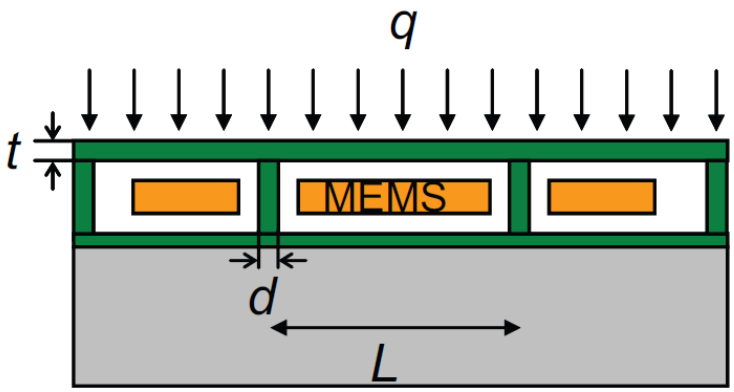
- **Develop predictive models to estimate weak spots in the design**
- **Find common failure modes of micro cavities**
  - **during manufacturing**
  - **during lifetime**

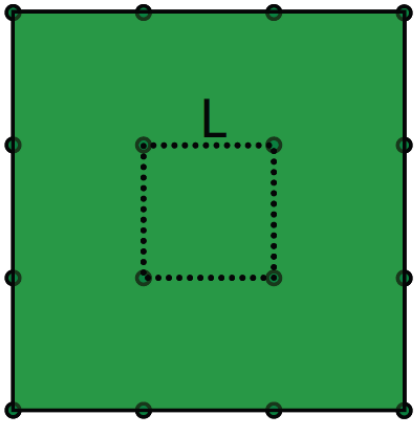
Approach

- **Combined experimental – modeling approach**
  - **Experimental determination of failure mode**
  - **Modeling of failure**
  - **Proposal of geometry / process adjustments**

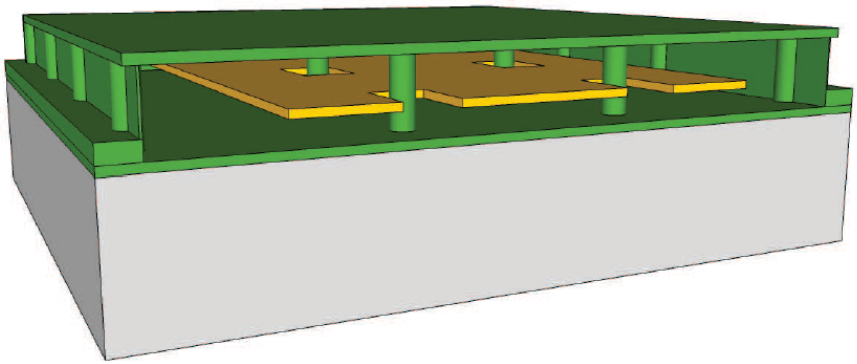
J.Zaal et al., TUDelft

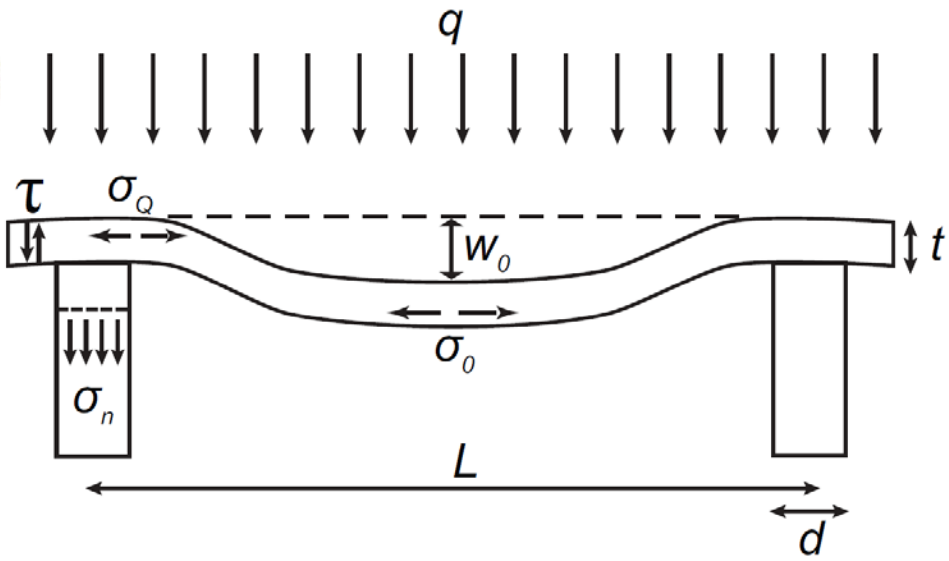
Mechanical Design of Thin Film Encapsulation





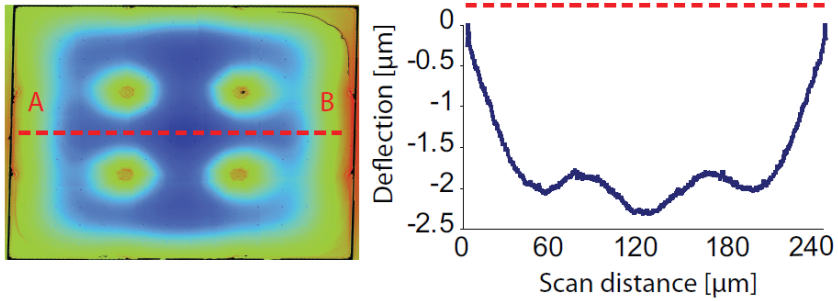
Thin-film package geometry consisting of a square plate with supporting columns

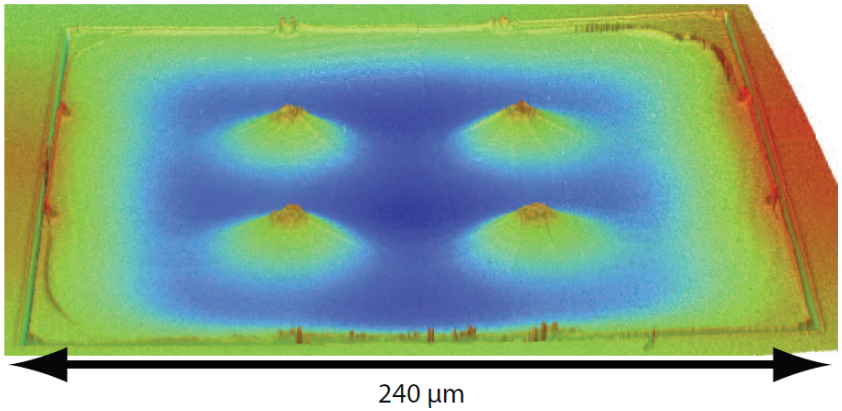




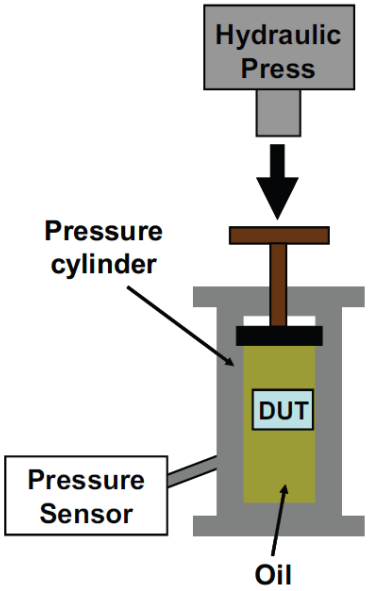
F.Santagata et al., TUDelft

Stress components and the deflection of the capping layer taken into account in the mechanical model.

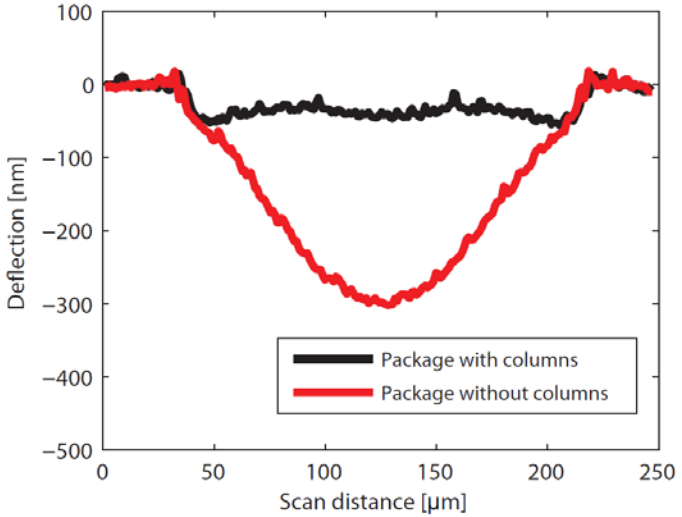




3D imaging of the packages by optical profilometry after loading. The cap deflects and is stuck to the bottom of the package.

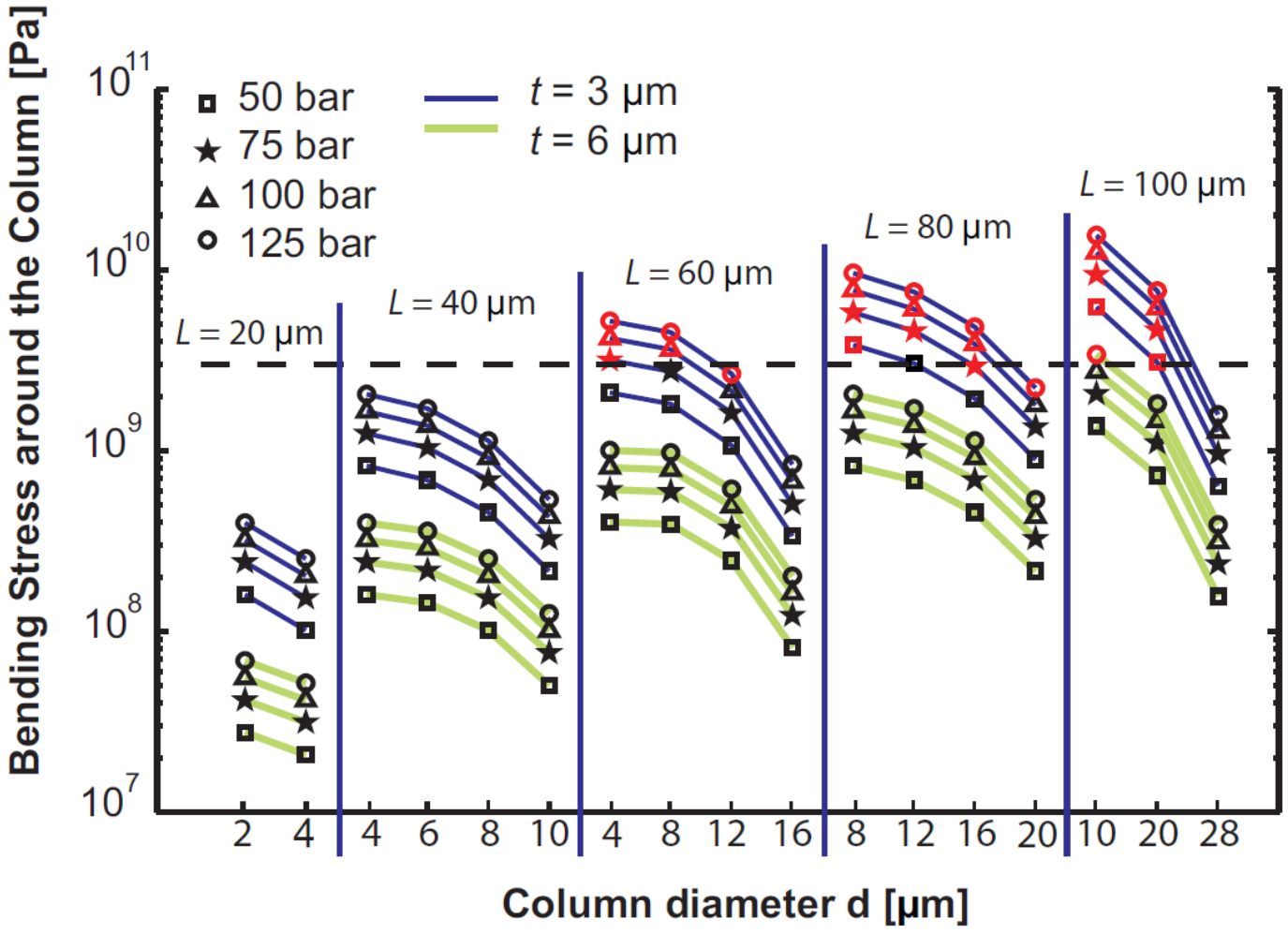


Sketch of the setup for the pressure test



Deflection under 1 bar. Comparison between two square packages (180 µm side length) with and without columns (4 µm diameter). The deflection of the package with no columns is too large for many applications.

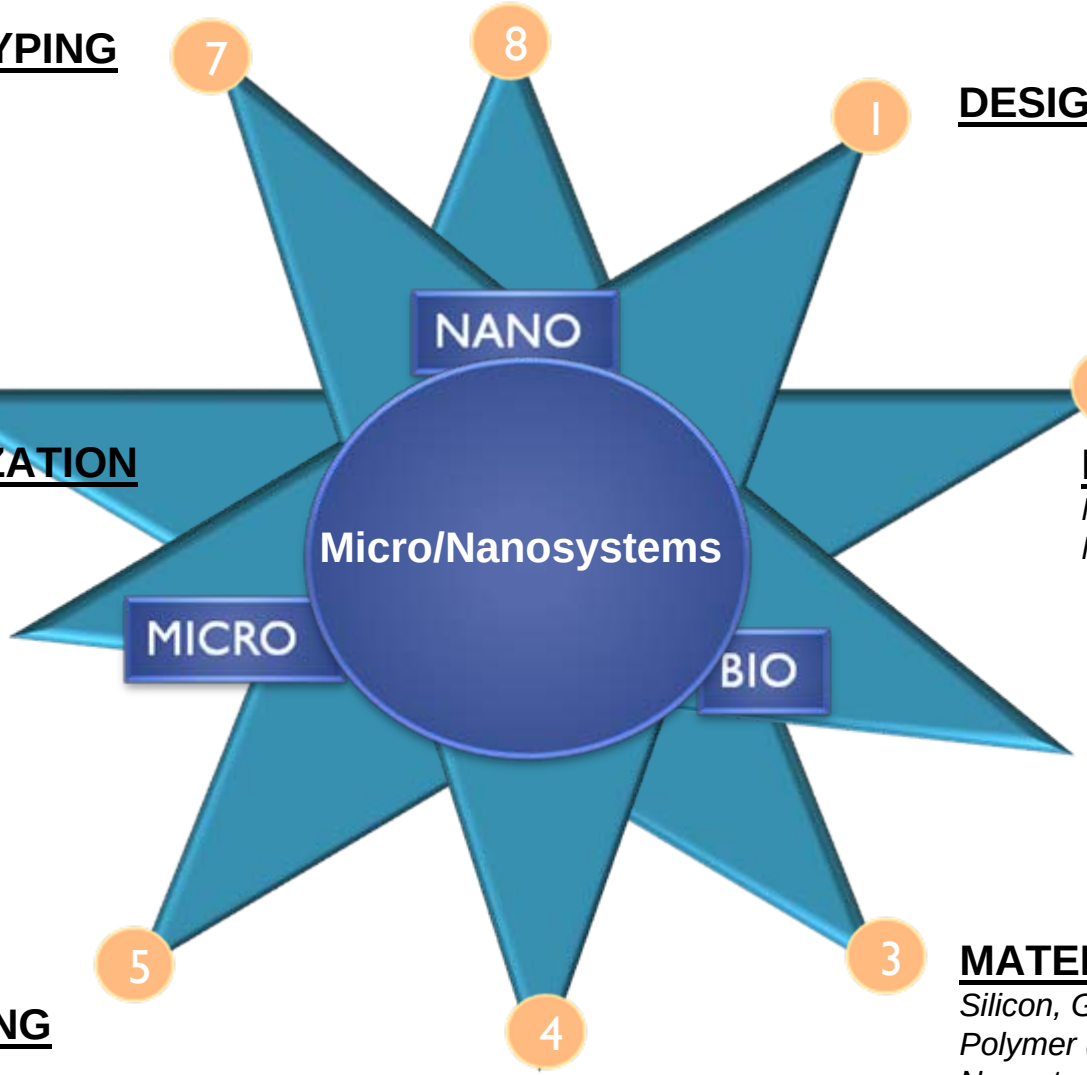
Hydrostatic pressure test



Not broken | Broken

The red markers represent the broken packages.

From idea to Product



Adapted from D'Amico et al, 2011

Challenges

- Miniaturization: size matters
- Integration: manage complexity
- New technologies: acceptance
- Autonomous: long life
- New applications: more functionality

Challenges

- Miniaturization:
  - Technology advances
  - Design tools
  - Simulation programs

Challenges

- Integration: manage complexity
  - Monolithic vs heterogeneous
  - Performance vs cost vs volume

➔“user” wants a system!

Challenges

- New technologies
  - Needed to integrate new functionalities
  - Reliability
  - “multiple” applicability

Challenges

- Design ⇔ Technology
  - Path to “generic” process(es)/standardization
  - Possibility and impossibility of a library
- Integration & Reliability
- Sub-domains:
  - Automotive
  - Bio/medical
  - CE and Mobile

Concluding Remarks

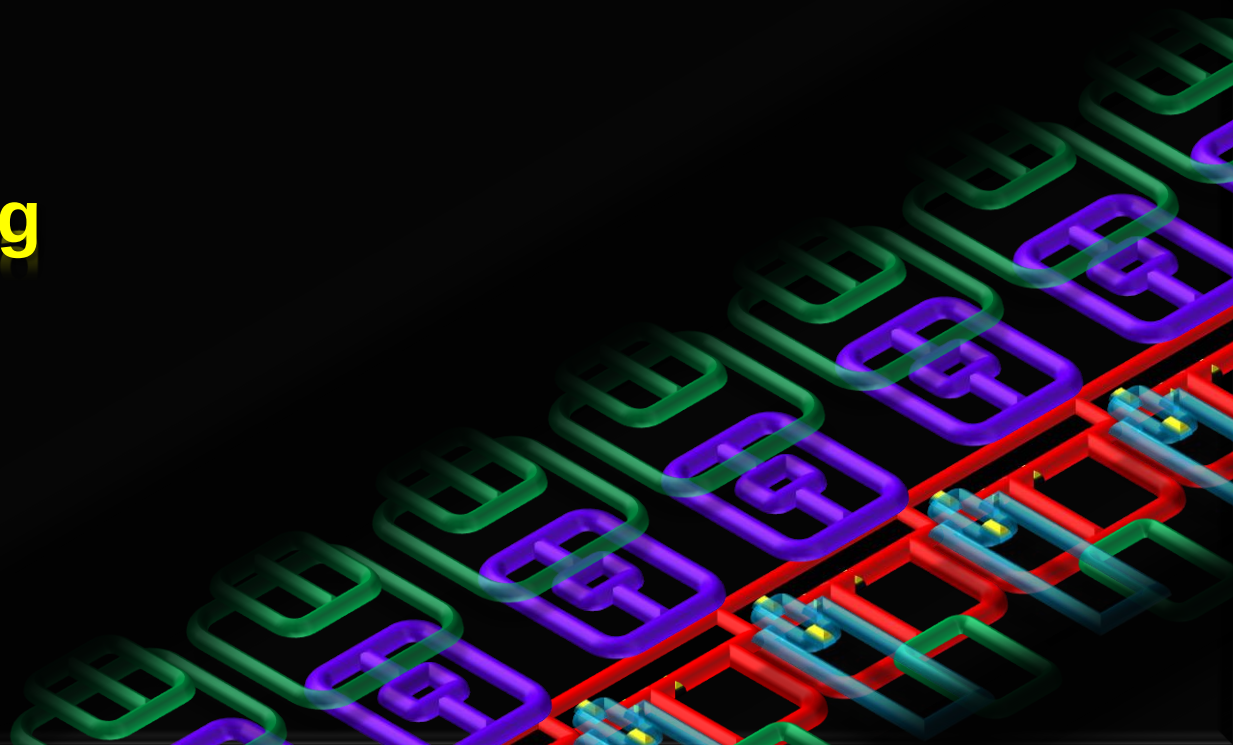
- **MEMS** development has come through fundamental research with an eye for the application.
- **Micro and nano technologies** advances offer many opportunities for improved performance and reduced costs in a wide range of industries.
- Emphasis is on improved functionality and reducing the size of the **system** rather than reduced size of individual components.
- **Scaling** of components should only be done where functional benefits can be obtained.
- Many applications require a **multi-disciplinary** approach
- **Health**, **Environment** and **Energy**: main application area

Solid State Quantum Computing

Jaw-Shen Tsai
NEC/Riken

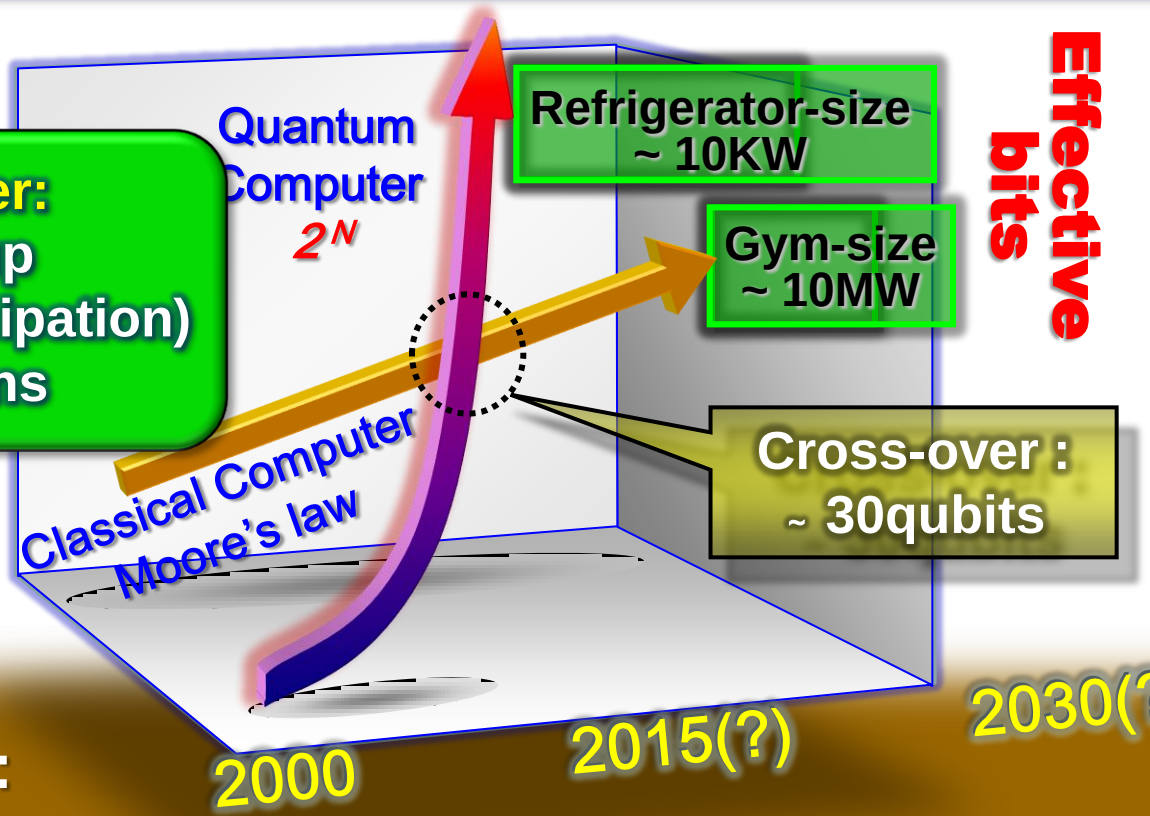
NANO-TEC, Athens, 10/13/2011

Decoherence
Integration Scaling

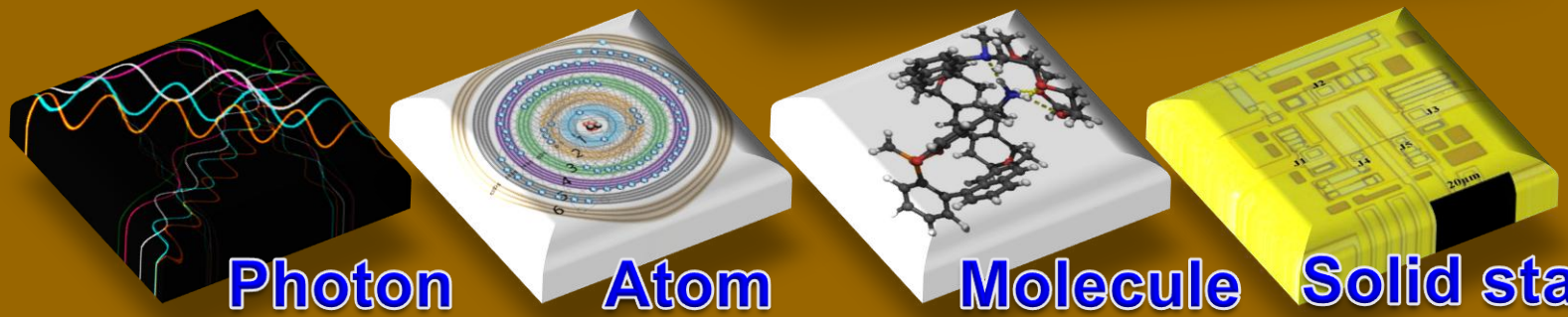


New Paradigm of Computing

Quantum Computer:
- Exponential speed up
- Low energy (no dissipation)
- Not for all applications



Physical realizations:



TRANSMISSION

LONG LIFE, UNIFORMITY

INTEGRATION, DESIGN/CONTROL FREEDOM

What can quantum computing (QC) do?

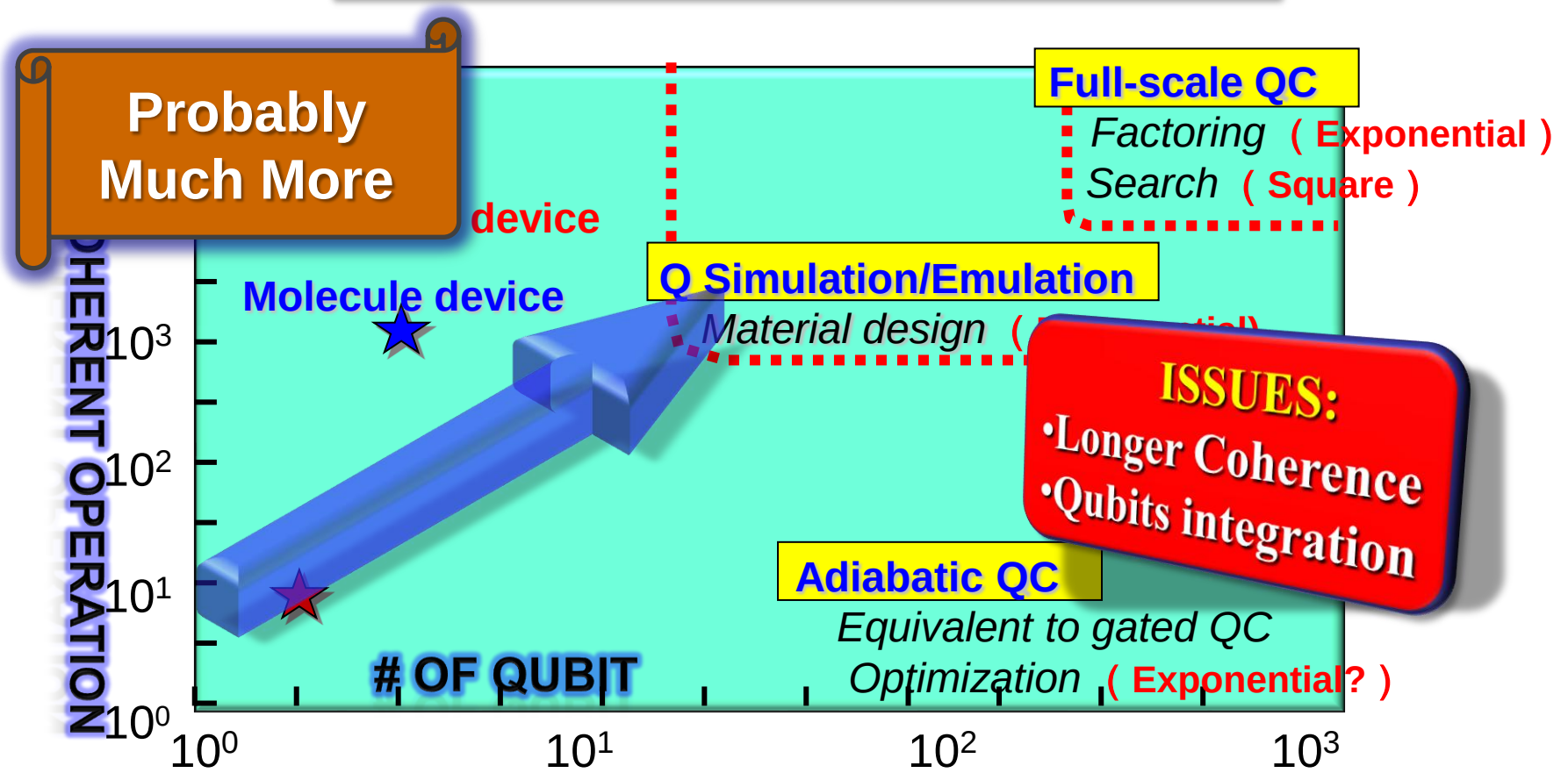
Hypothetical Quantum Computer

Breaking SSL128 (RSA1024):

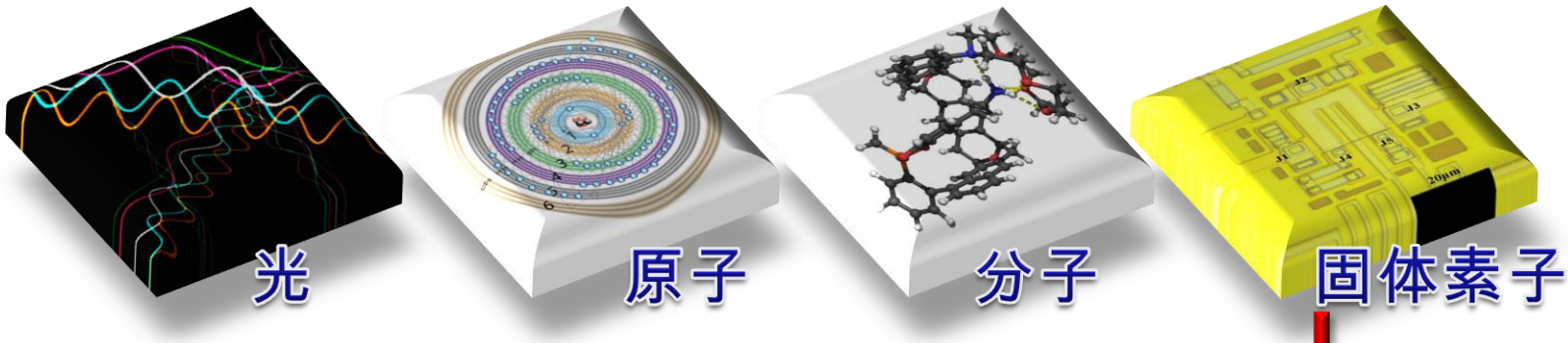
Number of qubit: 3ln(1024) X 7 (QEC) = ~ 20000 qubits

Computing time: 1024^3 X 10^4 (QEC) X 10 (connection) X GHz^{-1} = ~ 30h

C f : Supercomputer (35MW) : 3 M years



量子ビットの実現



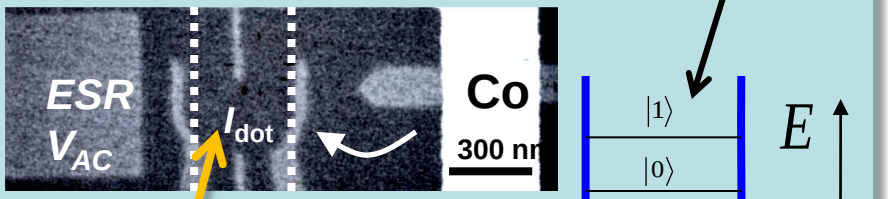
特

固体素子： 集積化、設計自由度、制

分子： 長寿命 均 送

半導体
量子ドット

超伝導体
ジョセフソン
接合



量子ドット

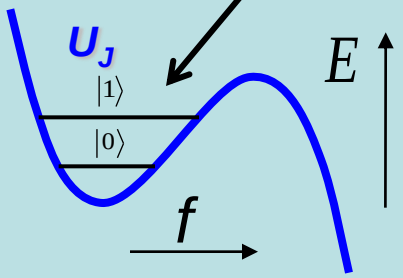
単電子状態

スピン量子ビットX

自由度： スピン、電荷数、ポーラロン

ジョセフソン接合

巨視的状態



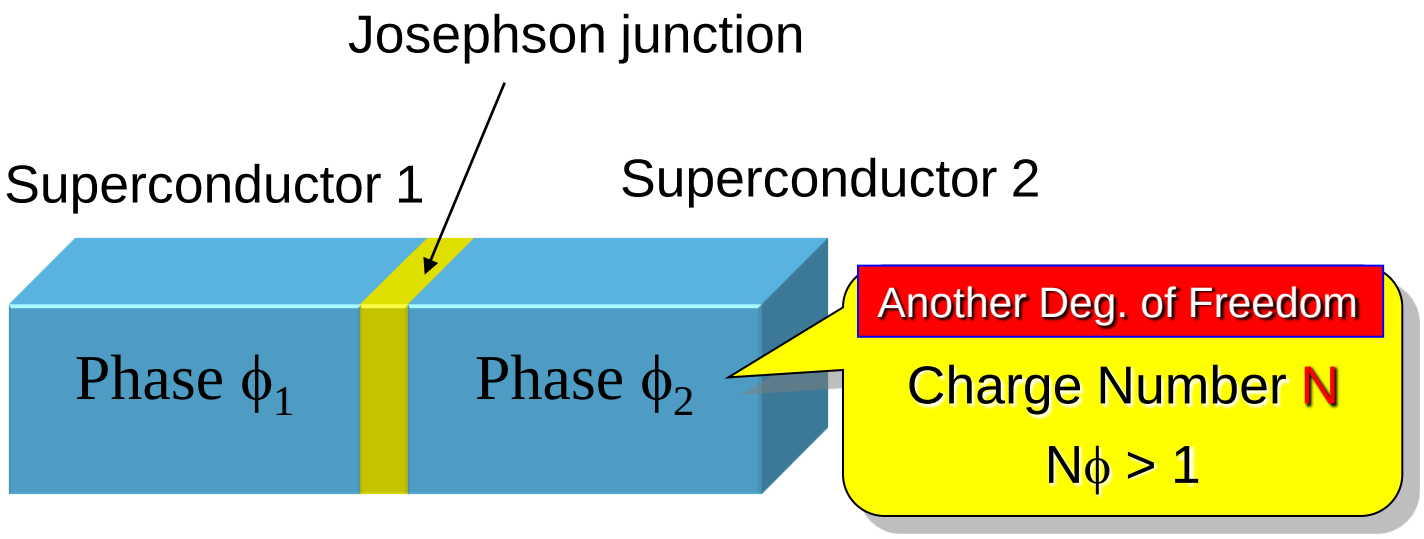
位相量子ビット

自由度： 位相差・磁束、電荷

A Macroscopic System

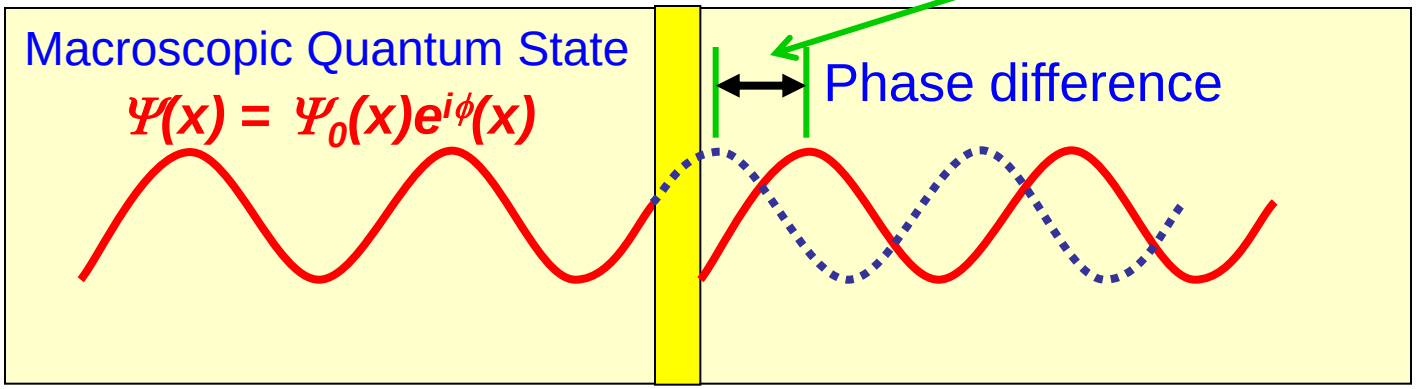
Macroscopic order parameter

$\psi(x) = \psi_0(x)e^{i\phi(x)}$



Supercurrent $\propto$ $I_0 \sin(\phi_1 - \phi_2)$

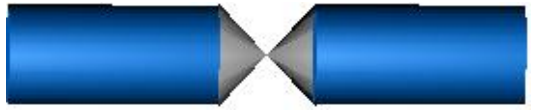
$$V = \frac{h}{2e}\frac{d\varphi}{dt}$$



Josephson junction

Secondary Macroscopic Quantum effect

Multi-energy state (cf. solitary BCS state)



$$C, \quad L_J = \frac{\Phi_0}{2\pi I_C \cos\theta}$$

Aharmonic oscillator

$$H = E_C N^2 + E_J(1-\cos\theta)$$

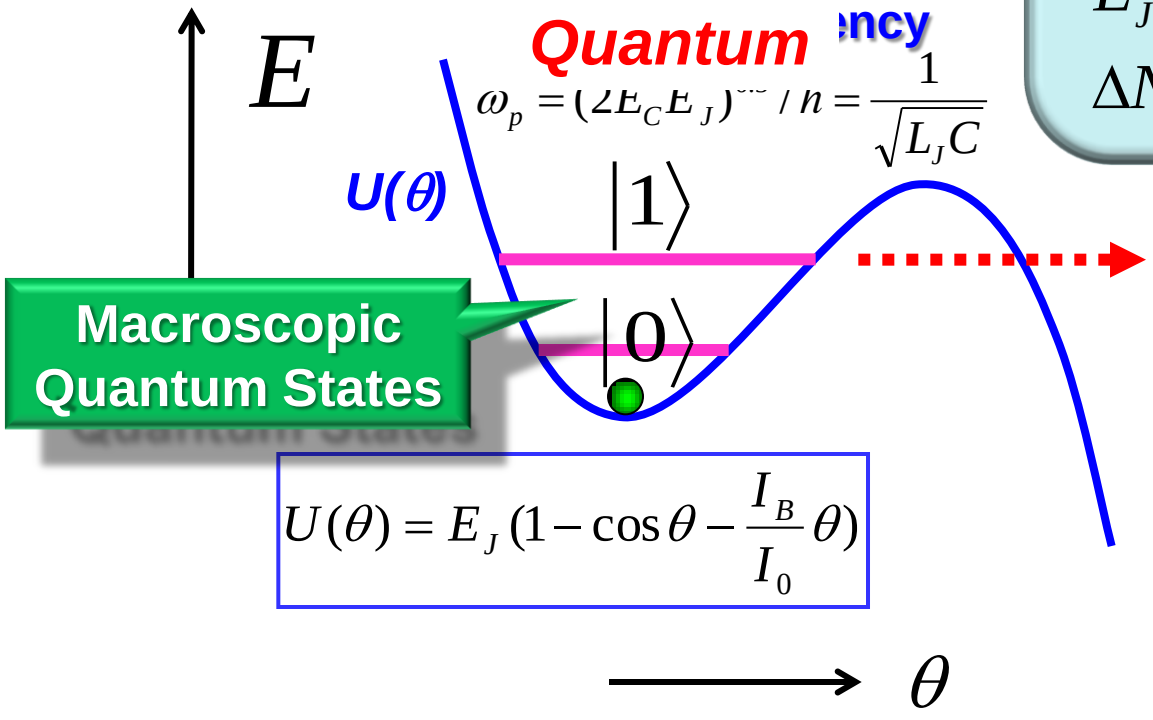
$$E_C = \frac{2e^2}{C}$$

$$E_J = I_0 \Phi_0$$

$$\Delta N \cdot \Delta\theta \geq 1/2$$

Quantum

$$\omega_p = (2E_C E_J)^{1/2} / n = \frac{1}{\sqrt{L_J C}}$$



Macroscopic Quantum States

$$U(\theta) = E_J\left(1-\cos\theta - \frac{I_B}{I_0}\theta\right)$$

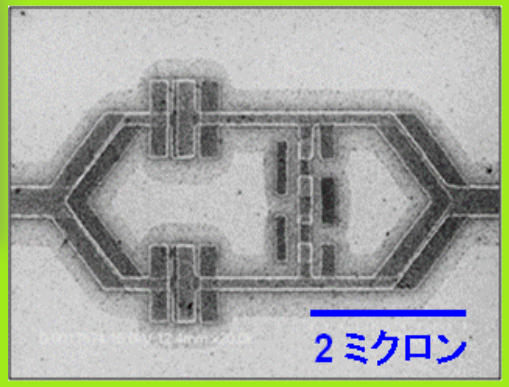
Macroscopic Tunneling

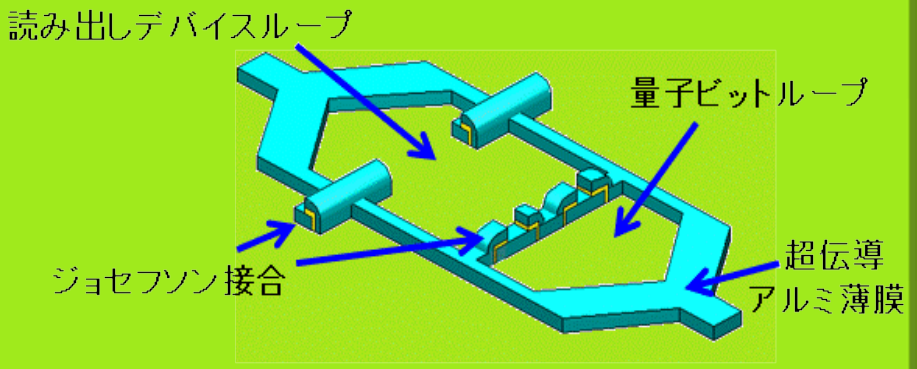
Phys. Rev. Lett. ***47****, 265 (1981)*

Level Quantization

Phys. Rev. Lett. 55, 1543 (1985)

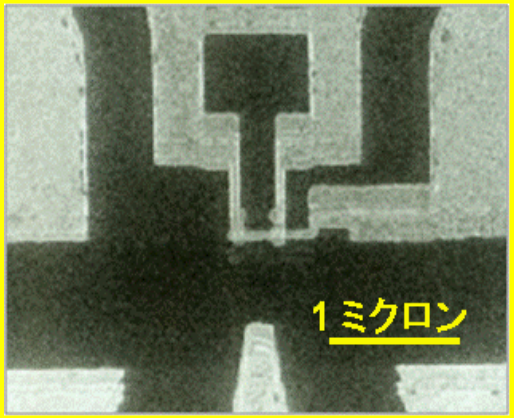
超伝導
磁束
量子ビット

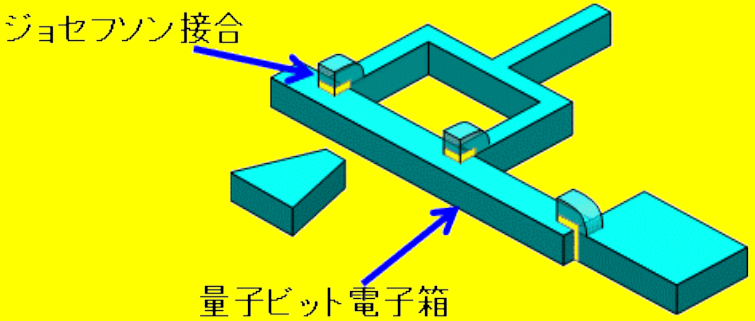




量子状態(例):
- 「0」状態: 量子ビットループに時計回りの永久電流
- 「1」状態: 量子ビットループに反時計回りの永久電流

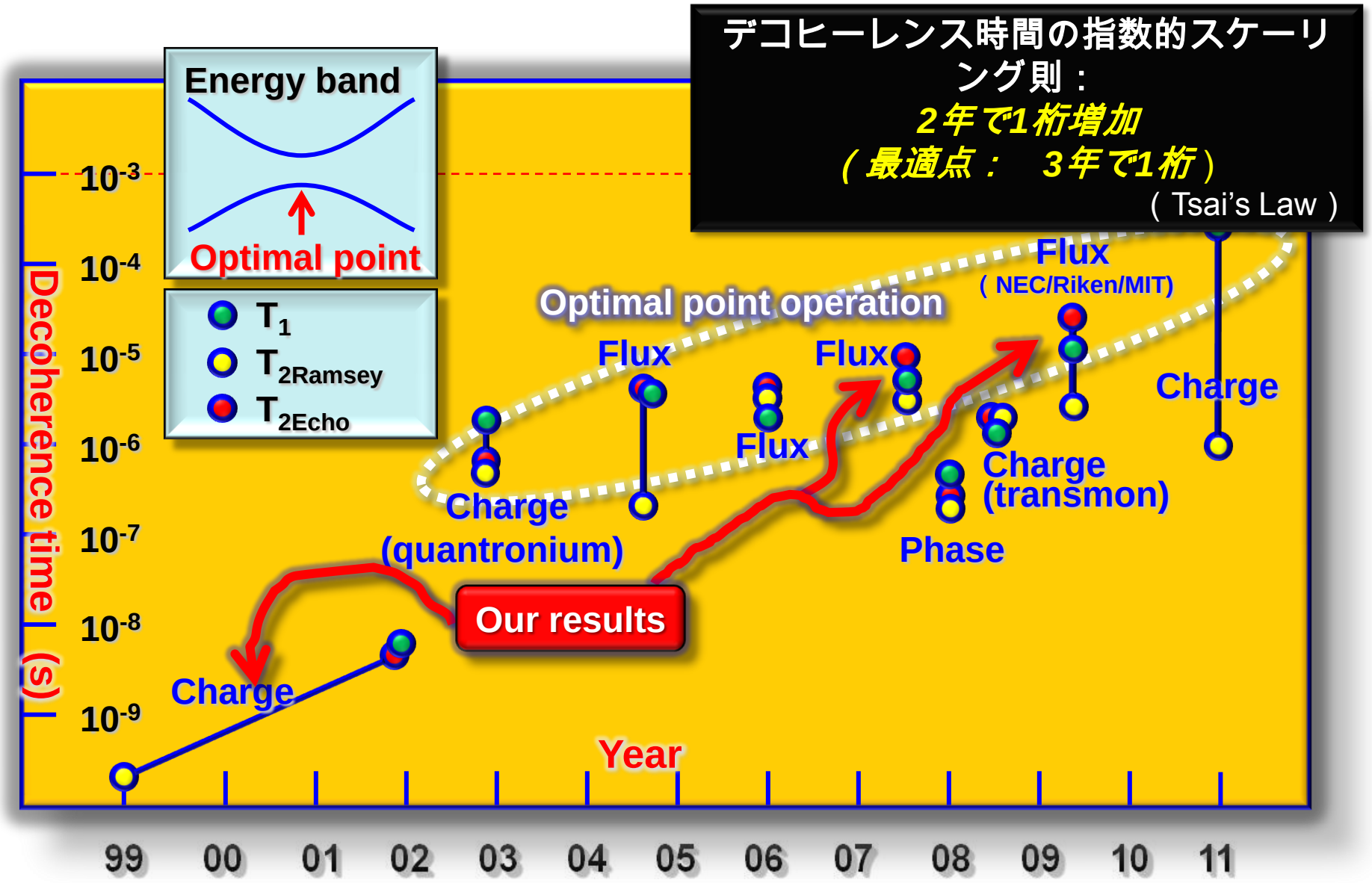
超伝導
電荷
量子ビット





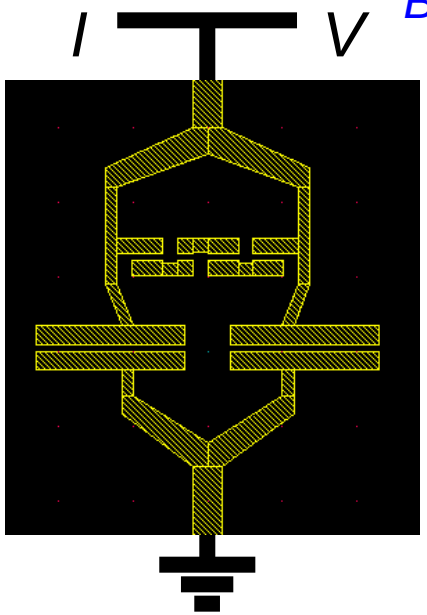
量子状態(例):
- 「0」状態: 量子ビット電子箱に余剰電子がない
- 「1」状態: 量子ビット電子箱に余剰な電子対が一つある

Progress in Decoherence time for Josephson Qubits



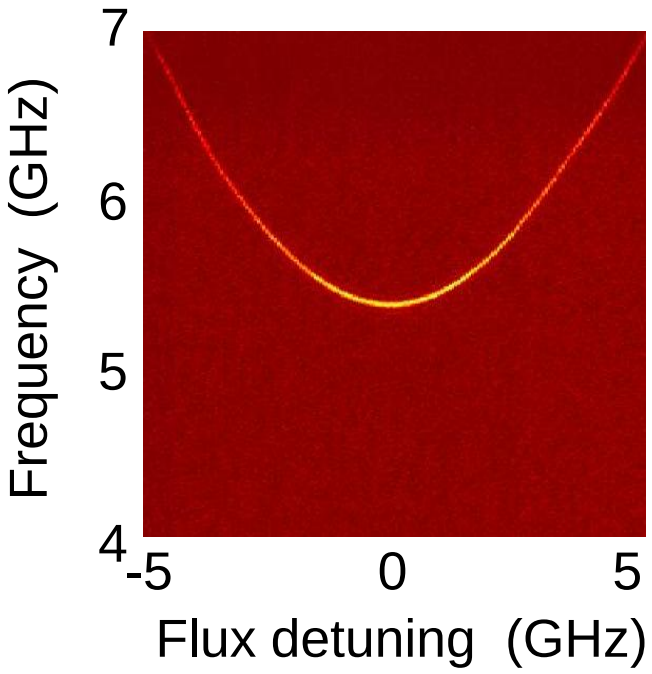
Long decoherence sample (with MIT)

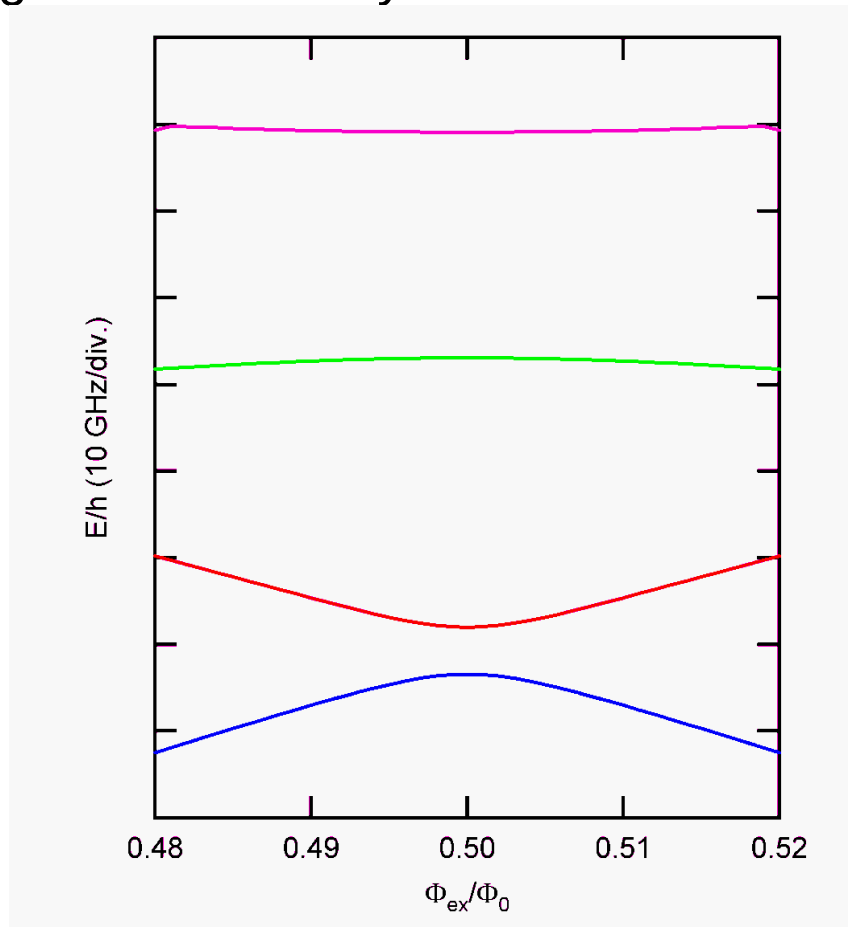
Bylander et al, **Nature Physics**, doi:10.1038/nphys1994, 2



Aluminum 4JJ flux qubit on SiO_2/Si

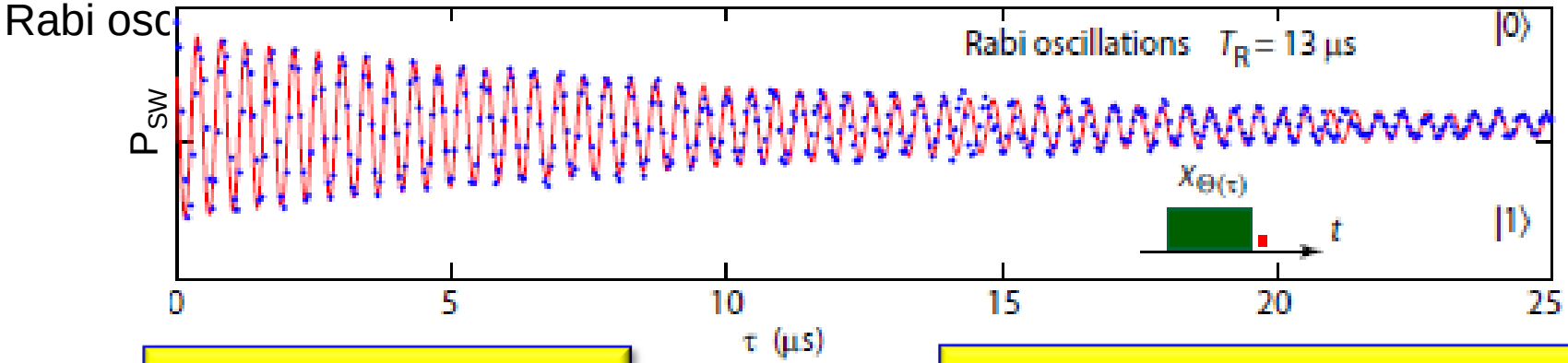
- Δ/h = 5.4 GHz
- I_P = 180 nA
- Large anharmonicity ~ 5
- E_J/h ~ 210 GHz
- E_C/h ~ 4 GHz
- α ~ 0.54



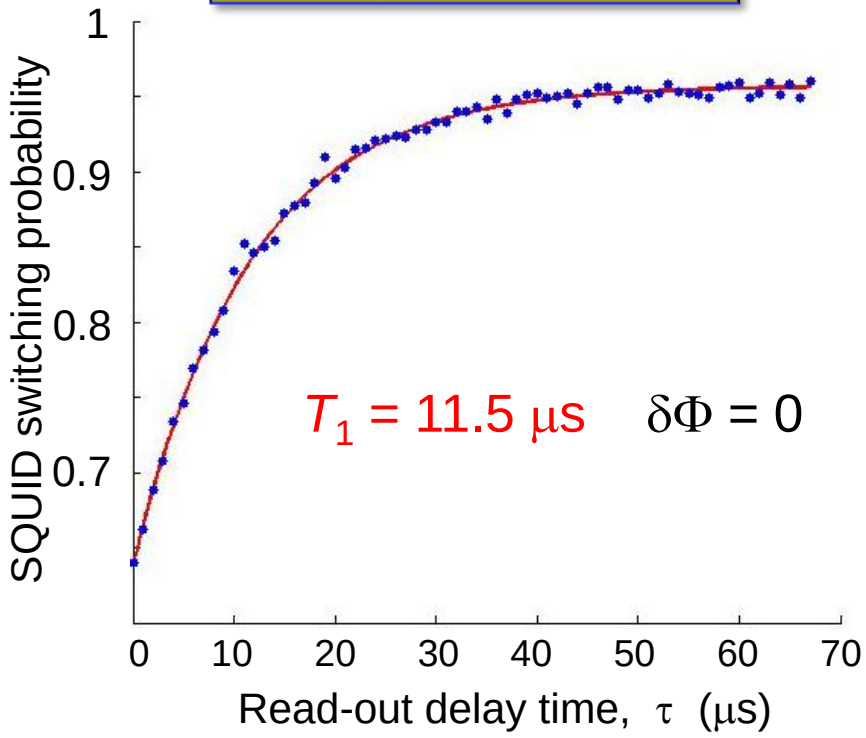


T_1 and T_2^{echo} at optimal point (with MIT)

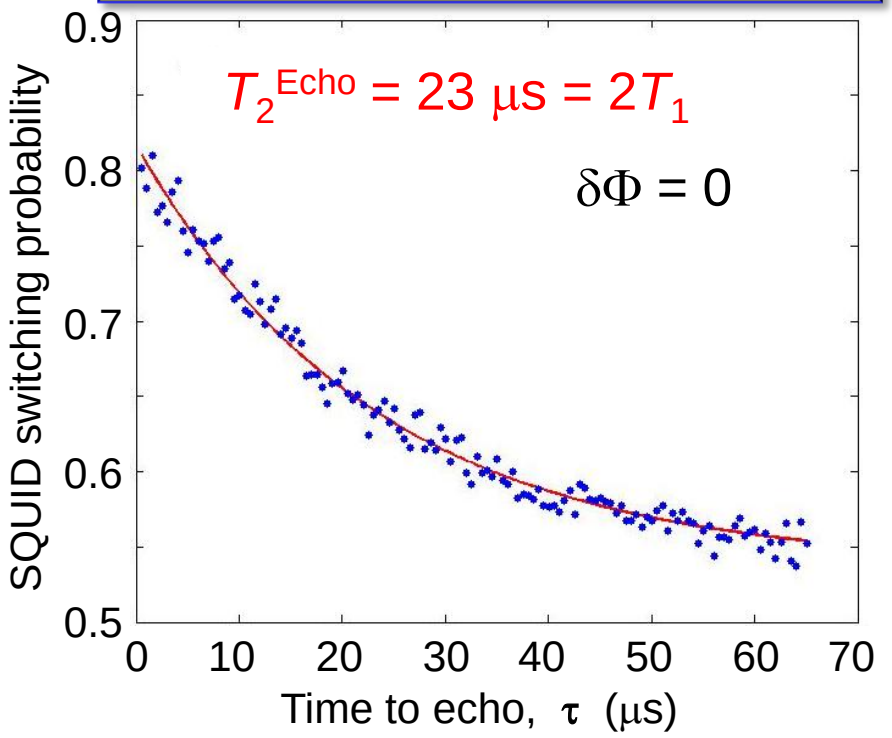
Bylander et al, **Nature Physics**, doi:10.1038/nphys1994, 2

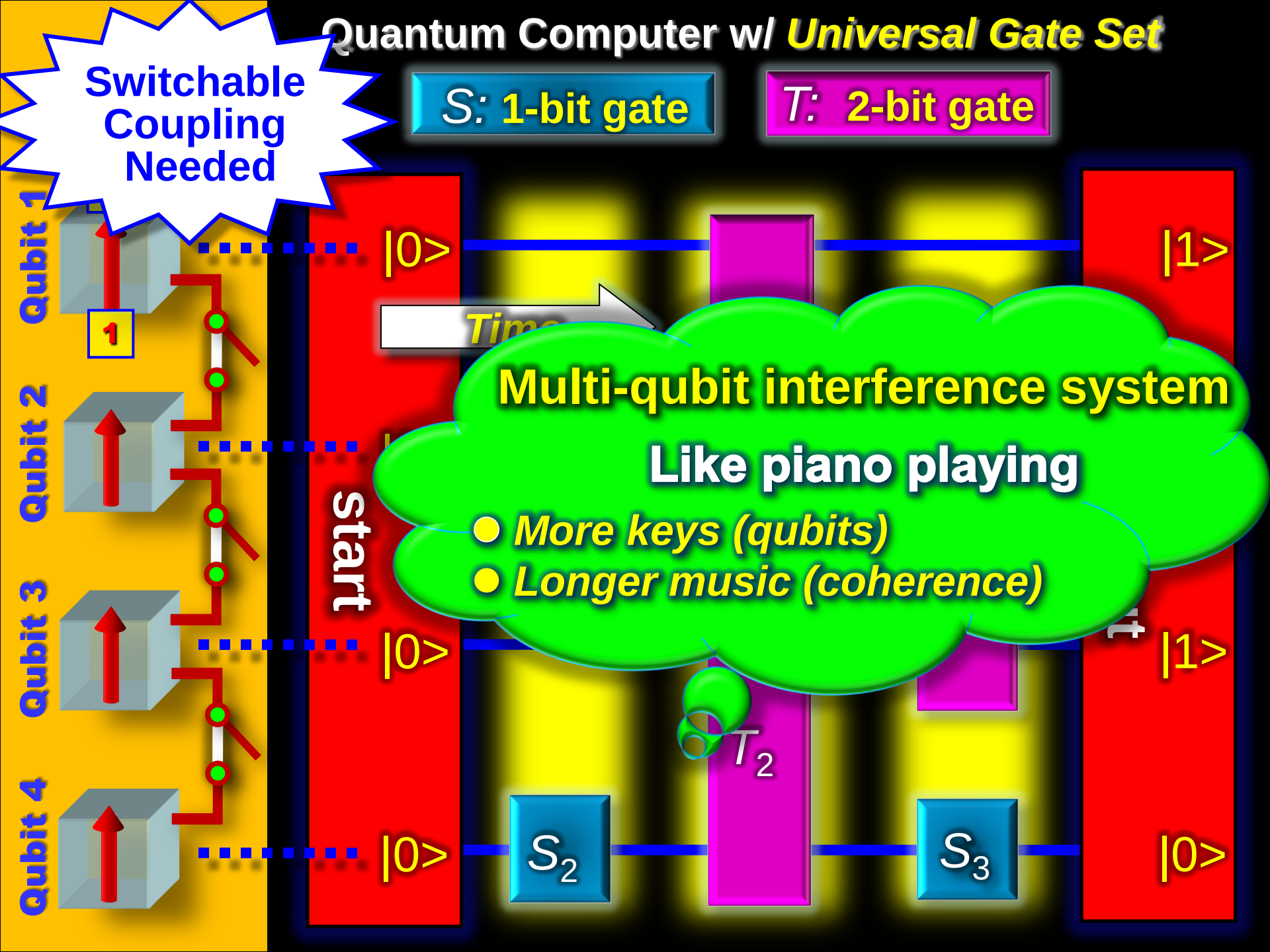


Q = $\omega_{01}T_1$ ~ 390,000



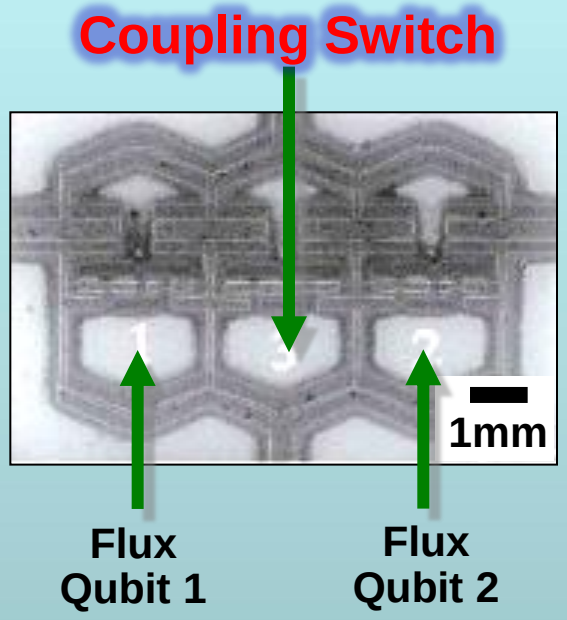
Pure dephasing time ~ 0.1ms




Quantum Computer w/ Universal Gate Set
Switchable Coupling Needed
S: 1-bit gate
T: 2-bit gate
Qubit 1
Qubit 2
Qubit 3
Qubit 4
1
start
|0>
|0>
|0>
|1>
|1>
|0>
Time
Multi-qubit interference system
Like piano playing
More keys (qubits)
Longer music (coherence)
T2
S2
S3

Progress in Scaling Up for Josephson Qubits

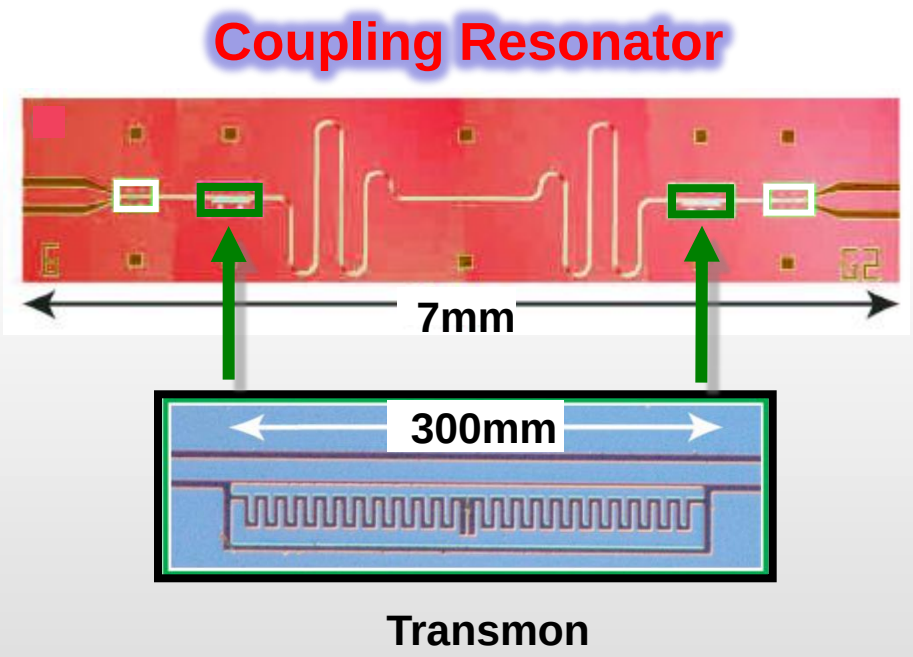
Adjustable Coupling Energy



Optimal point operation

Flux qubit:
Science, 316, 723 (2007)

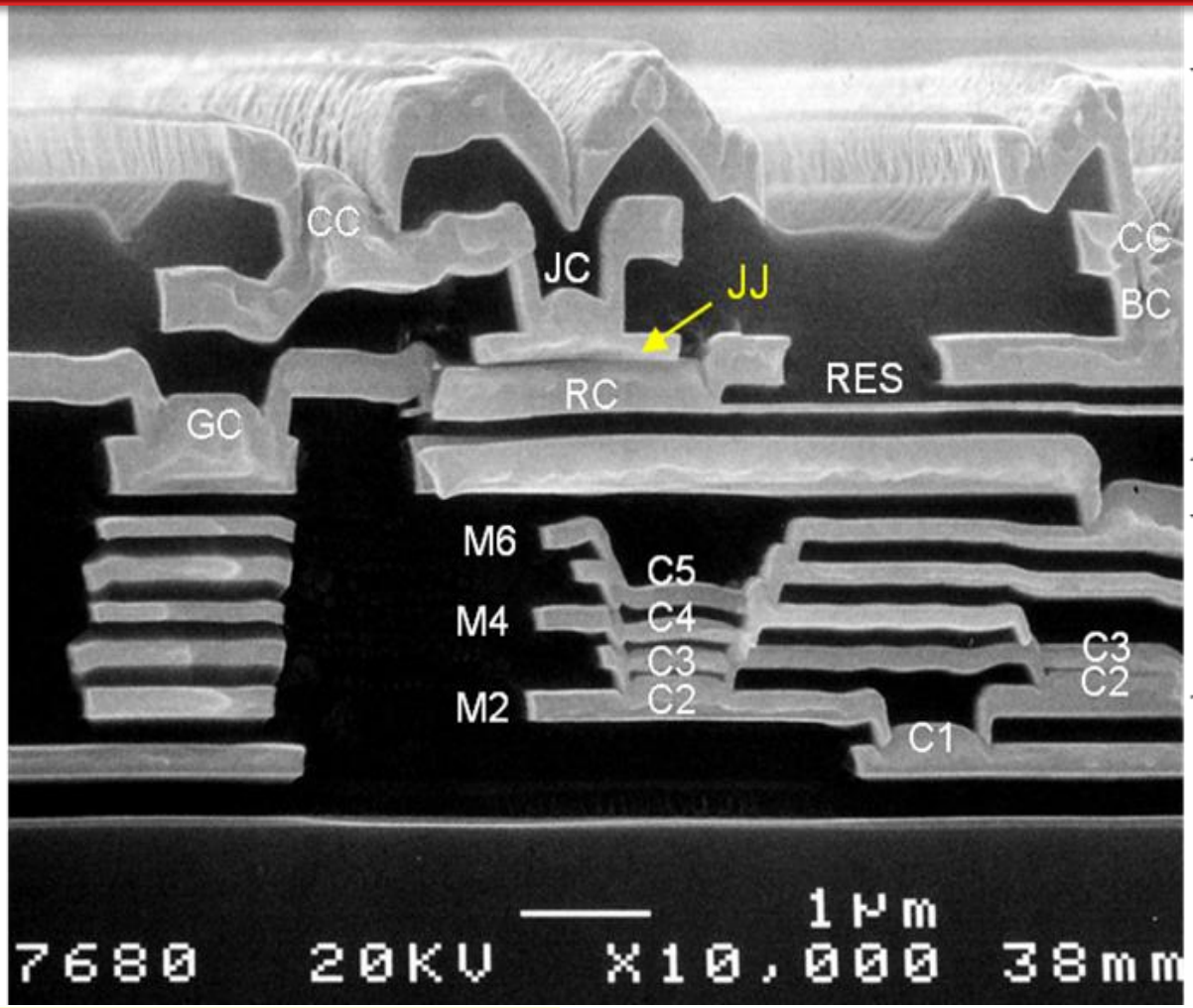
Fixed Coupling + non-adiabatic detuning



Phase qubit: Nature, 449, 438 (2007)
Charge qubit: Nature, 449, 443 (2007)

10-Nb-layer Josephson chip by the ISTEC

New effort to realize Al multi-layer qubits with EBL



The number of Nb layers: 10
J_c: 10 kA/cm^2
Sheet resistance ($R_{\square}$): 2.4 Ω

Minimum JJ size: 1×1 μm
Minimum line width: 1 μm
Stacked contact

超伝動量子万能ゲート計算 理研，NTT

ター状態計算 NTT

子計算 理研

口波光子量子計算 理研

量子ビット結合器 理研

量子バス 理研， NTT

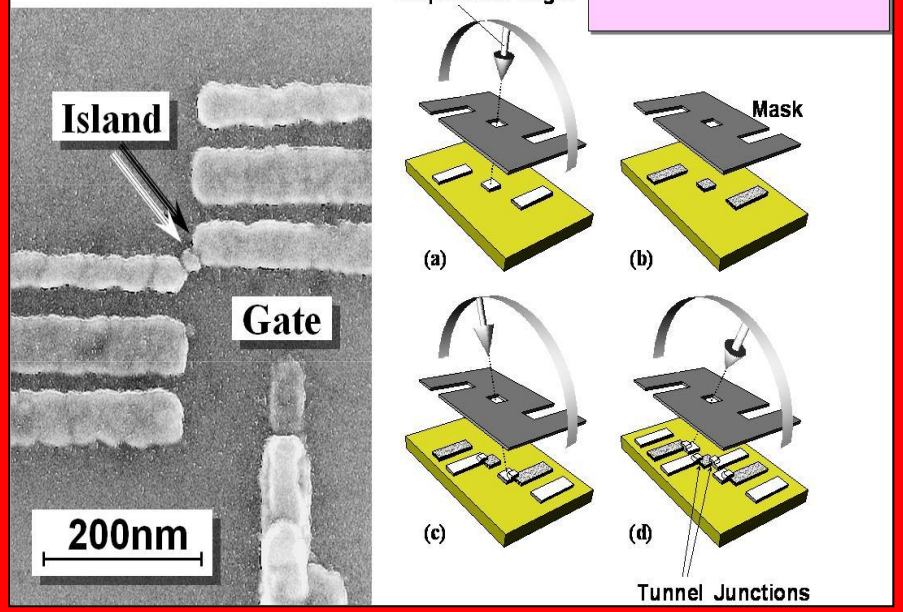
ターフェイス 東京理科大

パルサー 理研

術 理研

最先端Pjターゲッ
（4年）

現在の簡易作成法

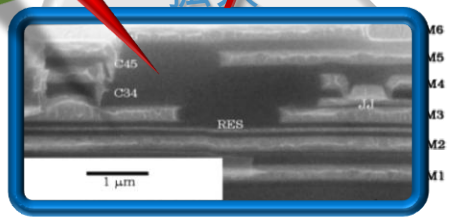


多チャンネル
マイクロ波パル
サー

光子

超伝導プロトタイプ
量子計算チップ

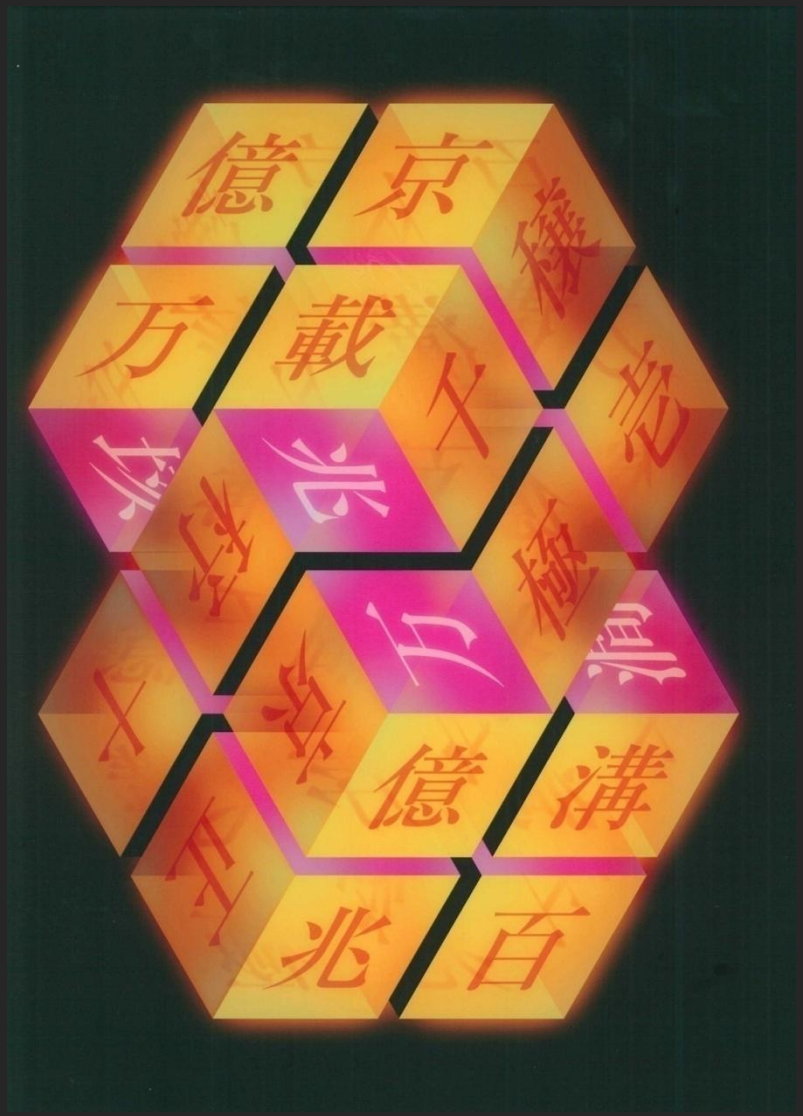
拡大



集積回路断面図(イメージ)：
多層のAl超伝導配線とAlトンネル接合より構成

量子ビット
ビット間結合
量子インターフェイス

壱： 10^{0}
十： 10^{1}
百： 10^{2}
千： 10^{3}
万： 10^{4}
憶： 10^{8}
兆： 10^{12}
京： 10^{16}
垓： 10^{20}
抒： 10^{24}
穣： 10^{28}
溝： 10^{32}
澗： 10^{36}
正： 10^{40}
載： 10^{44}
極： 10^{48} ~ 2^{150}



Thank you for your Attention

Benchmarking Spintronics

Johan Åkerman
University of Gothenburg
NanOsc AB

Outline

- What are the main drivers for Spintronics?
  - History
  - Present
- MRAM
  - Toggle MRAM
  - Spin Transfer Torque MRAM (STT-MRAM)
  - Thermally Assisted Switching MRAM (TAS-MRAM)
  - Thermally Assisted STT-MRAM (TAS+STT-MRAM)
  - Thermagnonic STT-MRAM
- Spin Torque Oscillators
- Spin Torque Microwave Detectors

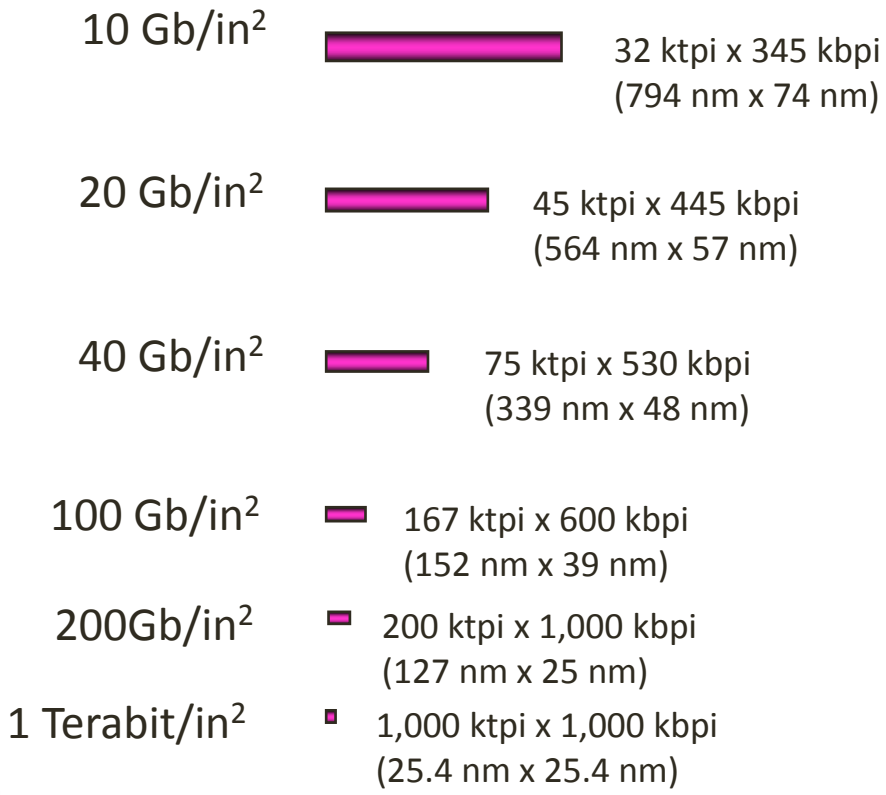
NANO-TEC

Historic Drivers for Spintronics

- Historic strong ”pull” from HDD Industry
  - Read heads – the main driver
    - Anisotropic Magnetoresistance
    - Made much more sensitive by GMR/TMR
  - Write heads – still an electromagnet
    - Concept of Microwave Assisted Magnetic Recording
    - Heat Assisted Magnetic Recording – flirting with nanoplasmonics
  - Media – benefits from spintronic read head development
    - Synthetic Antiferromagnet media – RKKY coupling

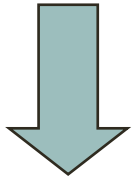
Bit size and Reader technologies

Areal Density vs. Magnetic Bit Sizes

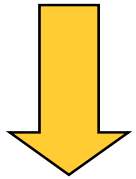


Experimental MR Effect

AMR (~2%)



GMR (~20 %)



TMR (20-230%)

CPP-GMR (up to 50%)

High MR ratio translates to High Signal– to–Noise ratio

Historic Drivers for Spintronics

- Historic strong ”pull” from HDD Industry
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  - Write heads – still an electromagnet
  - Media – benefits from spintronic read head development
- HDD companies + others starting MRAM research in 1995
  - Conventional field switched MRAM
  - DARPA driven

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  - Write heads – still an electromagnet
  - Media – benefits from spintronic read head development
- HDD companies + others starting MRAM research in 1995
  - Conventional field switched MRAM
  - DARPA driven
- MRAM pull – Half-Select Problem, Read Signal
  - Toggle MRAM solves Half-Select Problem (2001)
  - Toggle Patent out in 2004 – The end of conventional MRAM
  - MgO Tunneling Barrier out in 2004 – Almost the end of AlOx
  - 4 Mb Toggle MRAM goes commerical in 2006 – lukewarm response.
  - Toggle MRAM does not scale very well

Historic Drivers for Spintronics

- Parallel development: Academic ”Push” for Spintronics
  - Spin Transfer Torque (STT) – John Slonczewski, Luc Berger (1996)
  - Spin Torque Oscillator – John Slonczewski (1999)
  - STT driven domain walls
  - Spin Injection
  - Spin Hall Effect
  - Spin Pumping
  - Inverse Spin Hall Effect
  - Spin Seebeck Effect
  - Spin Injection using Spin Pumping
  - Spin Peltier Element
  - Thermally Driven STT, Thermo-magnonic STT
  - ”Spin Caloritronics”, ”Magnonics”

Present Drivers for Spintronics

- Limit power consumption

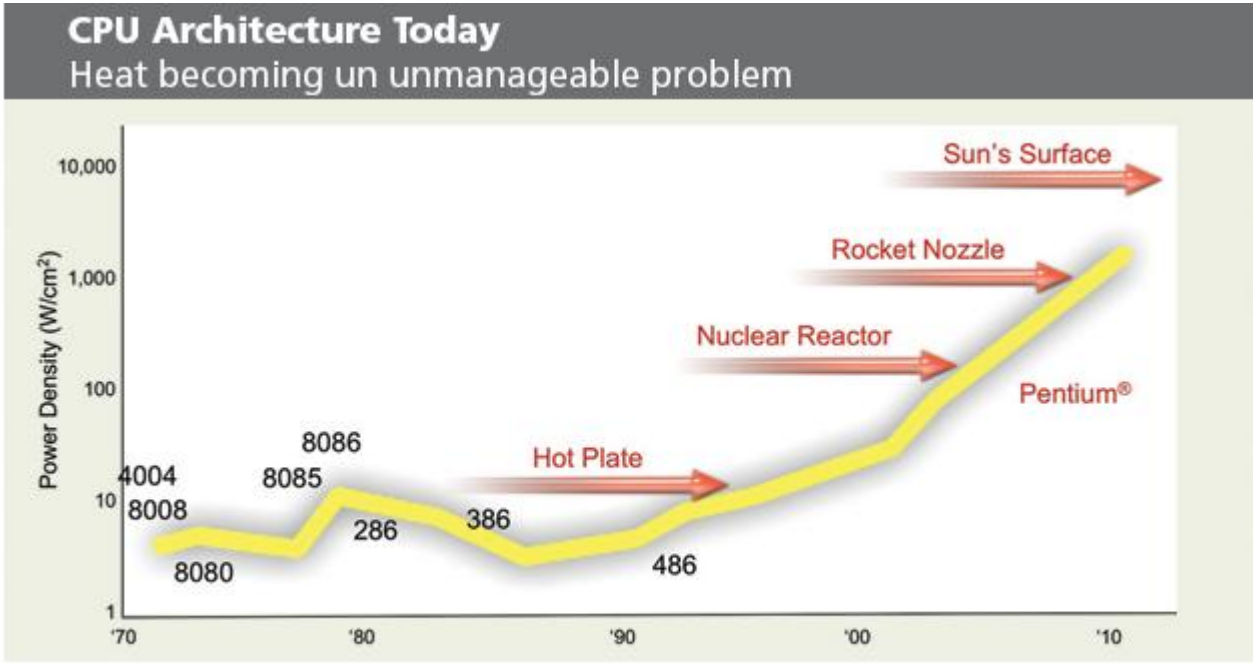
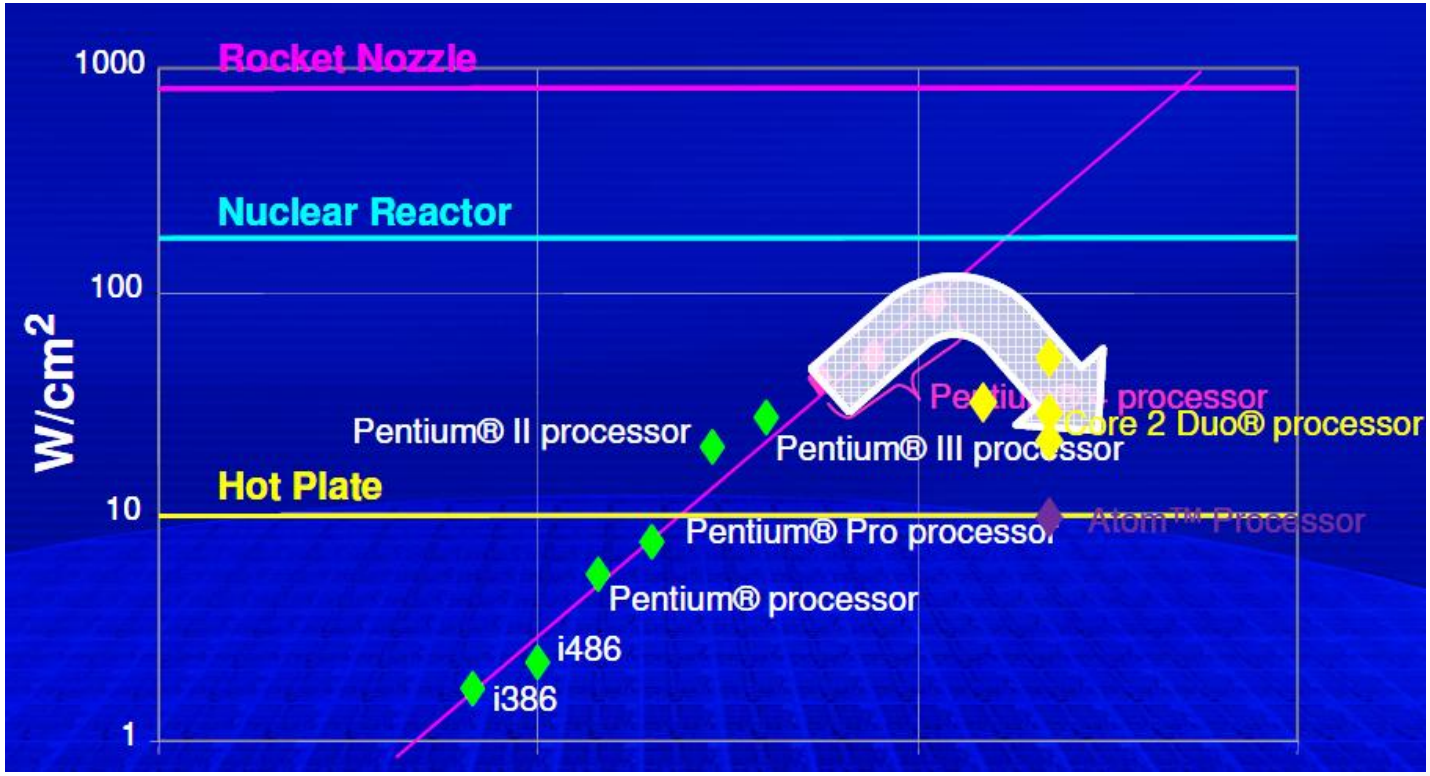


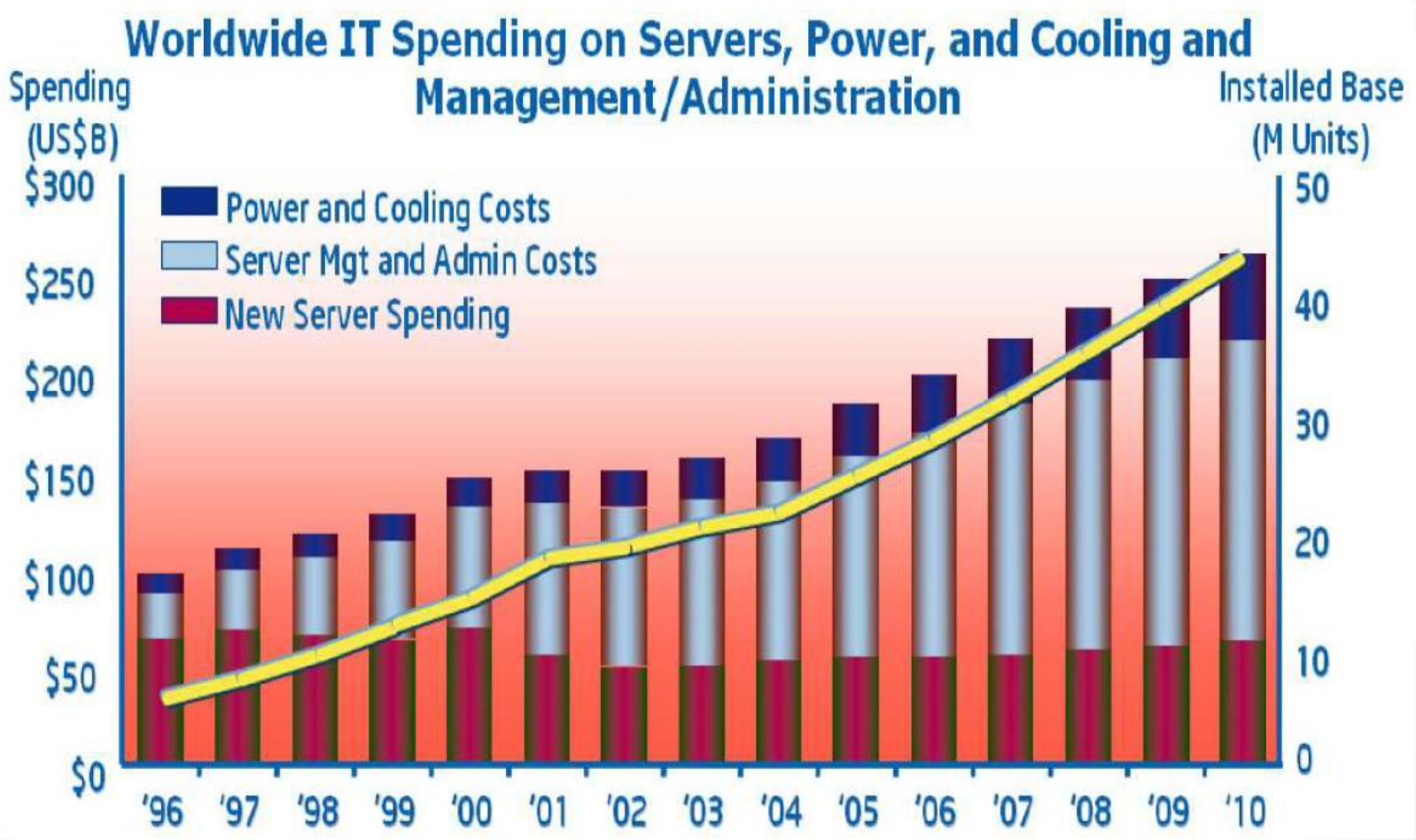
Figure 1. In CPU architecture today, heat is becoming an unmanageable problem. (Courtesy of Pat Gelsinger, Intel Developer Forum, Spring 2004)

Present Drivers for Spintronics

- Limit power consumption
- CPU solution = many cores
- Memory becoming the next problem



Power & Cooling Costs Still Increase



Present Drivers for Spintronics

Device Type	HDD	DRAM	NAND Flash	FRAM	MRAM	STTRAM	PCRAM	NRAM
Maturity	Product	Product	Product	Product	Product	Prototype	Product	Prototype
Present Density	400Gb/in^2 [7]	8Gb/chip [9]	64Gb/chip [10]	128Mb/chip	32Mb/chip	2Mb/chip	512Mb/chip	NA
Cell Size (SLC)	(2/3)F^2	6F^2	4F^2	6F^2	20F^2	4F^2	5F^2	5F^2
MLC Capability	No	No	4bits/cell	No	2bits/cell	4bits/cell	4bits/cell	No
Program Energy/bit	NA	2pJ	10nJ	2pJ	120pJ	0.02pJ	100pJ	10pJ [11]
Access Time (W/R)	9.5/8.5ms [8]	10/10ns	200/25us	50/75ns	12/12ns	10/10ns	100/20ns	10/10ns [11]
Endurance/Retention	NA	10^{16}/64ms	10^5/10yr	10^{15}/10yr	10^{16}/10yr	10^{16}/10yr	10^5/10yr	10^{16}/10yr

Device Type	RRAM	CBRAM	SEM	Polymer	Molecular	Racetrack	Holographic	Probe
Maturity	Research	Prototype	Prototype	Research	Research	Research	Product	Prototype
Present Density	64Kb/chip	2Mb/chip	128Mb/chip	128b/chip	160Kb/chip	NA	515Gb/in^2	1Tb/in^2
Cell Size	6F^2	6F^2	4F^2	6F^2	6F^2	N/A	N/A	N/A
MLC Capability	2bits/cell	2bits/cell	No	2bits/cell	No	12bits/cell	N/A	N/A
Program Energy/bit	2pJ	2pJ	13pJ	NA	NA	2pJ	N/A	100pJ [12]
Access Time (W/R)	10/20ns	50/50ns	100/20ns	30/30ns	20/20ns	10/10ns	3.1/5.4ms	10/10us
Endurance/Retention	10^6/10yr	10^6/Months	10^9/days	10^4/Months	10^5/Months	10^{16}/10yr	10^5/50yr	10^5/NA

Mark H. Kryder and Chang Soo Kim, IEEE Trans. Magn. **45**, 3406 (2009)

Outline

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  - Spin Transfer Torque MRAM (STT-MRAM)
  - Thermally Assisted Switching MRAM (TAS-MRAM)
  - Thermally Assisted STT-MRAM (TAS+STT-MRAM)
  - Thermagnonic STT-MRAM

- Spin Torque Oscillators

- Spin Torque Microwave Detectors

NANO-TEC

Toggle MRAM

Technology	Toggle MRAM – Commercially Available
Gain **Signal/Noise ratio** **Non-linearity**	N/A N/A N/A
Speed **Power consumption**	40 MHz Zero stand-by power, ~120 pJ per switching event
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	CMOS compatible, embeddable, modular
Other specific properties	Radiation hard, High Reliability, Temperature range
Manufacturability **(Fabrication processes needed, tolerances etc.)**	CMOS compatible
Timeline **(When exploitable or when foreseen in production)**	Commercialized

STT-MRAM

Technology	Spin Transfer Torque MRAM (STT-MRAM)
Gain **Signal/Noise ratio** **Non-linearity**	N/A N/A N/A
Speed **Power consumption**	40 MHz Zero stand-by power, ~0.02 - 2 pJ per switching event
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	CMOS compatible, embeddable, modular
Other specific properties	Radiation hard
Manufacturability **(Fabrication processes needed, tolerances etc.)**	CMOS compatible
Timeline **(When exploitable or when foreseen in production)**	1-3 years

TAS-MRAM

Technology	Thermally Assisted Switching MRAM (TAS-MRAM)
Gain **Signal/Noise ratio** **Non-linearity**	N/A N/A N/A
Speed **Power consumption**	40 MHz Zero stand-by power
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	CMOS compatible, embeddable, modular
Other specific properties	Radiation hard
Manufacturability **(Fabrication processes needed, tolerances etc.)**	CMOS compatible Reliability?
Timeline **(When exploitable or when foreseen in production)**	1-3 years?

TAS+STT-MRAM

Technology	Thermally Assisted STT-MRAM (TAS+STT-MRAM)
Gain **Signal/Noise ratio** **Non-linearity**	N/A N/A N/A
Speed **Power consumption**	40 MHz Zero stand-by power, 2-3 pJ per switching event
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	CMOS compatible, embeddable, modular
Other specific properties	Radiation hard
Manufacturability **(Fabrication processes needed, tolerances etc.)**	CMOS compatible Reliability?
Timeline **(When exploitable or when foreseen in production)**	1-3 years?

Thermagnonic STT-MRAM

Technology	Thermagnonic STT-MRAM
Gain **Signal/Noise ratio** **Non-linearity**	N/A N/A N/A
Speed **Power consumption**	40 MHz Zero stand-by power, <1 pJ per switching event
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	
Other specific properties	Radiation hard
Manufacturability **(Fabrication processes needed, tolerances etc.)**	CMOS compatible? Functionality demonstrated?
Timeline **(When exploitable or when foreseen in production)**	3-5 years

Spin Torque Oscillators (STO)

Technology	Spin Torque Oscillators (STO)
Gain **Signal/Noise ratio** **Non-linearity**	N/A Low to moderate signal, high phase noise Mostly linear
Speed **Power consumption**	0.1 - 50 GHz demonstrated, >100 GHz expected Low to moderate depending on technology
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	CMOS compatible, embeddable, modular
Other specific properties	Ultra wide band, Ultra high modulation rates, Nano size
Manufacturability **(Fabrication processes needed, tolerances etc.)**	RF CMOS compatible GMR based STOs show good wafer uniformity
Timeline **(When exploitable or when foreseen in production)**	3-5 years

Spin Torque Microwave Detectors

Technology	Spin Torque Microwave Detectors
Gain **Signal/Noise ratio** **Non-linearity**	N/A High signal, noise reasonably good Mostly linear
Speed **Power consumption**	Very fast, >1 GHz expected Low
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	CMOS compatible, embeddable, modular
Other specific properties	Ultra wide band, Nano size, Good spectral resolution
Manufacturability **(Fabrication processes needed, tolerances etc.)**	RF CMOS compatible
Timeline **(When exploitable or when foreseen in production)**	3-5 years

Memristors

J. Grollier

Unité Mixte de Physique CNRS/Thales

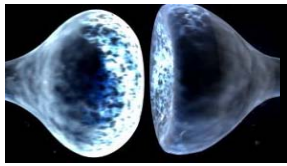
Palaiseau, France

cnrs

UNIVERSITÉ PARIS-SUD 11

THALES

erc Nanobrain



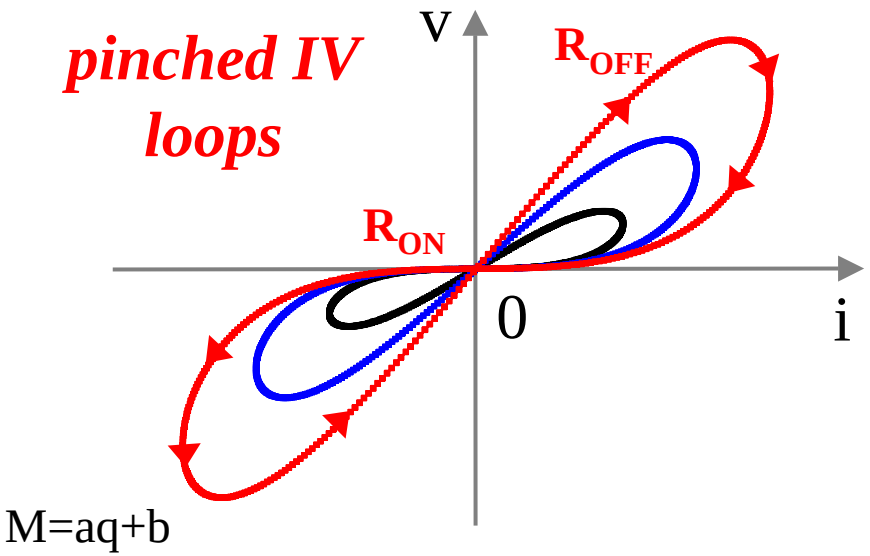
Memristor

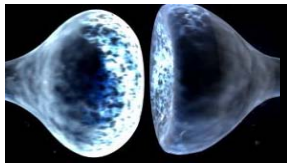
L. O. Chua, "memristor – the missing circuit element" IEEE Trans. Circuit Theory (1971)

$$v = M(q)\, i$$

M is a resistance that "remembers" how much current was injected, and how long

continuously tunable between R_{ON} and R_{OFF}





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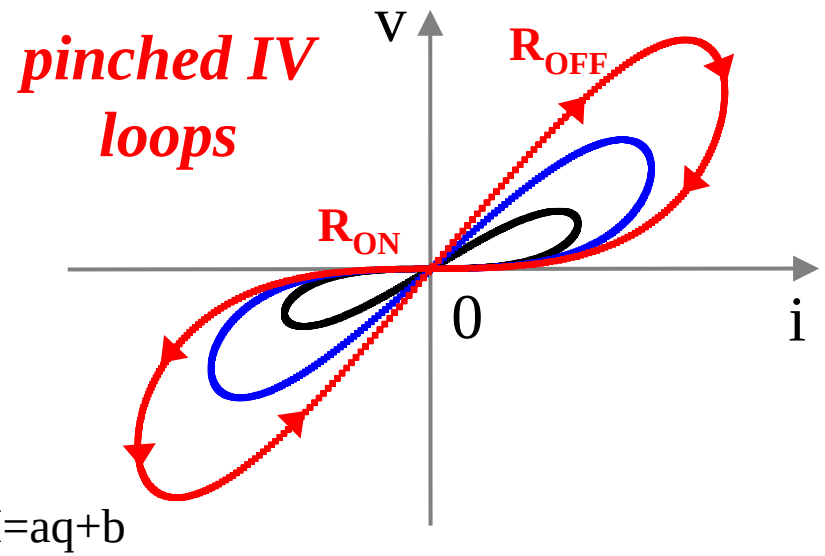
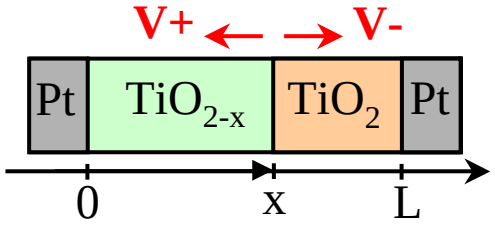


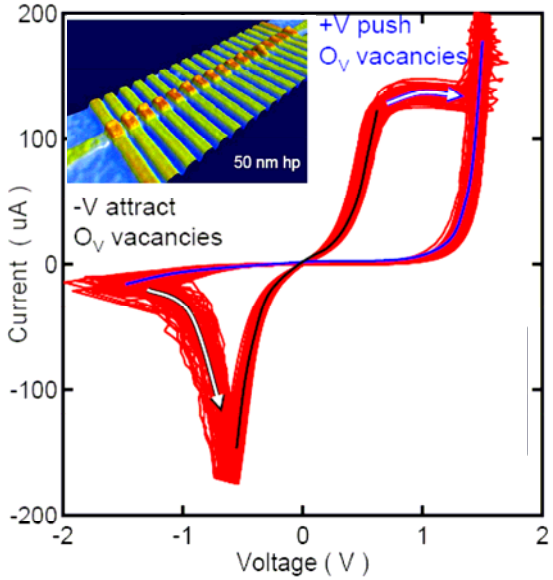
M=aq+b

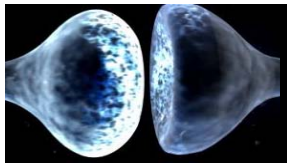
the HP memristor



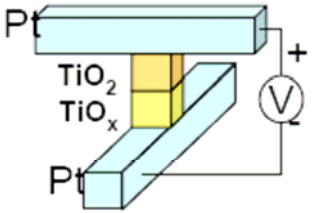
ions electromigration

Yang et al., Nature Nano (2008)



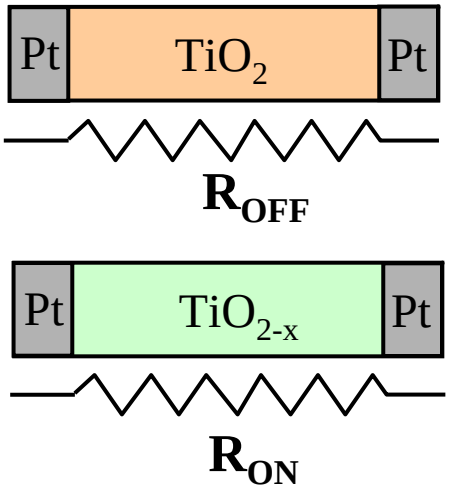


Hewlett-Packard Memristor

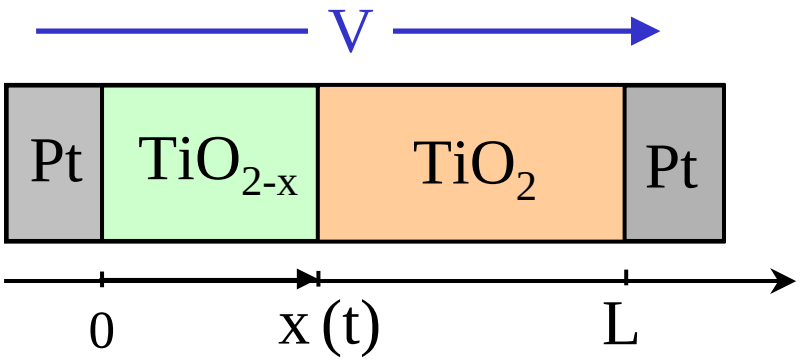


< 30x30 nm²

$$\frac{R_{OFF}}{R_{ON}} > 1000$$



migration of oxygen vacancies



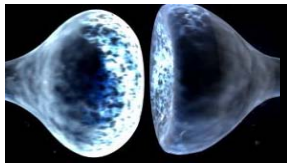
$$R = R_{ON}\frac{x}{L} + R_{OFF}\left(1 - \frac{x}{L}\right)$$

displacement proportional to the charge

$$x \propto q$$

$$M(q) \cong R_{OFF}\left[1 - \mu\frac{R_{ON}}{L^2}q\right]$$

Strukov, Snider, Stewart & Williams, Nature 453 (2008)



Memristor applications

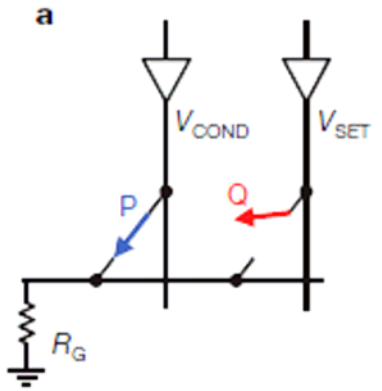
- non-volatile digital memories

(R_{OFF}/R_{ON}>1000)

- logic functions (no transistors)

Kuekes et al., JAP 2005

Borghetti et al., Nature 2010



b

$q' \leftarrow pIMPq$

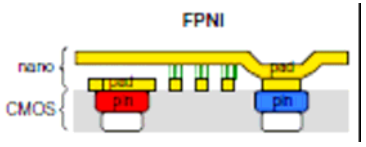
In p	In q	Out q'
0	0	1
0	1	1
1	0	0
1	1	1

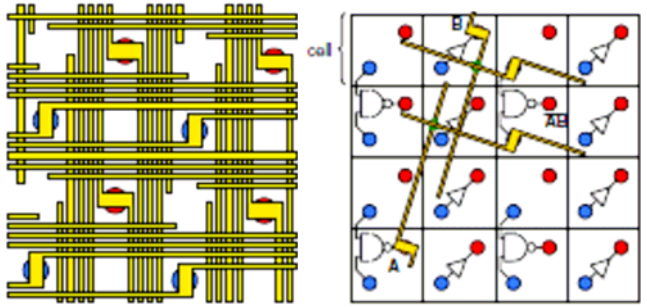
- Reconfigurable Architectures

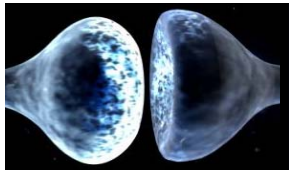
(Field Programmable Gate Arrays)

Snider et al., Nanotechnology 2007

Field Programmable Nanowire Interconnect



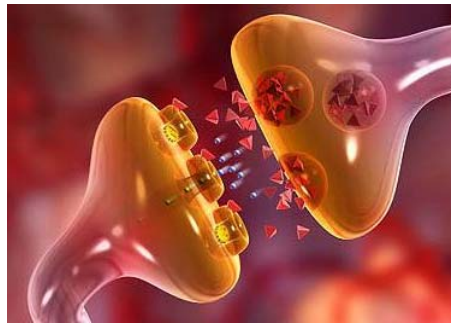




Memristors : artificial synapses

biological synapse : synaptic plasticity

change in strength in response to either use or disuse of transmission

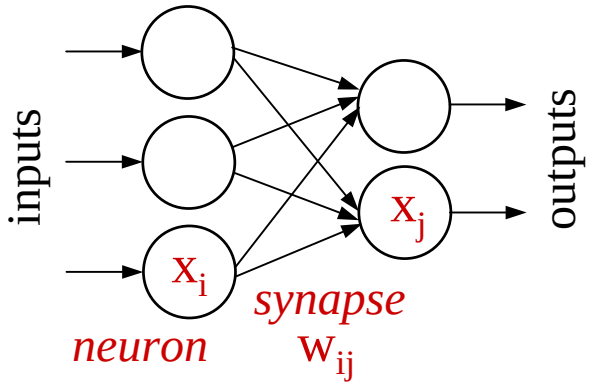


Memristors directly implement the synaptic plasticity

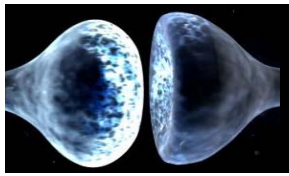
- v = M(q) i
- sub-µm size

key to the development of hardware Artificial Neural Networks

Bio-inspired computing architectures



- w_{ij} : synaptic weights
  - network memory
  - efficiency to transmit information
  - adjustable = **plasticity** = learning
- huge interconnectivity



Von Neumann vs. Neuromorphic computing

- **Human brain**

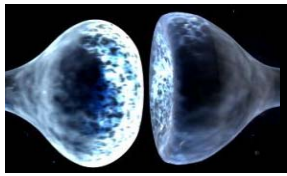
parallel architecture	**analog**
10^{11} neurons	10 Hz
10^{15} synapses	20 W

- **Simulations of mouse cortex on Blue Gene L**

Von-Neumann architecture	**digital**
8.10^{4} neurons	1 GHz
5.10^{10} synapses	40 kW
super-computers slower than mouse (×10)	

- **Advantages of parallel, analog architecture**

speed, low energy consumption, defect tolerance



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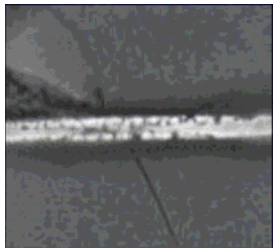
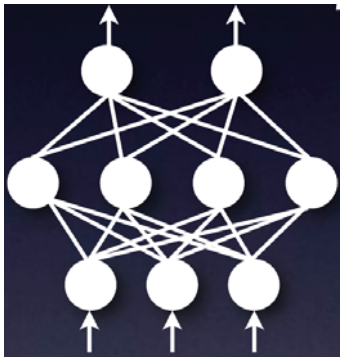


Constraints

Neurobiology



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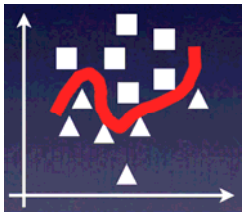
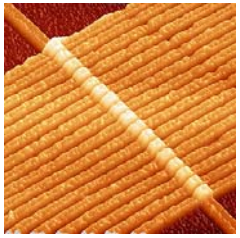


Machine learning

Applications



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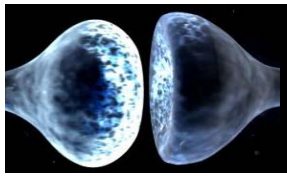
O. Temam, The rebirth of Neural Networks, Proc. ISCA'2010



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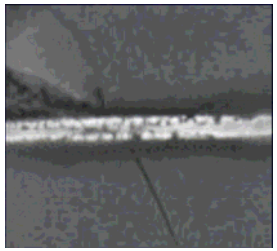

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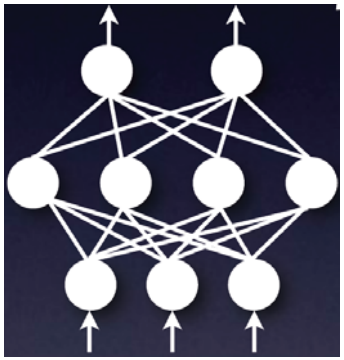

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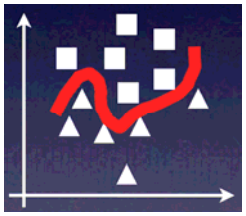

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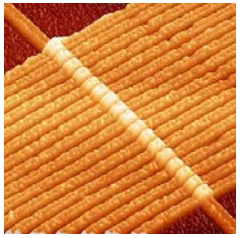

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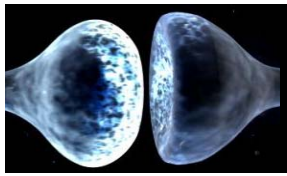

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• defects
• heterogenerous multi-cores

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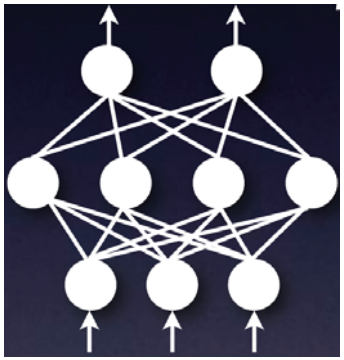

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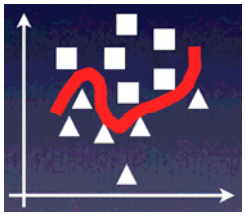

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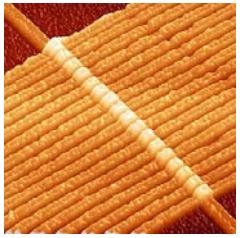

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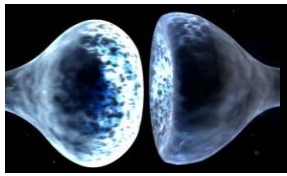

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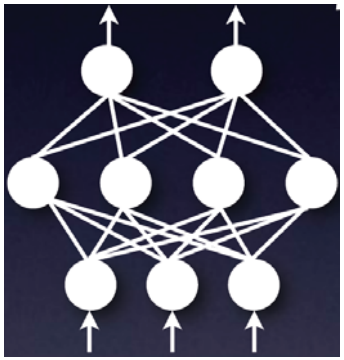

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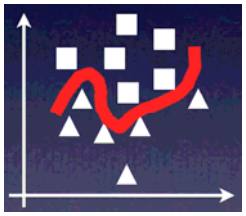

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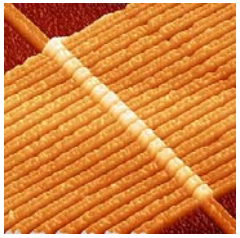

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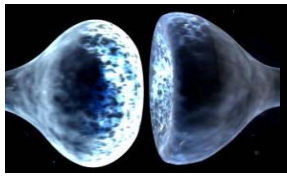

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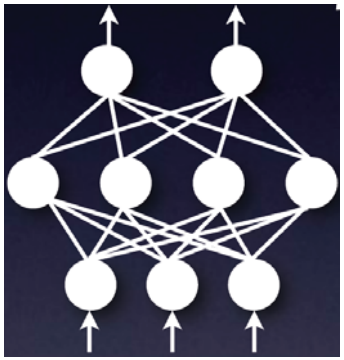

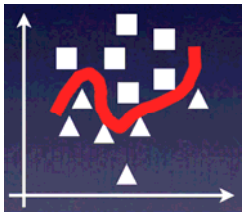

Machine learning

Intel 2005 :
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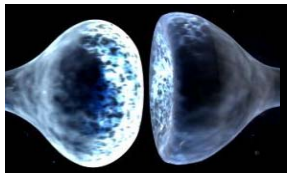

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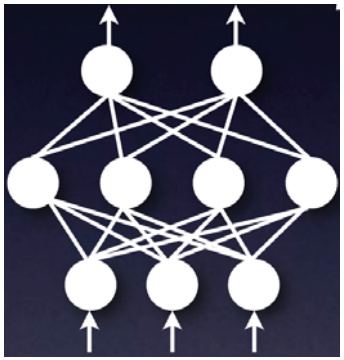

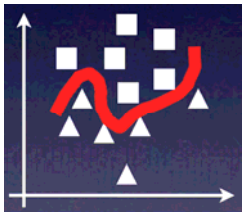

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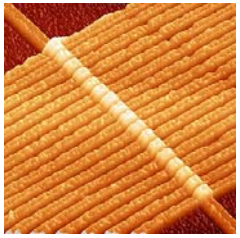

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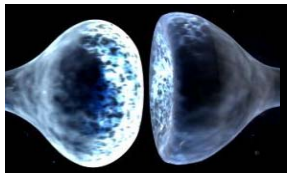

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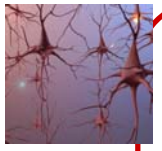
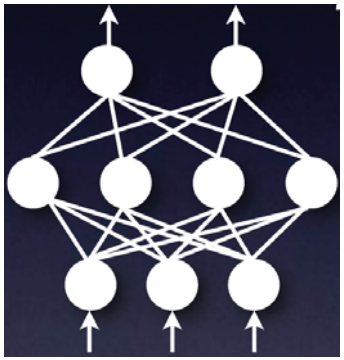


• brain reverse enginering
• visual cortex
ex : T. Poggio

Neurobiology



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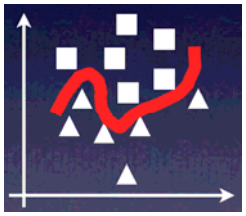

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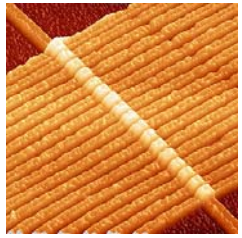

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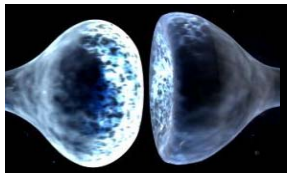

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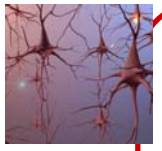

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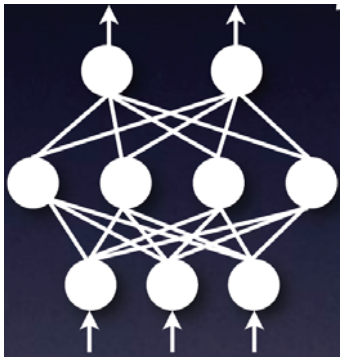

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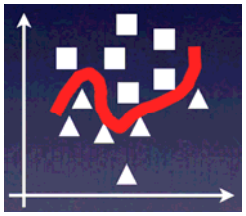

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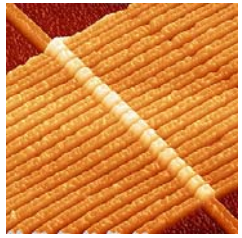

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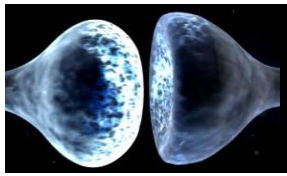

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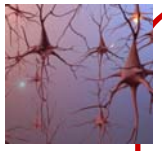

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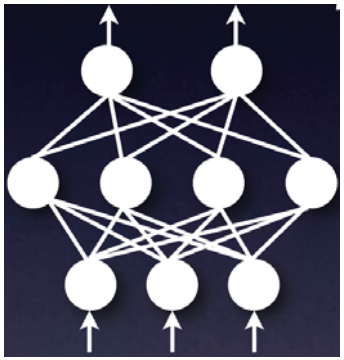

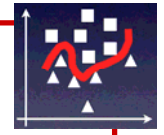

• deep networks
• powerfull classifiers

Machine learning

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Hardware ANNs

Nanotechnology

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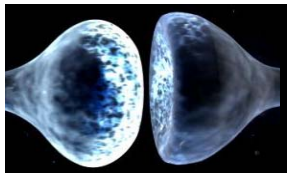

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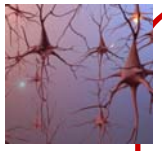

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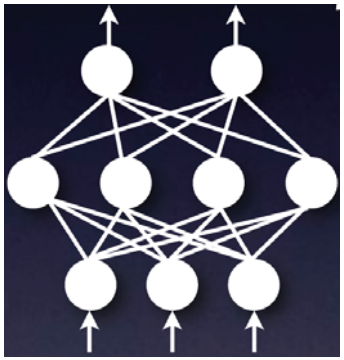
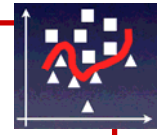
ex : T. Poggio

Neurobiology



Hardware ANNs



• deep networks
• powerfull classifiers

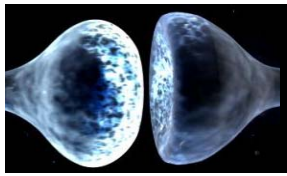
Machine learning

Intel 2005 :
• Recognition
• Mining
• Synthesis

Applications

Nanotechnology

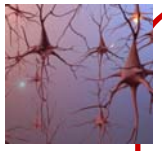
O. Temam, The rebirth of Neural Networks, Proc. ISCA'2010



Convergence of trends

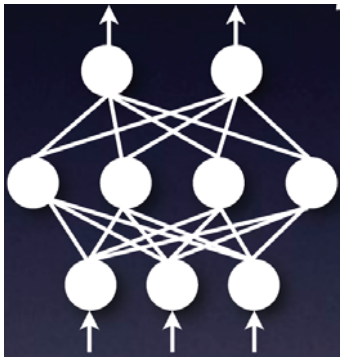
• power limita-
-tions : Multi-cores
• defects
• heterogenerous multi-cores

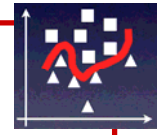
Constraints



• brain reverse enginering
• visual cortex
ex : T. Poggio

Neurobiology





• deep networks
• powerfull classifiers

Machine learning

Intel 2005 :
• Recognition
• Mining
• Synthesis

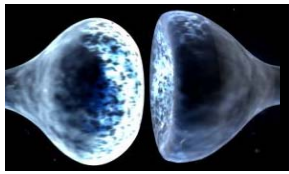
Applications

Hardware ANNs

• 1 memristor = 1 synapse
• 3D stacking
• 10^4 synapses/neuron

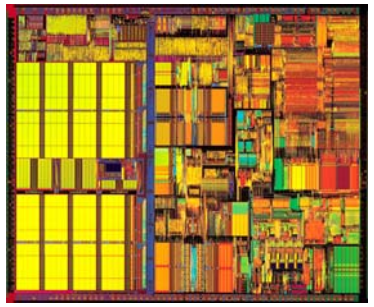
Nanotechnology

O. Temam, The rebirth of Neural Networks, Proc. ISCA'2010

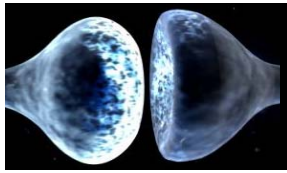


Memristors synapses : applications

• **Hardware ANNs accelerators (heterogenous multi-core)**



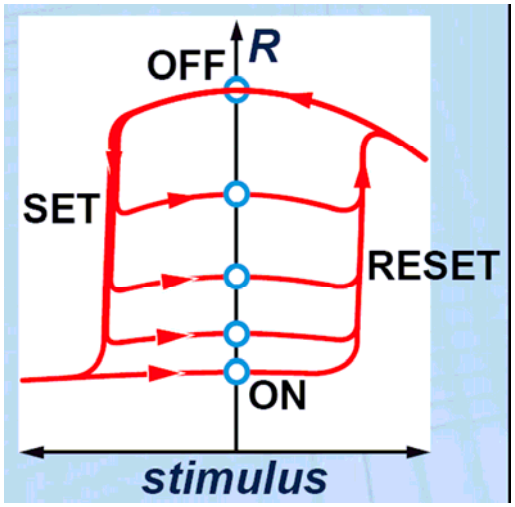
• **Large scale hardware simulations of the human brain ?**



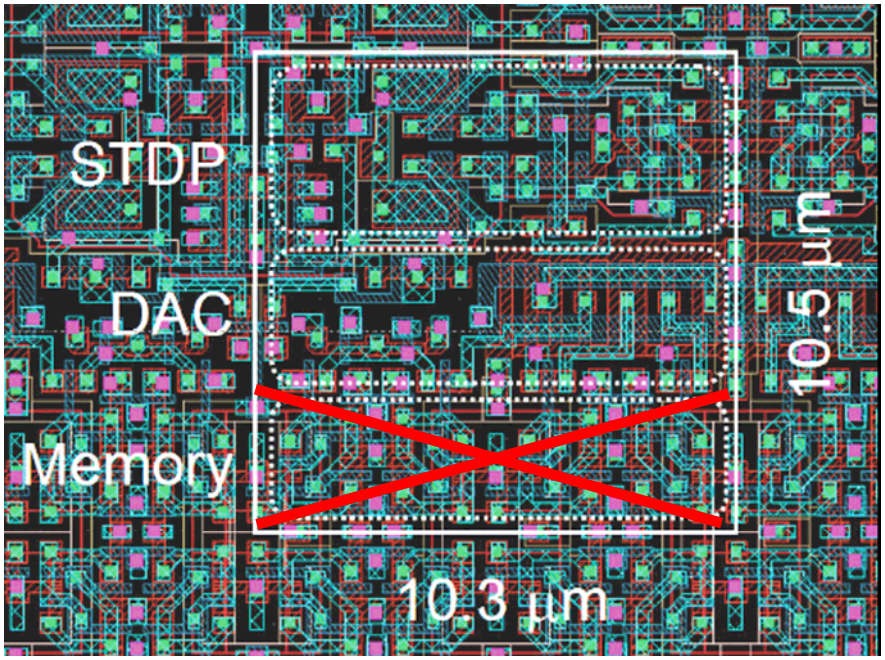
Memristors : artificial synapses

- **Memristors directly store the synaptic weights *(w = conductance)***

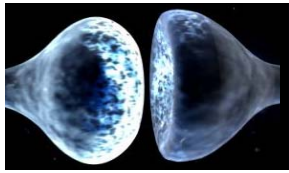
Non-volative multi-valued resistances



No need for space consuming SRAM banks



Schemmel *et al.*, IJCNN 2006

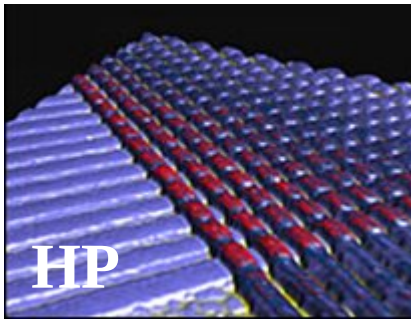


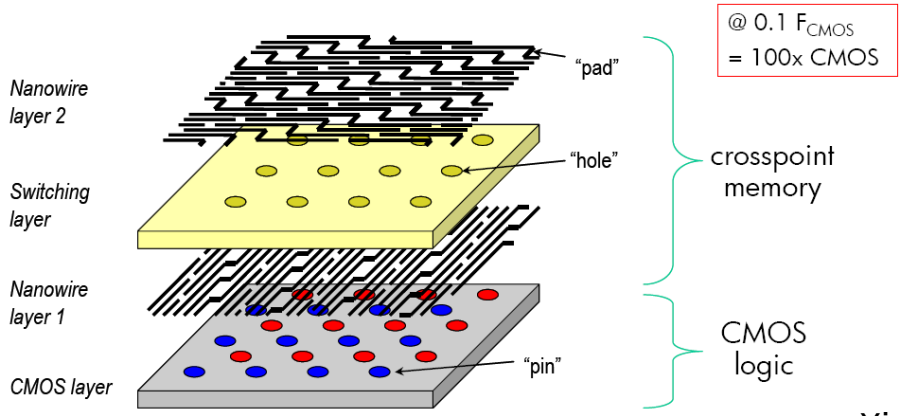
Memristors : artificial synapses

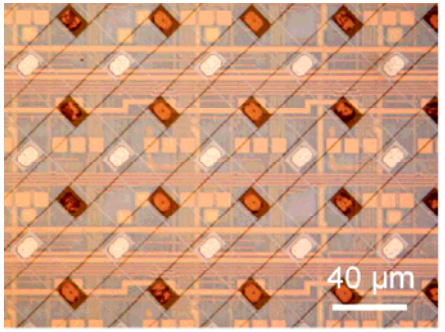
- **Memristors are small *(< 50 x 50 nm^2)***

interconnection issue : about 10^4 synapses per neuron in the brain

ex : CMOS “neurons” + memristive “synapses”





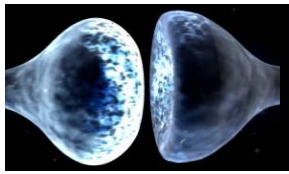


Xia *et al.,* Nanoletters (2010)

memristor crossbar arrays

No demonstration yet of operational mixed memristor/CMOS cognitive chip

to be solved : cross-talk, sneak paths, lithography



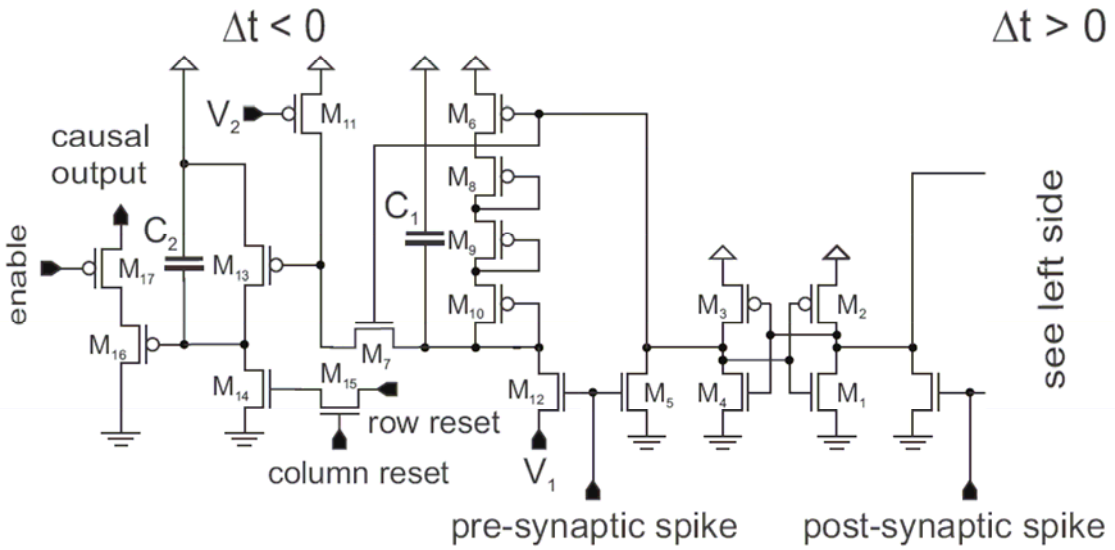
Memristors : artificial synapses

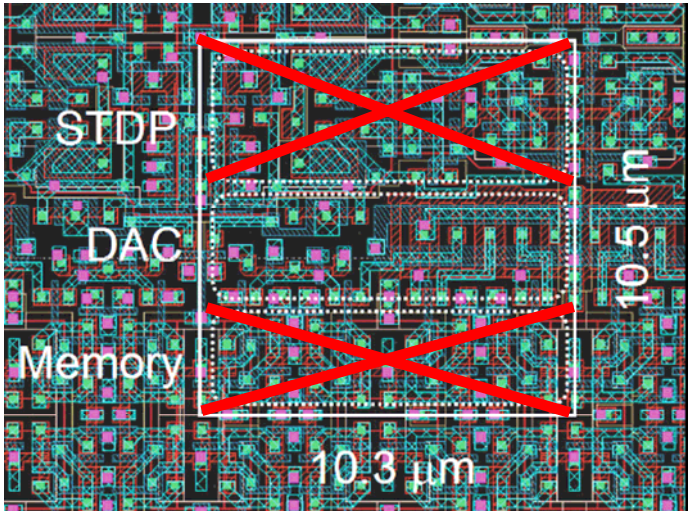
- **Memristors directly implement the synaptic plasticity**

  change in strength in response to either use or disuse of transmission

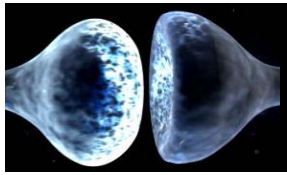
  - v = M(q) i

No need for space consuming complicated CMOS circuits





Schemmel *et al.*, IJCNN 2006

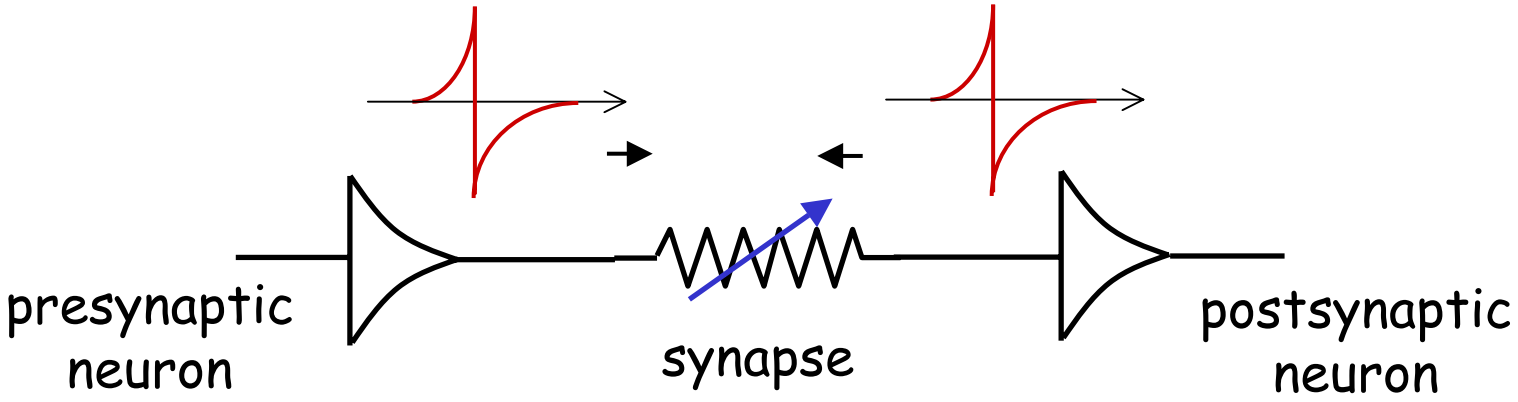


Hebbian learning

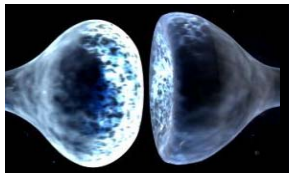
- **Learning rule :**

« Neurons that fire together wire together » Hebb, 1949

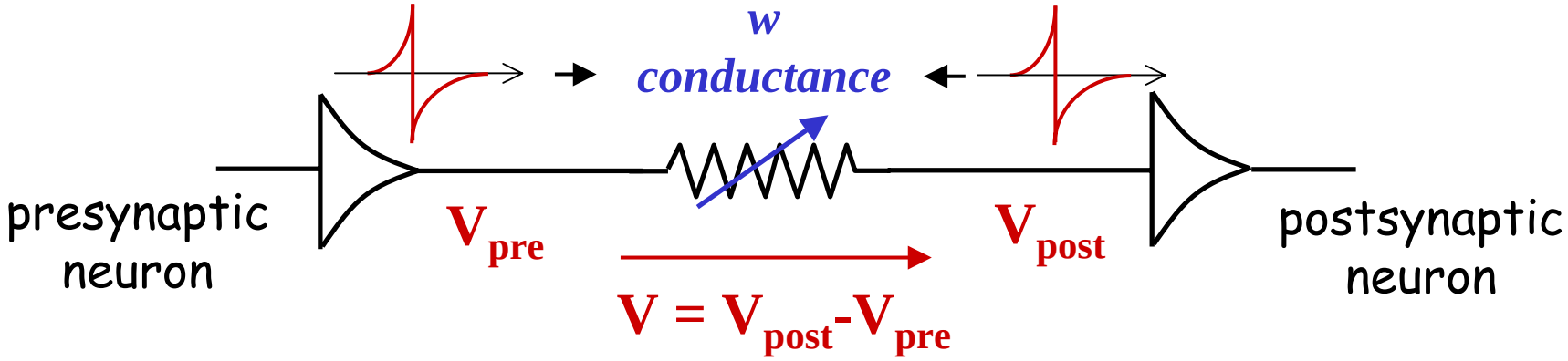
- **Spike timing dependent plasticity :**



- causality is important:
transmission enhanced if post-neuron fires after pre-neuron
- timing is important :
–ΔT small, large transmission changes

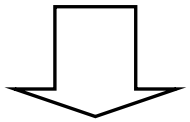


Spike timing dependent plasticity

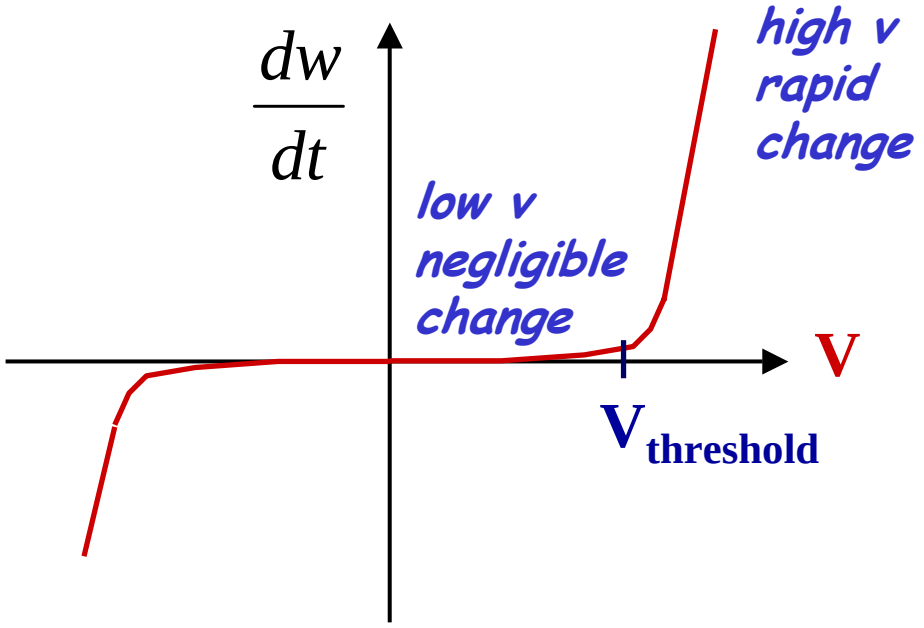


- **change of conductance vs. applied voltage :**

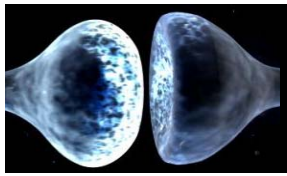
general shape for memristors



enables learning



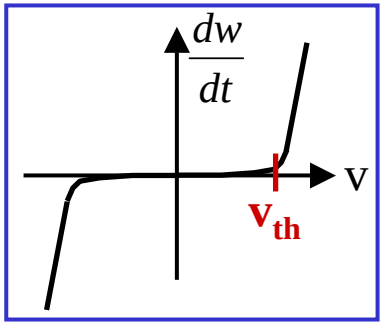
Snider *et al.*, Nanotechnology 2007

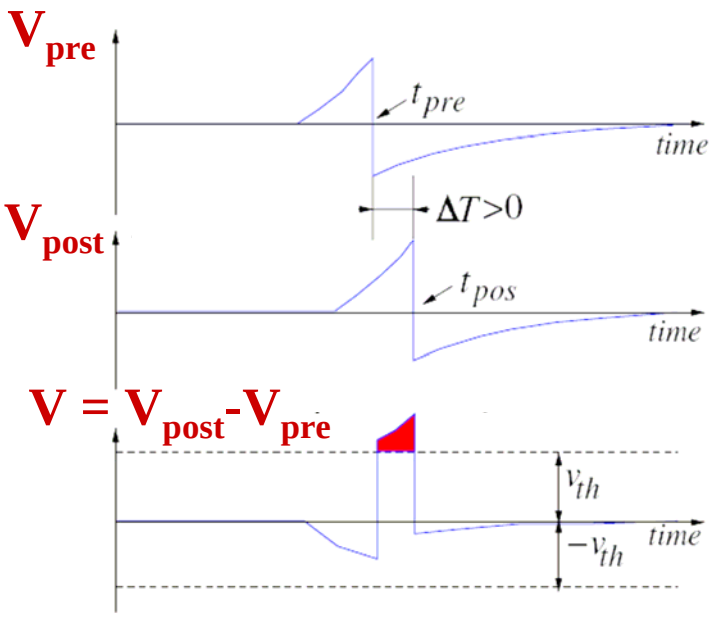


Spike timing dependent plasticity

Memristor change of conductance (synapse weight)

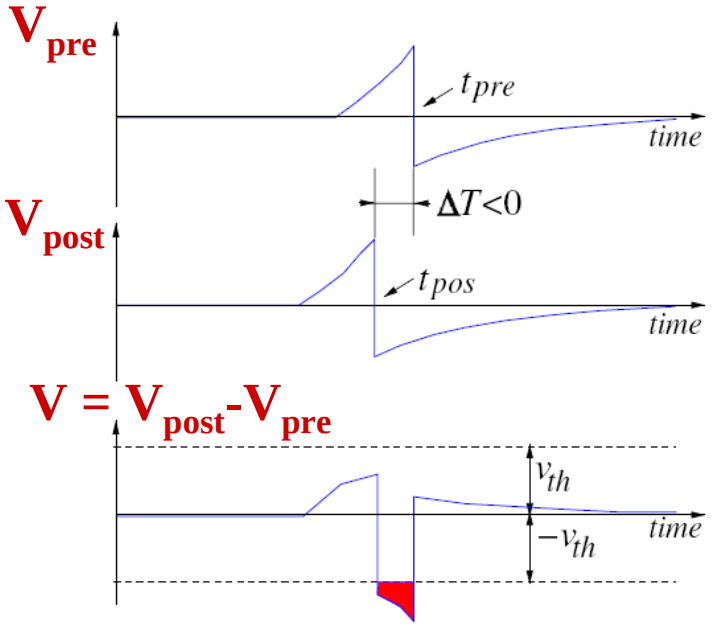
Linarres-Barranco *et al.*, frontiers in Neuroscience, 2011





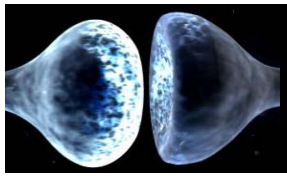
conductance increase

potentiation



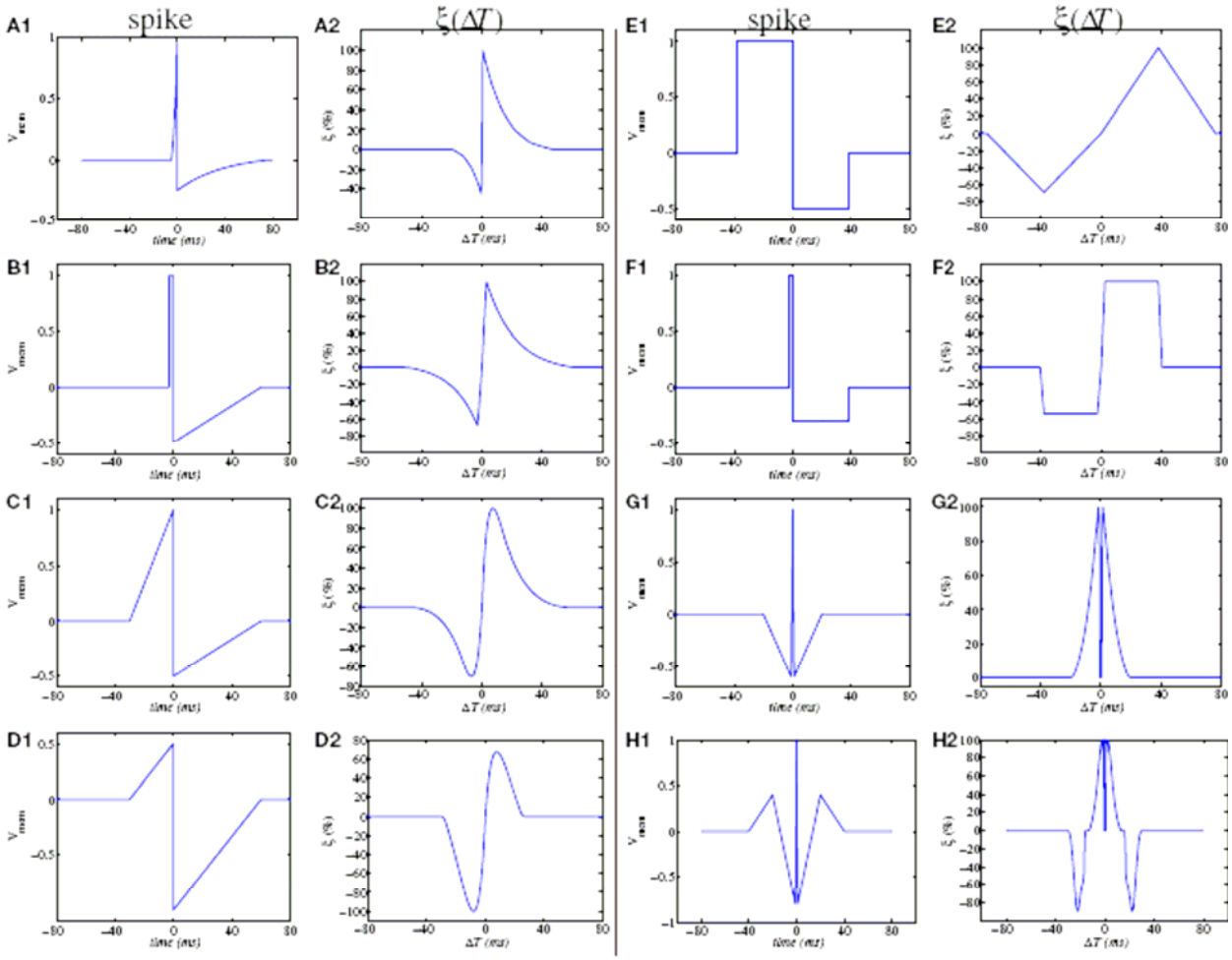
conductance decrease

depression

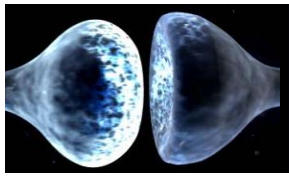


STDP curve vs action potential shape

Linarres-Barranco *et al.*, frontiers in Neuroscience, 2011

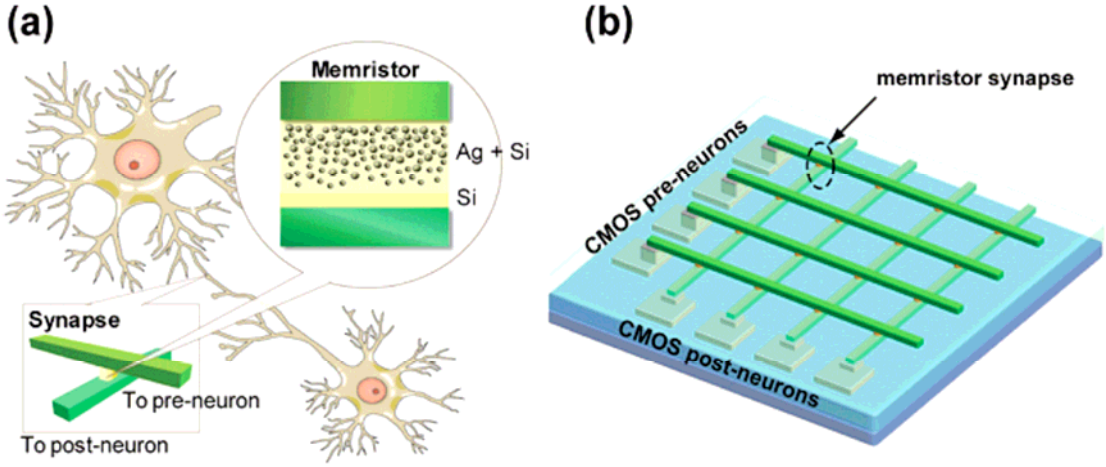


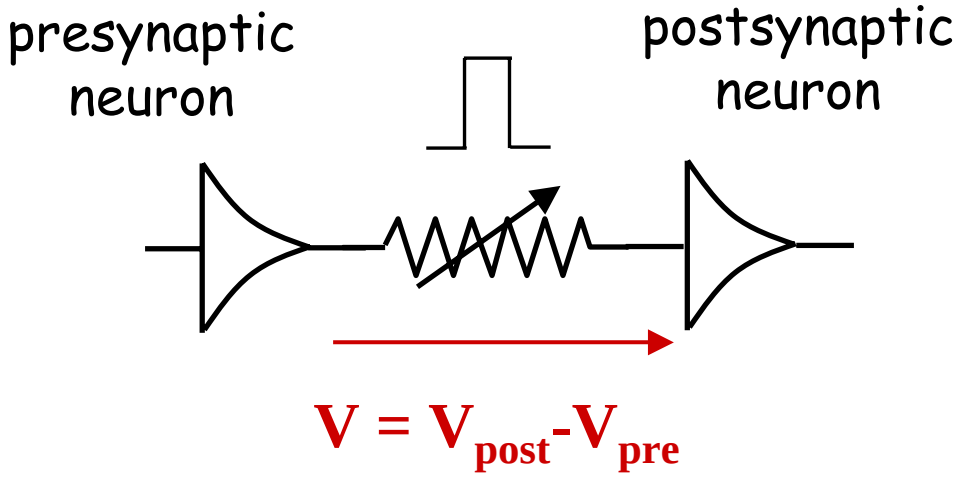
possibility to implement different kinds of STDP with a single device

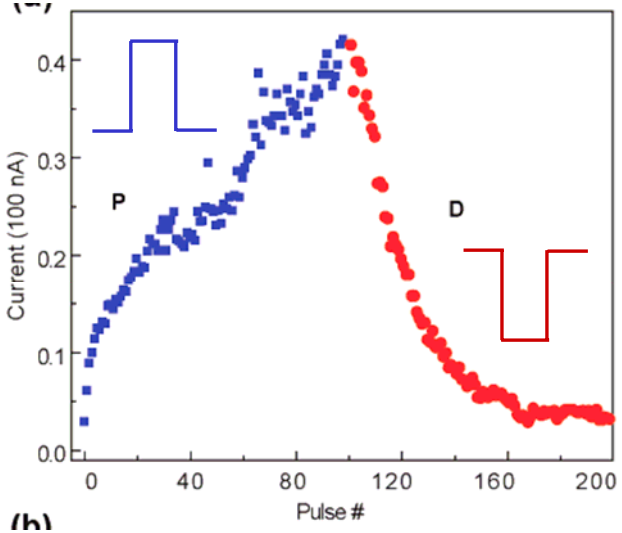


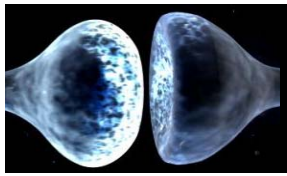
STDP : experimental implementation

Jo *et al.*, Nanoletters 2010



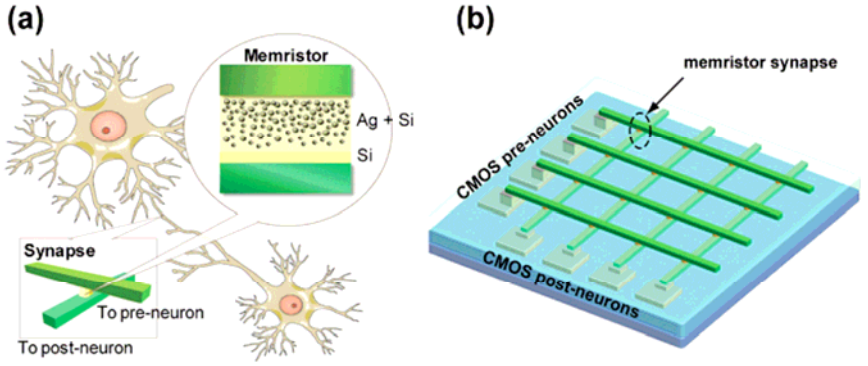




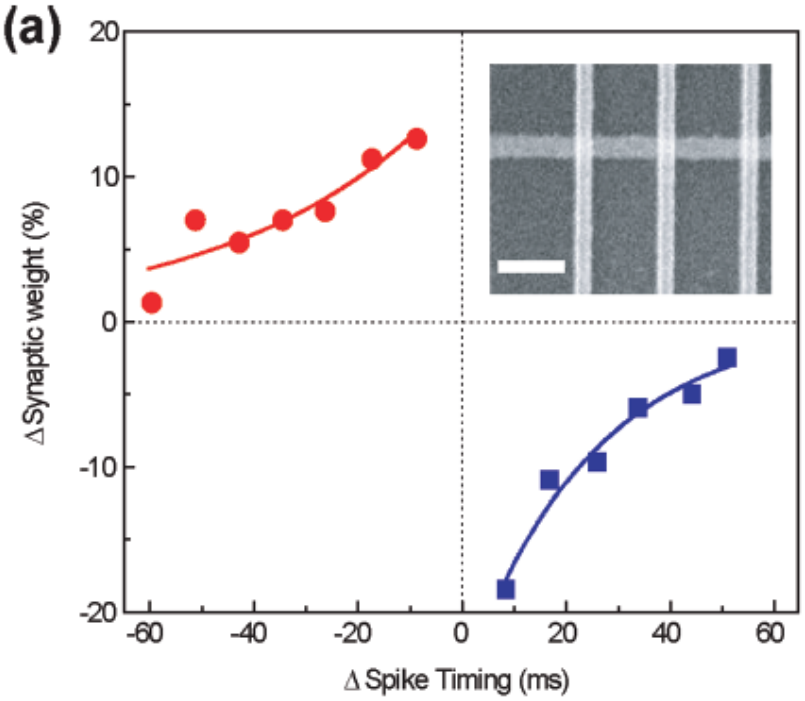


STDP : experimental implementation

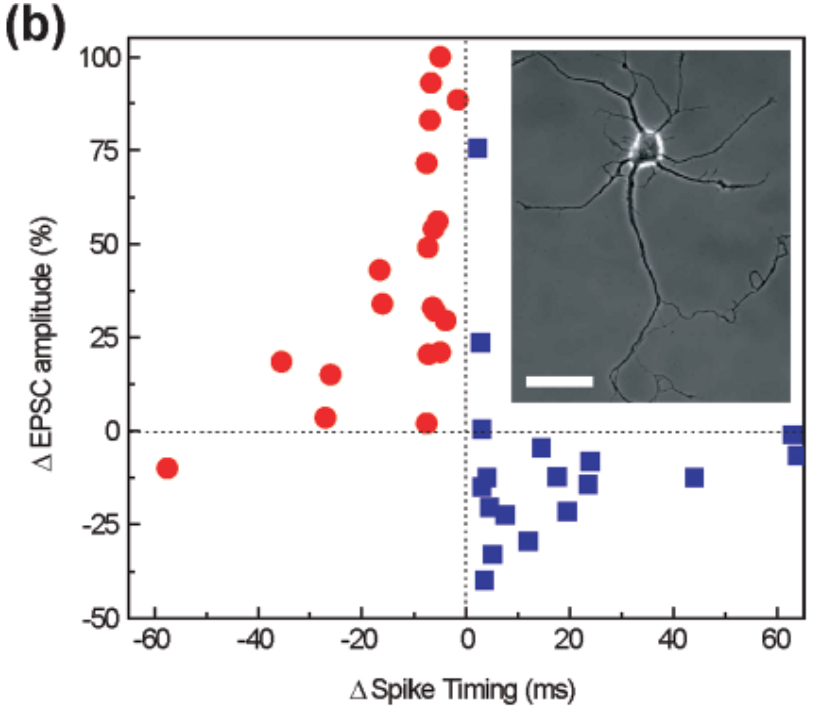
Jo *et al.*, Nanoletters 2010

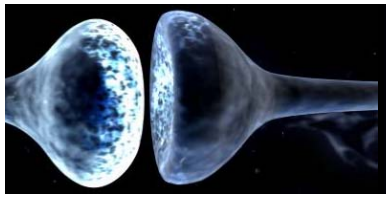


Memristor STDP curve



Bi & Poo 1998





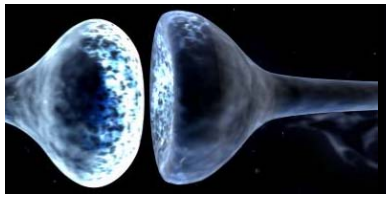
Which memristor ?

After (and even before) Hewlett-Packard TiO_2 memristor was proposed, many other very different memristor concepts were identified :

Erokhin et al., Surface and thin films (2007) *PANI*
A.A. Zakhidov et al., Organic elec. (2009) *metal/mixed conductor/metal*
F. Alibart et al., Advanced Func. Mater. (2009) *Pentacene + gold particles*
Ben Jamaa et al., IEEE Nano (2009) *Poly-cristalline Si nanowires*
Derycke et al., TNT (2009) *Carbone nanotubes*
Driscol et al., APL (2009) *Phase change material*
Gergel et al., IEEE EL (2009) *flexible TiO2*
Jo et al., Nanoletters (2009) *Ag/Si*
Wang et al., IEEE EL (2009) *spintronics*
Kim et al., Nanoletters (2009) *nanoparticle assemblies*
Jeong et al., Nanoletters (2010) *graphene*
Lee et al., Nature Materials (2011) *Ta2O5*
Ohno et al., Nature Materials (2011) *atomic switches*
Chanthbouala, Grollier et al., Nature Physics (2011) *spintronics*
….

Classification :

- ***Organic memristors***
- ***Most Resistive Switching memristors***



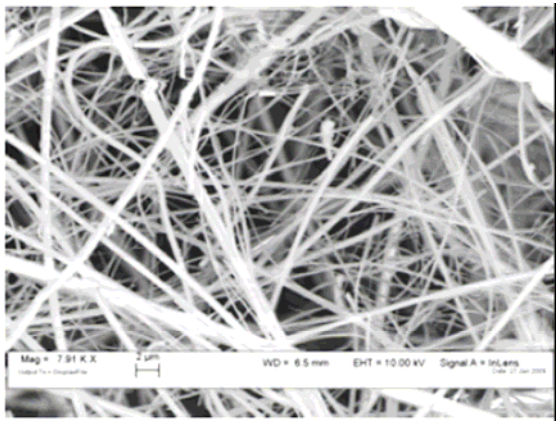
Organic memristors

• ***Organic memristors :*** NOMFET (polymer), CNT-FET, PANI….

- additional functionalities
ex : interaction with light

-bottom up approach
ex : self-organization

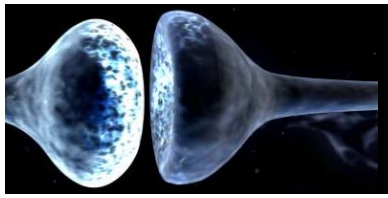
- high density



Erokhin *et al.*, NanoNet 2009

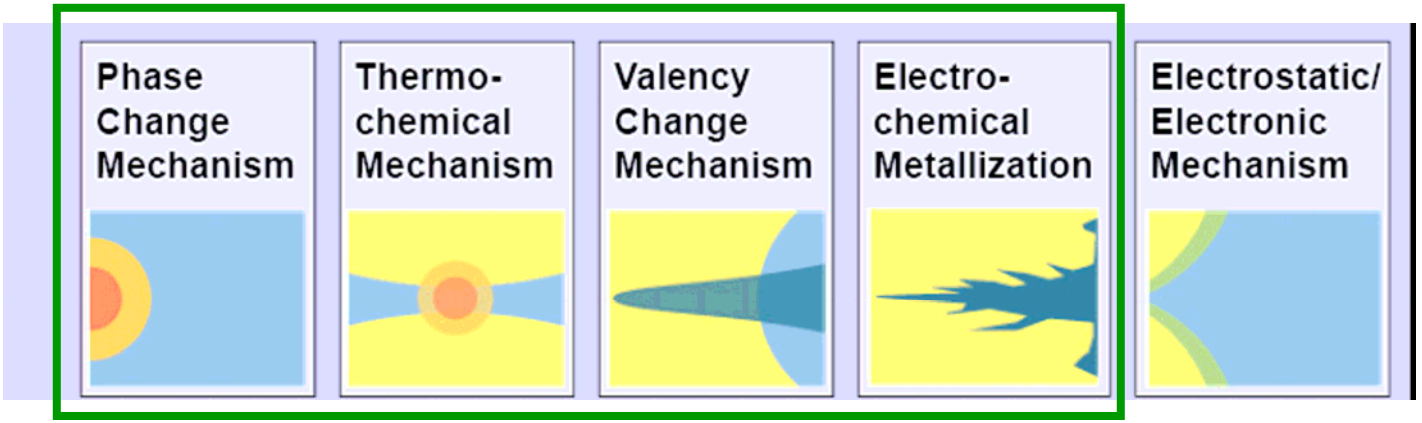
• Very promising
• time scale > 10 years

FP7 Bion & Nabab projects



Resistive switching memristors

"easy" implementation in crossbar arrays – top down approach



Waser *et al.*, Nature Materials 2007

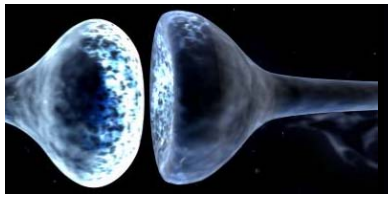
- defect-mediated : thermal effects, ionic motion

Ex : HP memristor based on electromigration : reliability / endurance issues

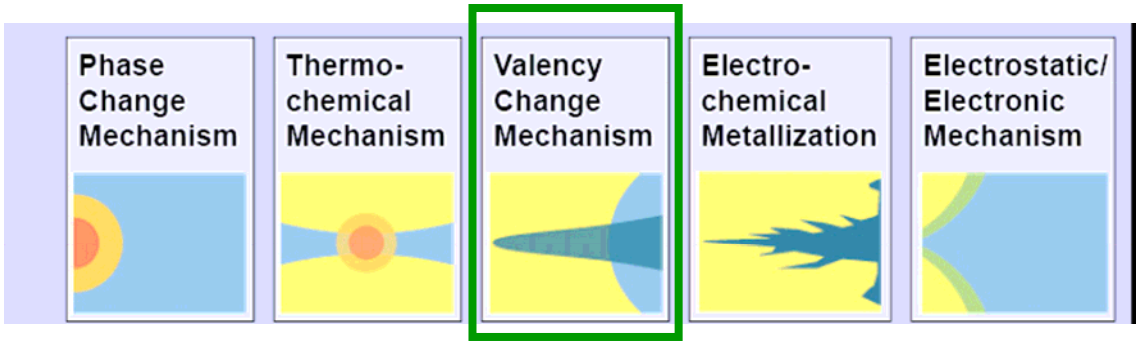
- large local heating - need of a forming step - physics not understood

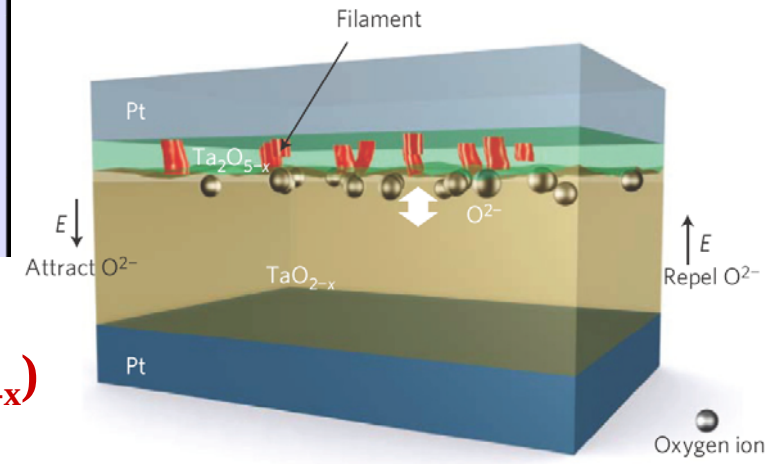
- the most mature existing technology

- Strukov et al., Nature 2008 (TiO2)
- Jo et al., Nanoletters 2010 (Ag/Si, no forming step)

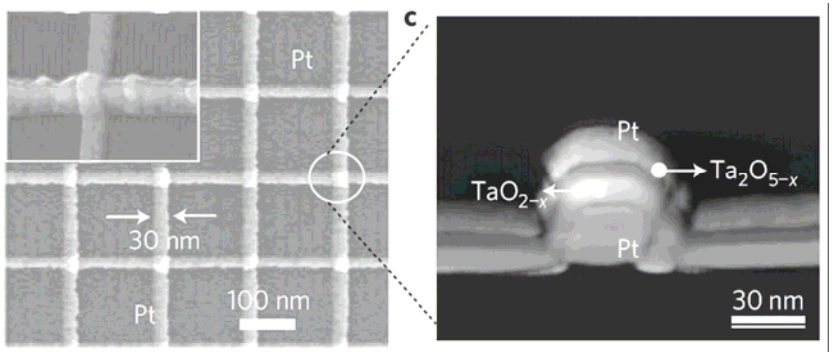


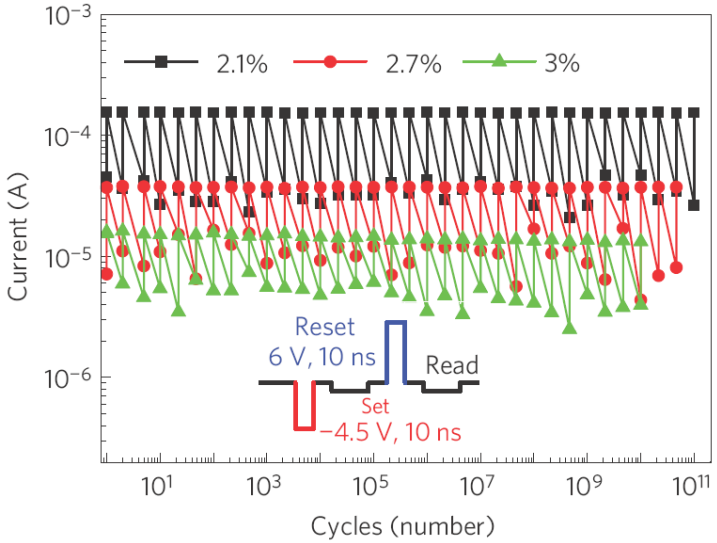
Resistive switching memristors



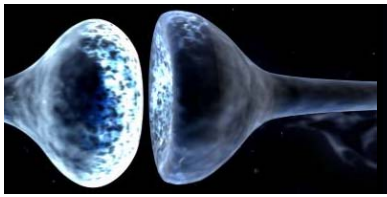


Lee et al., Nature Materials 2011 (Ta_2O_{5-x}/Ta_{2-x})

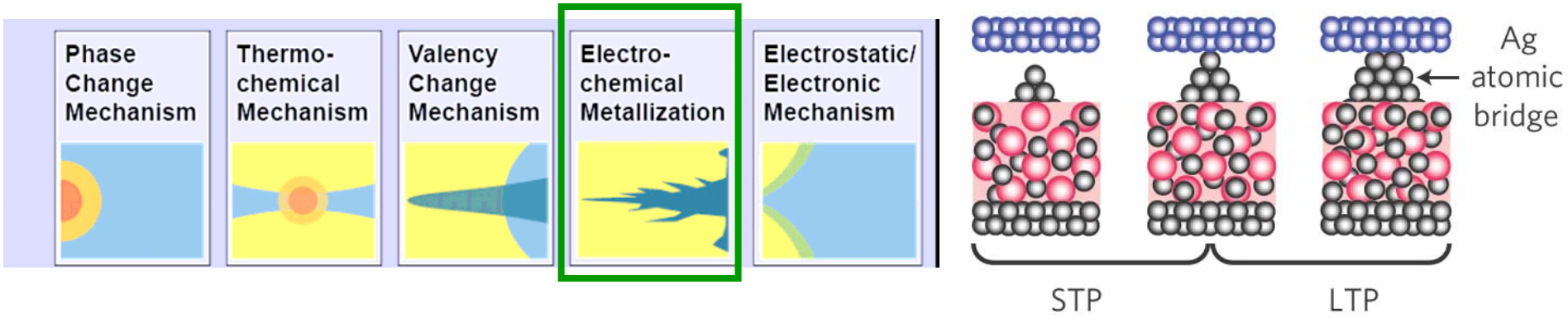




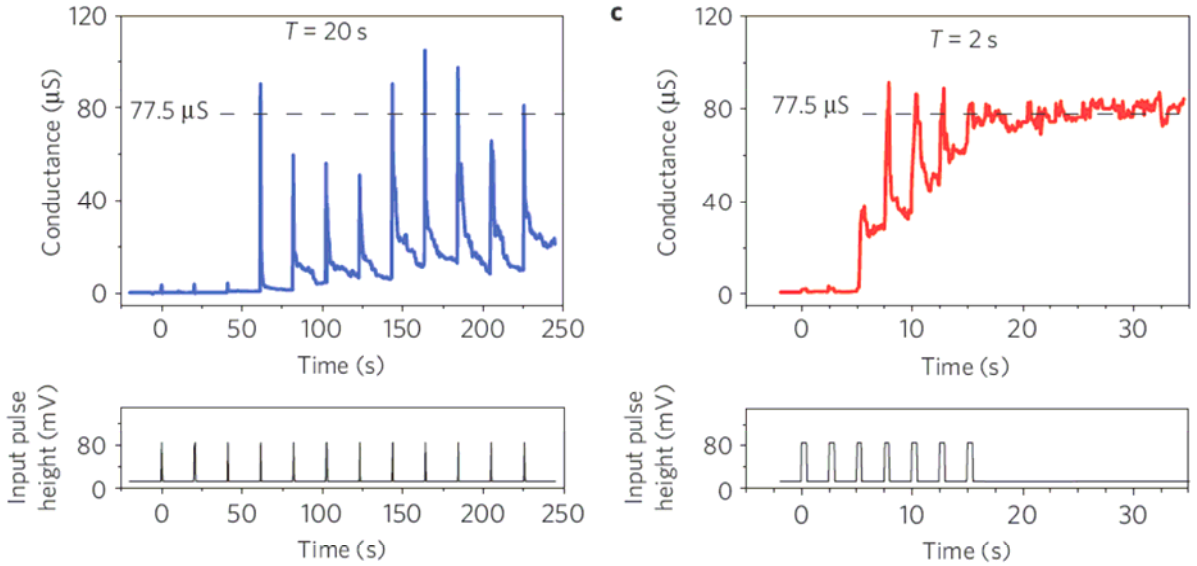
good cyclability > 10^{12}, fast (10ns) and reduced power consumption



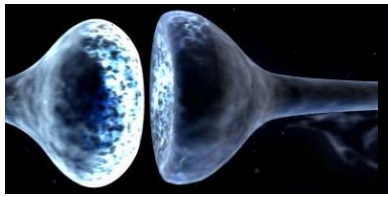
Resistive switching memristors



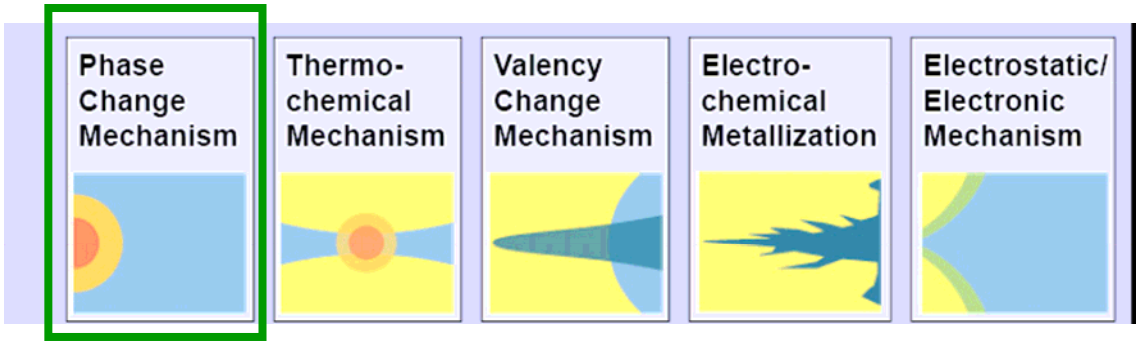
Ohno et al., Nature Materials 2011 (Ag_2S atomic switch)

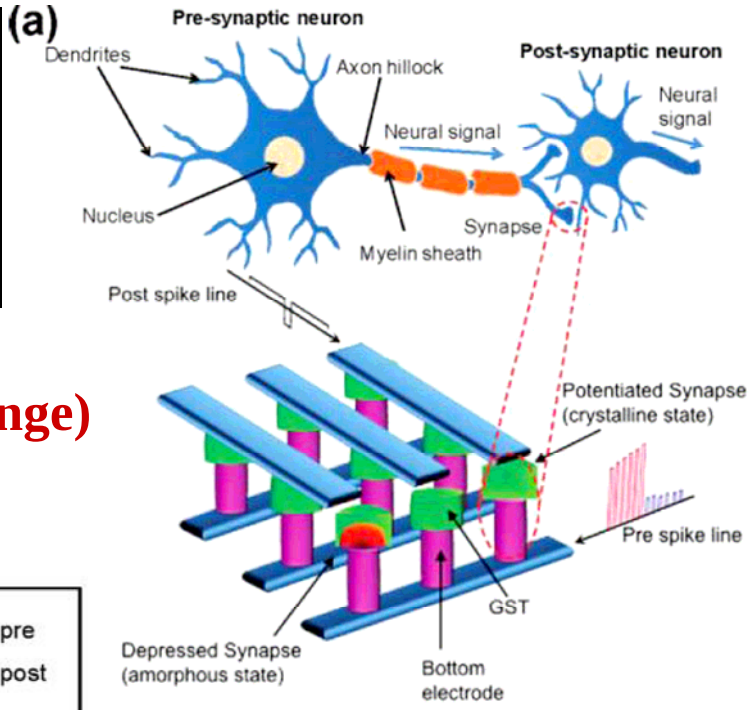


Short AND long term potentiation ! STDP ? Cyclability ?



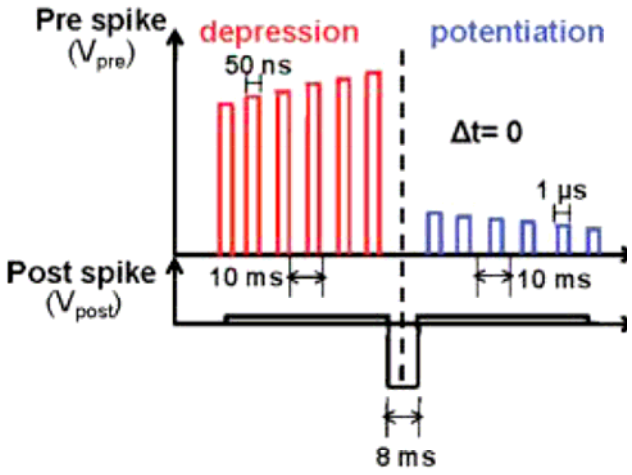
Resistive switching memristors

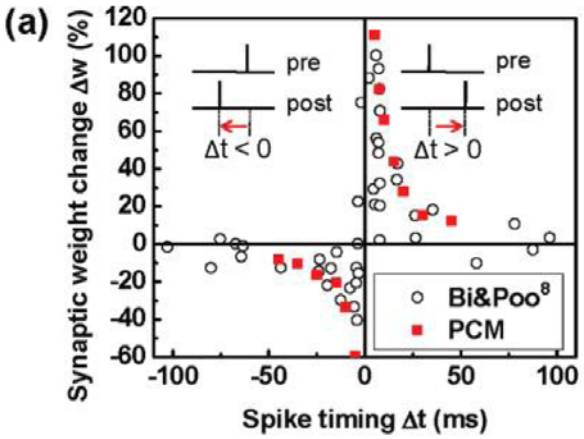




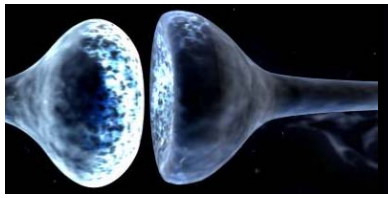
Kuzum et al., Nature Materials 2011 (Phase change)

see also : Wright et al., Advanced Materials 2011

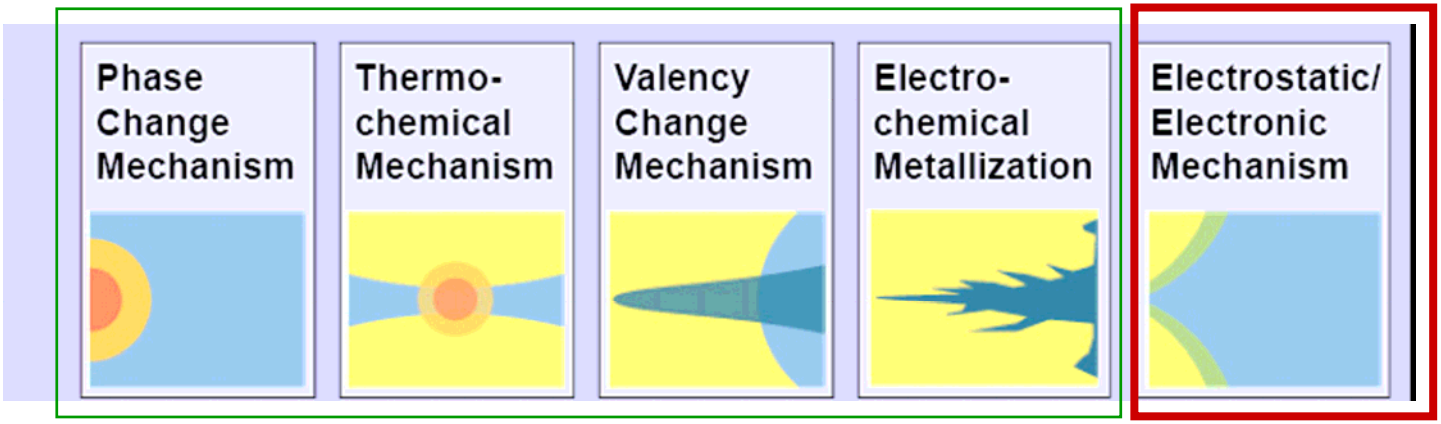




Phase change : unipolar switching. STDP = yes, complicated ?



Resistive switching memristors

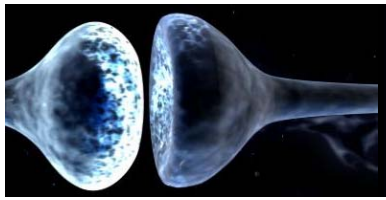


Waser *et al.*, Nature Materials 2007

- *defect-mediated : thermal effects, ionic motion*

- our work : **purely electronic resistive switching**

  1 example : "spintronic" memristor *WO 2010/ 142762 A1*



Spintronic memristor

A. Chanthbouala, J. Grollier, R. Matsumoto, V. Cros, A. Anane, A. V. Khvalkovskiy, A. Fert

Unité Mixte de Physique CNRS/Thales, France

K.A. Zvezdin

A.M. Prokhorov General Physics Institute of RAS, Russia
Istituto P.M. s.r.l., Italy

K. Nishimura, Y. Nagamine, H. Maehara, K. Tsunekawa

Process Development Center, Canon ANELVA Corporation, Japan

A. Fukushima, and S. Yuasa

National Institute of Advanced Industrial Science and Technology (AIST), Japan

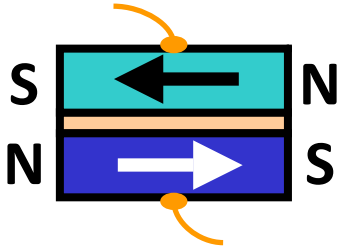
Magnetic Random Access Memory (MRAM)

MRAM building block = Magnetic Tunnel Junction

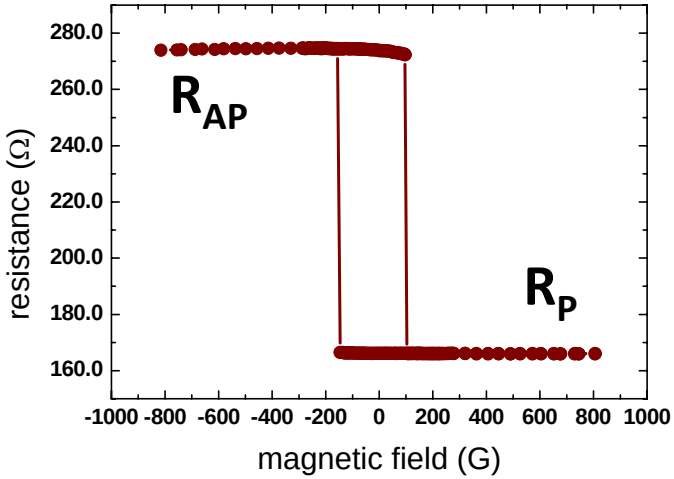
Magnetic metal/Insulator/Magnetic metal

Tunnel MagnetoResistance (TMR)

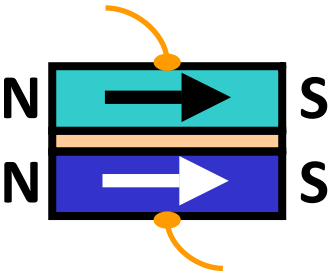
Anti-parallel state (AP)



R_{AP}



Parallel state (P)



R_P

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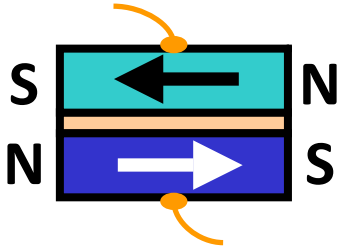
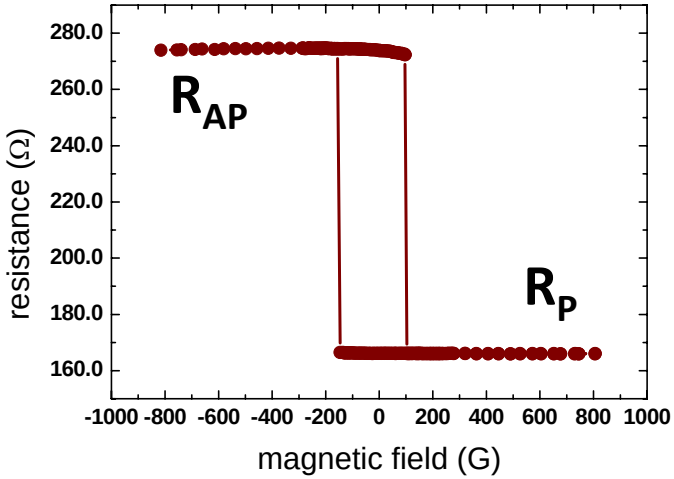
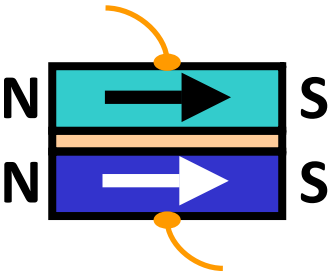


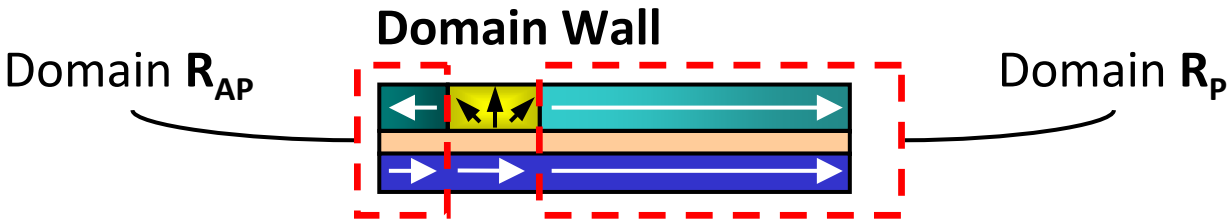
R_{AP}



Parallel state (P)



R_P



- Resistance: proportion of parallel and anti-parallel domains

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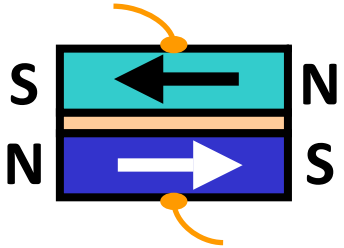
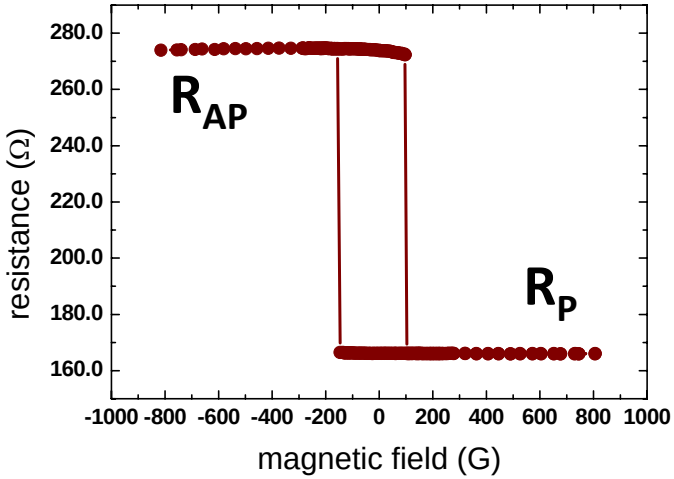
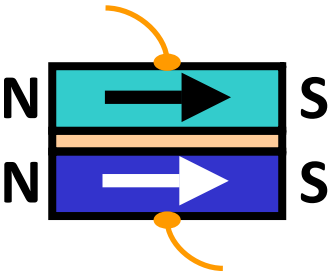


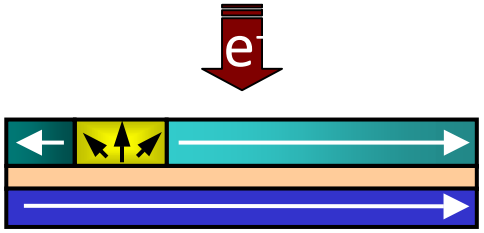
R_{AP}



Parallel state (P)



R_P



- Resistance variation: **Spin Transfer Torque (STT)**

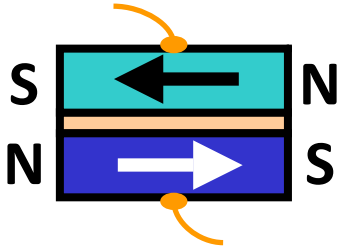
Magnetic Random Access Memory (MRAM)

MRAM building block = Magnetic Tunnel Junction

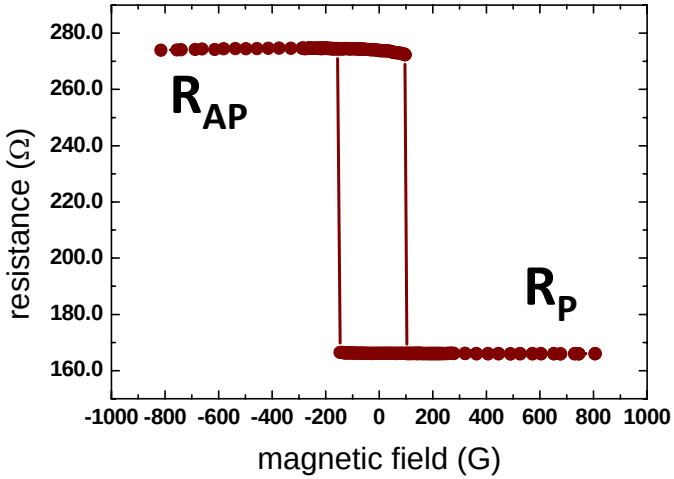
Magnetic metal/Insulator/Magnetic metal

Tunnel MagnetoResistance (TMR)

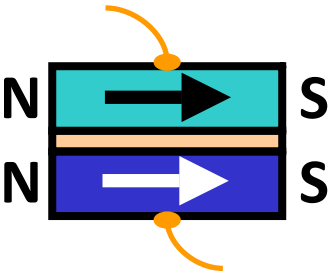
Anti-parallel state (AP)



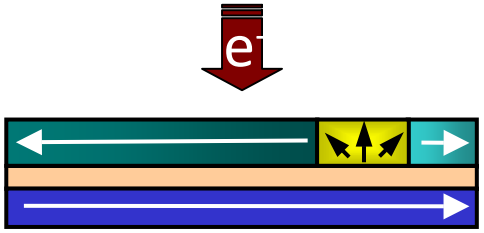
R_{AP}



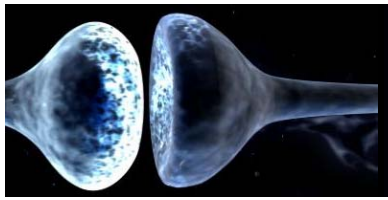
Parallel state (P)



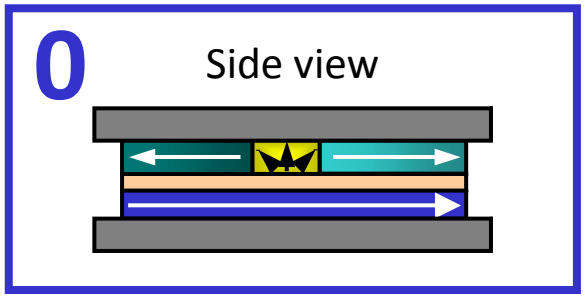
R_P

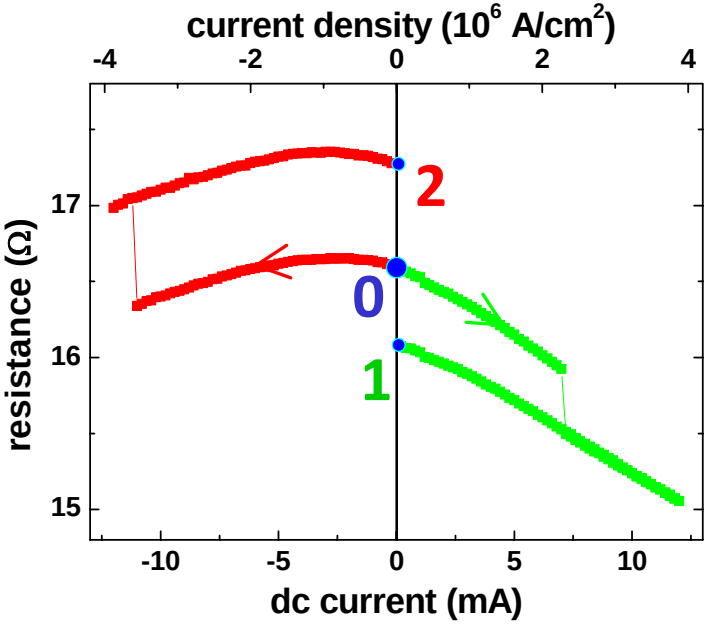


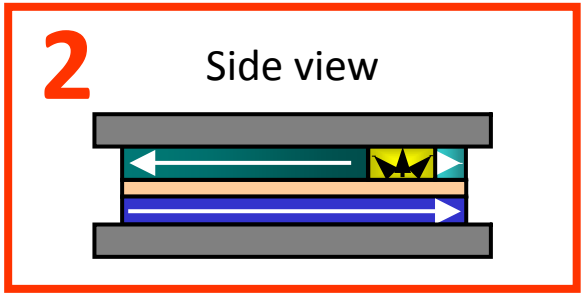
- Resistance variation: **Spin Transfer Torque (STT)**

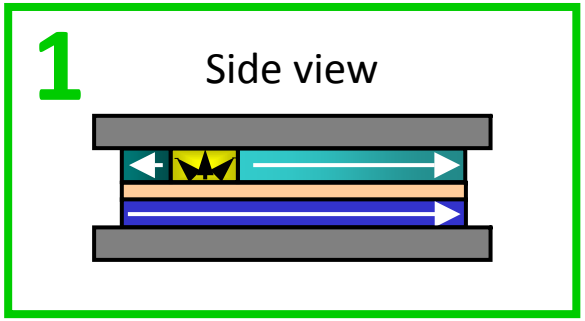


DW displacement by vertical DC current



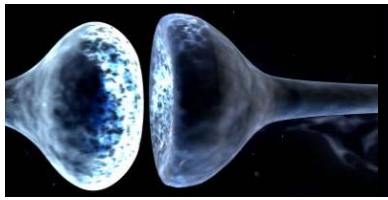






- **Bidirectionnal DW motion**
- Current densities lower than previous DW motion experiments

A. Chanthbouala *et al.*, Nature Phys., 2011



Concept of the spintronic memristor

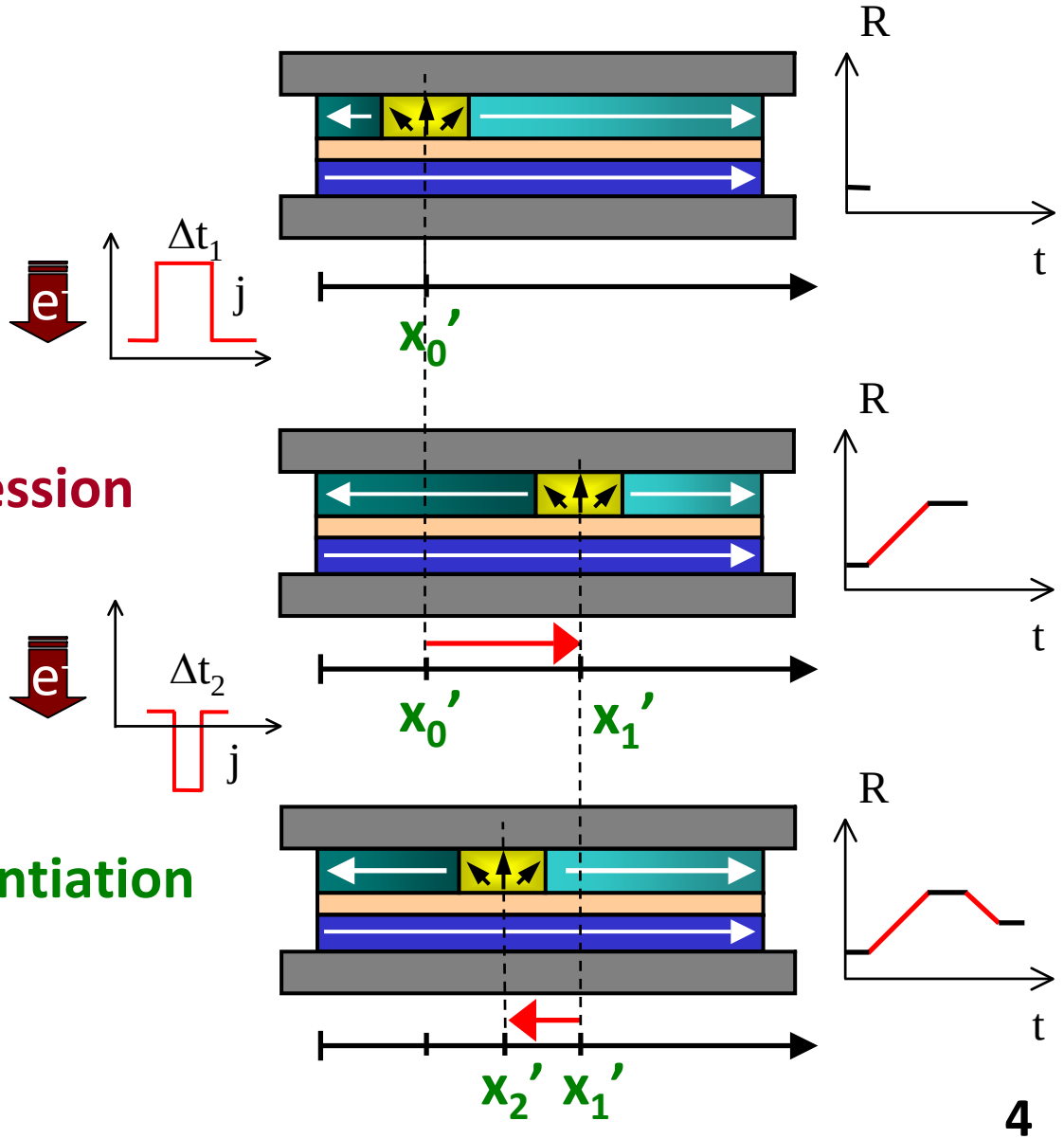
$$\Delta x \propto J\Delta t \propto q$$

- Resistance: DW position
- DW position: charge injected

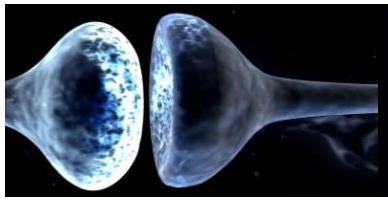
Positive current pulse: **Depression**

Negative current pulse: **Potentiation**

➢ **Synaptic weight**



Wang *et al.*, IEEE, 2009



Conclusion on the spintronic memristor

✓ Advantages

- Understanding of the underlying mechanisms: key to further improvements and **tuning of the synapse transfer function**

- **Fast**: sub-ns write process

- **Purely electronic effect**: high reliability and endurance

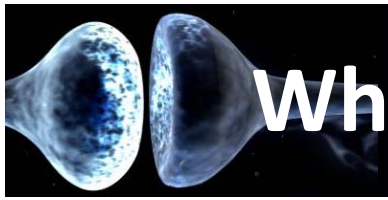
✗ Perspectives

- ON/OFF (R_{AP}/R_P) ratio now max = 6 ➔ **Theoretical limit 100**

- Connectivity: **perpendicularly magnetized materials**

➔ **Scalable below 50x100 nm**

International **T**echnology **R**oadmap for **S**emiconductors identified **Spin Transfer Torque-RAM** as one of the two most promising emerging memory devices: **Spintronic memristor will benefit from these developments**



Which memristor for which application ?

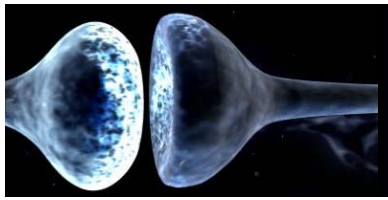
- **ITRS table for memory evaluation applicable ?**

		Baseline Devices					Prototypical Devices [A]			
		DRAM		SRAM [C]	Floating Gate [E]		Trapping Charge [G]	FeRAM	MRAM	PCM
		Stand-alone [A]	Embedded [C]		NOR	NAND				
Storage Mechanism		Charge on a capacitor		Inter-locked state of logic gates	Charge on floating gate		Charge trapped in gate insulator	Remnant polarization on a ferroelectric capacitor	Magnetization of ferromagnetic layer	Reversibly changing amorphous and crystalline phases
Cell Elements		1T1C		6T	1T		1T	1T1C	1(2)T1R	1T1R
Feature size F, nm	2007	68	90	65	90	90	65	180	90	65
	2022	12	25	13	18	18	10	65	22	18
Cell Area	2007	$6F^2$	$12F^2$	$140\ F^2$	$10\ F^2$	$5\ F^2$	$6F^2$	$22F^2$	$20F^2$	$4.8F^2$
	2022	$6F^2$	$12F^2$	$140\ F^2$	$10\ F^2$	$5\ F^2$	$5.5F^2$	$12F^2$	$16F^2$	$4.7F^2$
Read Time	2007	<10 ns	1 ns	0.3 ns	10 ns	50 ns	14 ns	45 ns [I]	20 ns [M]	60 ns [P]
	2022	<10 ns	0.2 ns	70 ps	2 ns	10 ns	2.5 ns	<20 ns [J]	<0.5 ns	< 60 ns
WE Time	2007	<10 ns	0.7 ns	0.3 ns	1 □s/ 10 ms	1/0.1ms	20□s/20ms[H]	10 ns [K]	20 ns [M]	50/120ns[P]
	2022	<10 ns	0.2 ns	70 ps	1 □s/ 10 ms	1 ms/ 0.1 ms	~10□s/10 ms	1 ns[J]	<0.5 ns [N]	<50 ns
Retention Time	2007	64 ms	64 ms	[D]	>10 y	> 10 y	>10 y	>10 y	>10 y	>10 y
	2022	64 ms	64 ms	[D]	>10 y	> 10 y	>10 y	>10 y	>10 y	>10 y
Write Cycles	2007	>3E16	>3E16	>3E16	>1E5	>1E5	1.00E+05	1.00E+14	>3E16	1.00E+08
	2022	>3E16	>3E16	>3E16	>1E5	>1E5	1.00E+06	>1E16	>1E16	1.00E+15
Write Operating Voltage (V)	2007	2.5	2.5	1.1	12	15	7–9	0.9–3.3	1.5 [M]	3 [P]
	2022	1.5	1.5	0.7	12	15	6-Apr	0.7–1	<1.5	<3
Read Operating Voltage (V)	2007	2	2	1.1	2	2	1.6	0.9–3.3	1.5 [M]	3
	2022	1.5	1.5	0.7	1.1	1.1	1.1	0.7–1	<1.8	<3
Write Energy (J/bit)	2007	5E-15 [B]	5.00E-15	7.00E-16	>1E-14 [F]	>1E-14 [F]	1E-13 [H]	3E-14 [L]	7E-11 [A]	5E-12 [Q]
	2022	2E-15 [B]	2.00E-15	2.00E-17	>1E-15 [F]	>1E-15 [F]	>1E-15	5E-15 [L]	2E-11 [A]	<1E-13 [Q]
Comments					Multiple-bit potential	Multiple-bit potential	Multiple-bit potential	Destructive read-out	Spin-polarized Write has a potential to lower Write current density and energy [O]	Multiple-bit potential

organic memristors ?

endurance/cyclability/low power consumption/OFF-ON ratio/small : yes

speed, retention time : ?



Memristors around the world

- **US** : 2009 DARPA “SyNAPSE” program

Systems of Neuromorphic Adaptive Plastic Scalable Electronics

define a new path forward for creating
useful, intelligent machines

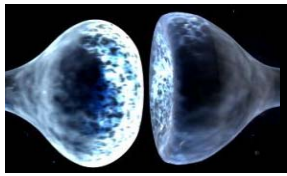
3 funded projects (~ *5 M$ each for the first phase*)

- Hewlett-Packard (*memristors*) - HRL labs (*memristors*) - IBM (*?)*

- **Europe** :

FP7 Nabab, FP7 Bion (ended)
ERC NanoBrain & ERC Femmes projects, Chist-Era PNEUMA

2 FET Flagship pilots : Guardian Angels & The Human Brain Project



Conclusion & perspectives

- State of the art memristor : exciting potential of memristor devices as artificial synapse

- spintronic memristor : resistance switching based on purely electronic effects

⇨ very promising : endurance, speed, power consumption

- Young topic : no demonstration yet of a cognitive chip based on memristors

- Dedicated architectures and programmation schemes to be developed

- Which type of memristor for which application ?

Prospects for graphene electronics

Jari Kinaret[1] and Daniel Neumaier[2]

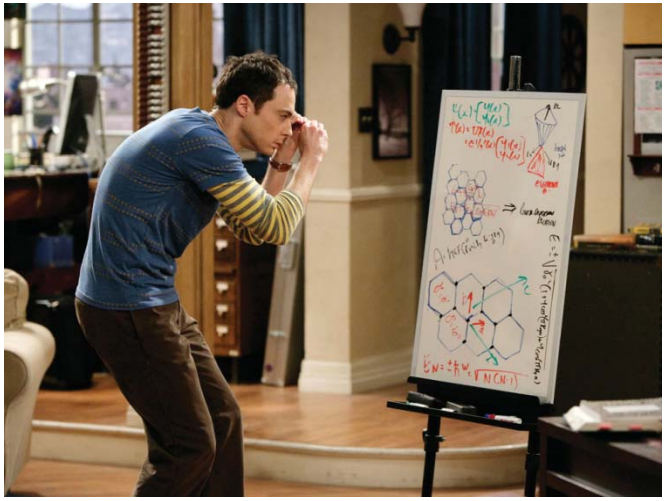
[1]Chalmers University of Technology, Sweden
[2]AMO GmbH, Germany

Graphene-based electronics

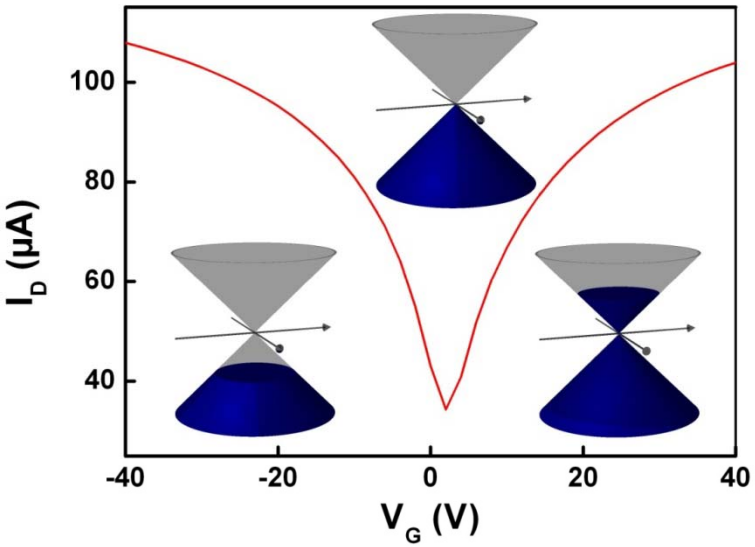
- At its infancy: *Si anno 1955*
- Not just graphene but also other two-dimensional materials (BN, MoS_2, $MoSe_2$, $NbSe_2$, Bi_2Te_3,…): *a whole new palette*

- Different aspects:
  - Pre-requisites: materials and device fabrication
  - Digital vs. analog
  - Consumer vs. high-performance
  - Integrated systems: optical, flexible
  - Novel components
- For recent reviews, see
  D. Reddy *et al*., J. Phys. D **44**, 313001 (2011);
  F. Schwierz, Nature Nanotechnology **5**, 487 (2010);
  S.K. Banarjee *et al*., Proc. IEEE **98**, 2032 (2010)

What's so special about graphene?

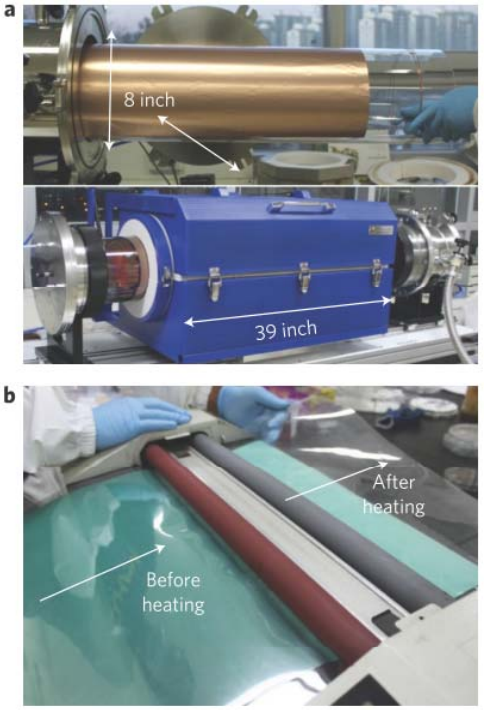


- Conducting (semi-metal: *ambipolar*)
- High carrier mobility (up to 200 000 cm^2/Vs, on substrate ~10 000 cm^2/Vs)
- Large saturation velocity (4 $x10^5$ m/s)
- High current-carrying capacity
- Linear dispersion relation (*Dirac fermions*)
- Ultimately thin
- Compatible with planar technology
- Optically transparent (absorption $\pi\alpha \approx 2.3$ %)
- Flexible and strong (100-300 stronger than steel)
- Best conductor of heat
- Chemically inert
- Biocompatible



Materials production

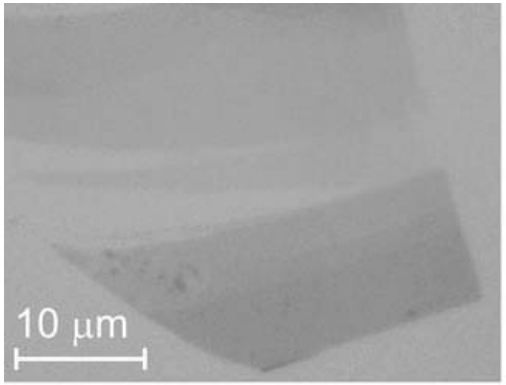
- Exfoliation
  - Mechanical: highest quality, not scalable
  - Chemical: mostly flakes, OK for many applications
  - Mobility up to 200 000 cm^2/Vs and higher (suspended)
- **CVD**
  - Scalable, transferable, rapidly developing
  - Usually on Cu but also other metals and insulators
  - Roll-to-roll production
  - Mobility up to 7 000 cm^2/Vs on SiO_2, 3x higher on h-BN (A. Venugopal et al., J. Appl. Phys. **109**, 104511 (2011))
- SiC sublimation
  - High electrical quality, expensive, not transferable
- Chemical synthesis
  - Atomistic control, placement issues similar to CNTs
- Exploratory techniques

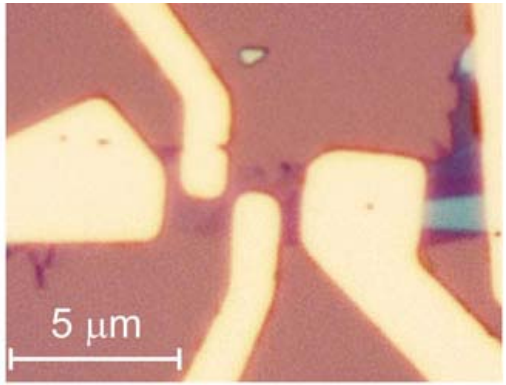


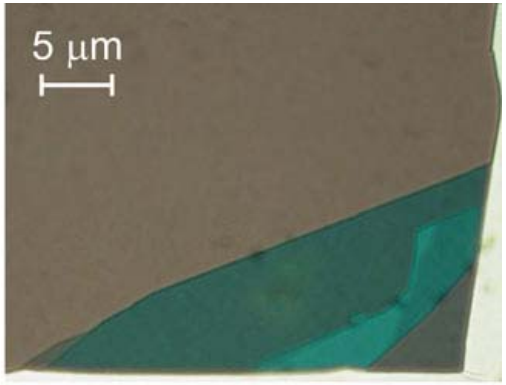
S. Bae et al. Nature Nano. 5, 571 (2010)

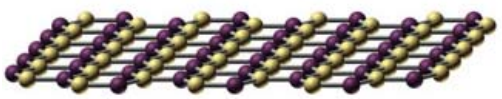
Other (mono-)layered materials

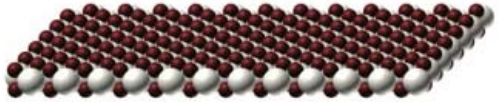
- Graphene is the first material in a palette of monolayers from layered materials

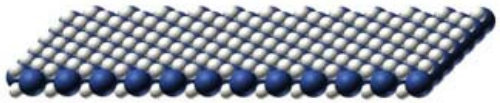












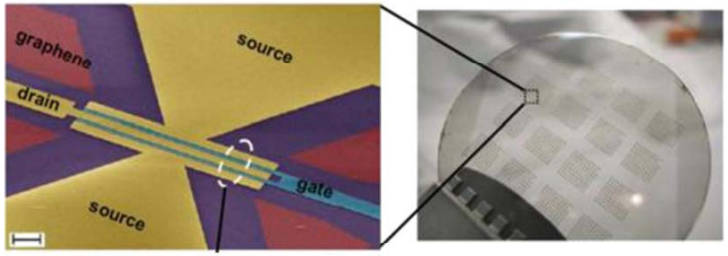
Hexagonal BN
Insulator

$NbSe_2$
semimetal

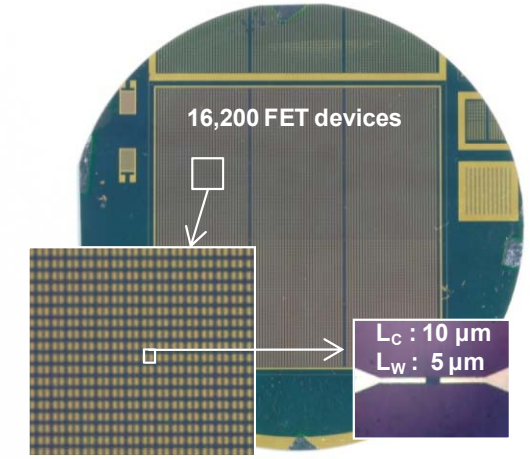
MoS_2
Direct-bandgap SC
(MoS_2 FET:
Nature Nano **6**, 147 (2011))

(K. Novoselov, Rev. Mod. Phys. **83**, 837 (2011))

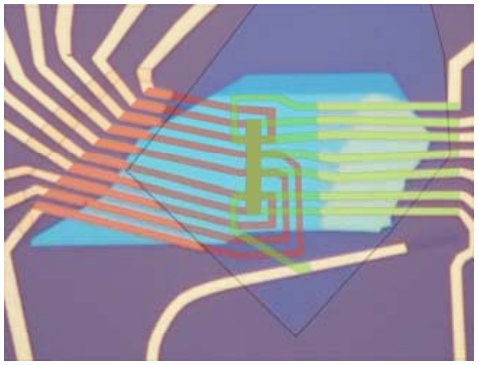
Device fabrication



- Planar technology:
  conventional lithography is applicable
  → integrable
- Sandwich structures G-BN-G
  (L.A. Ponomarenko et al., to appear in Nature Phys.)



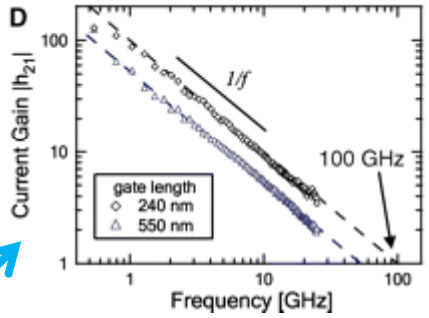
2 graphene layers,
individually contacted
and separated by 5 BN
layers
→ Coulomb drag etc.

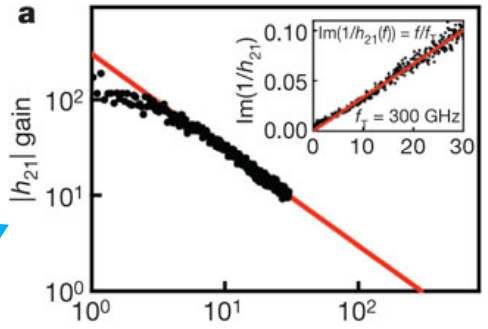


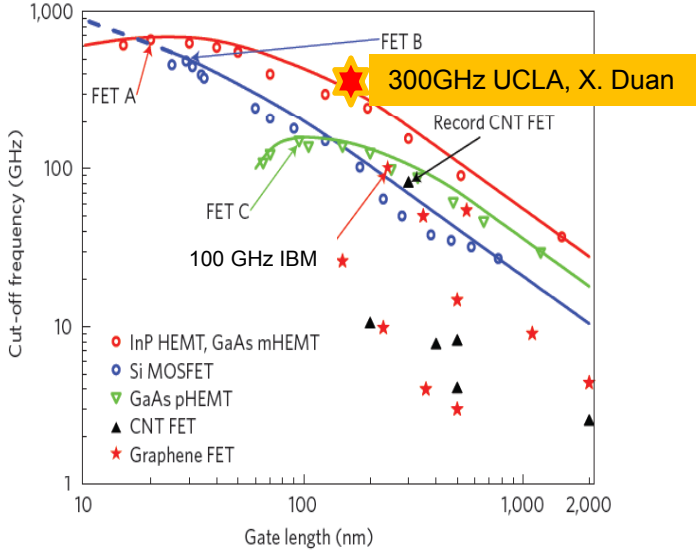
- Challenge is to use CVD or similar but without having to transfer!

Analog electronics

- High mobility and high saturation velocity give promise for fast electronics
- Extrapolated performance
  IBM: f_T = 100 GHz @ 240 nm;
  UCLA: f_T = 300 GHz @ 144 nm
- Poor power gain due to absence of a gap
- Ambipolar: new design feature that enables novel devices (Palacios)







(adapted from F. Schwierz)

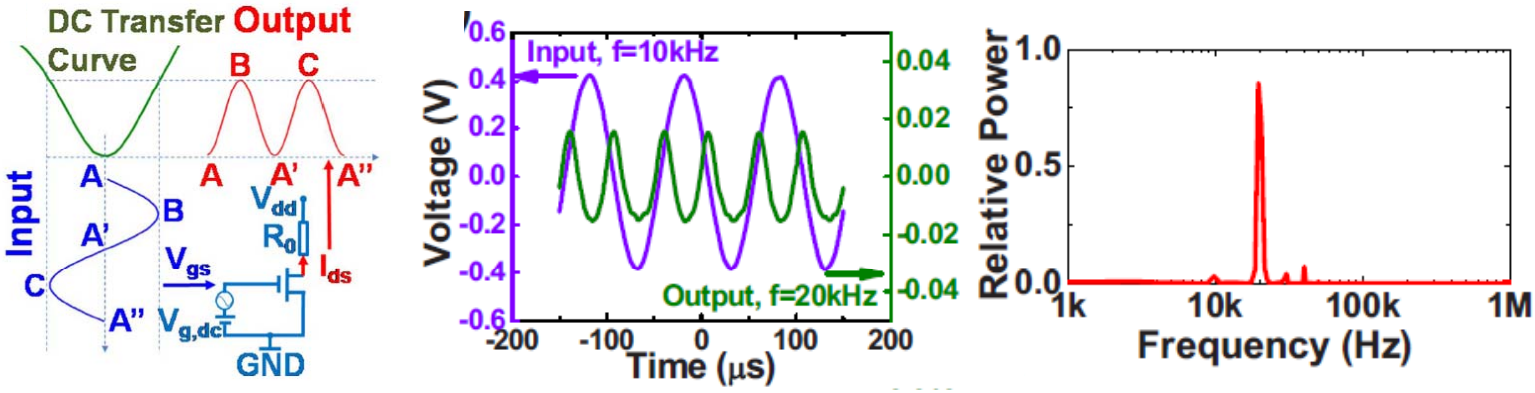
Comparison of graphene RF-transistors in terms of maximal transconductance g_m, minimal source-drain conductance g_0, and maximum power gain A

	Oxid (EOT)	**g_m max (mS/µm)**	**g_0 min (mS/µm)**	**A max**
IBM (SiC)	PHS/HfO_2 (17 nm)	0.15	0.4	<<1
IBM (CVD)	Al_2O_3 (10 nm)	0.04	0.2	<<1
UCLA (Exfoliated)	Al_2O_3 (8 nm)	1.2	2	<1
Columbia (BN)	BN (8 nm)	0.4	0.05 - 0.1	4 - 8
Columbia(pulsed)	PVA/HfO_2 (7nm)	0.5	0.1 - 0.2	2.5 - 5
AMO (E_G = zero)	Al_2O_3 (8nm)	0.12	0.02	6
AMO (E_G ~ 100meV)	Al_2O_3 (8nm)	0.12	0.002	60

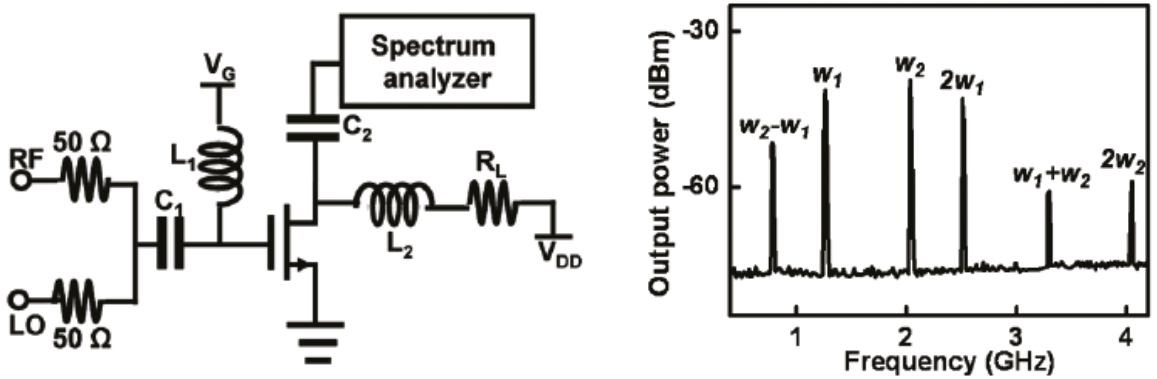
AMO unpublished

Exploiting ambipolarity for RF applications

Frequency doubling
(Z. Wang et al., APL **96**, 173104 (2010)



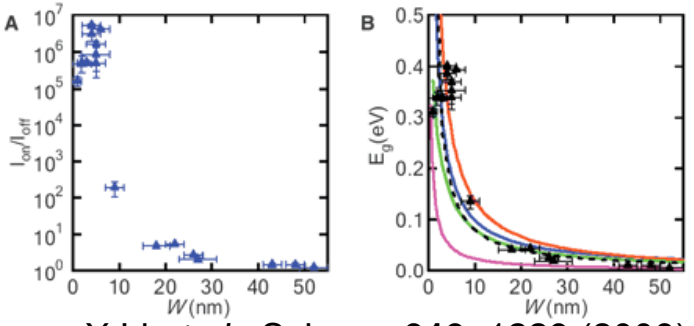
Mixer with one transistor
(L. Liao et al., Nano Lett, June 7, 2011)



Room for many more innovations!

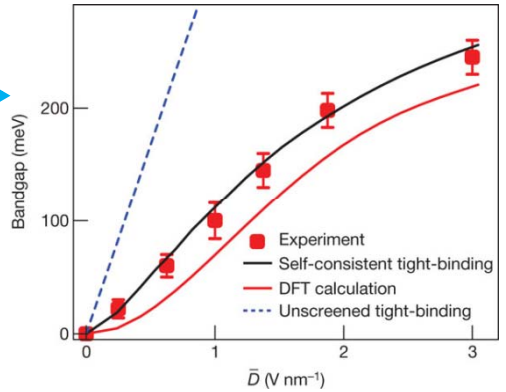
Digital electronics

- Challenge: absence of a band gap makes it hard to turn the devices off
- Old thinking: create a gap
  - Graphene nanoribbons (GNR)
    $E_g \approx 0.8$ eV nm/W
    - Lithographically: hard, need width 2-5 nm, good edges
    - Chemical synthesis: on metals, hard to position, no transport measurements exist yet
    - Unzipping of CNTs or synthesis inside a CNT



X.Li *et al.*, Science **319**, 1229 (2008)

  - Bilayer graphene with electric field: gap 100-200 meV, required V_{bg} ~100 V
  - Chemical modification (*e.g.*, nitrophenyl), gap 0.4 eV (S. Niyogi *et al.*, Nano Lett. **10**, 4061 (2010))

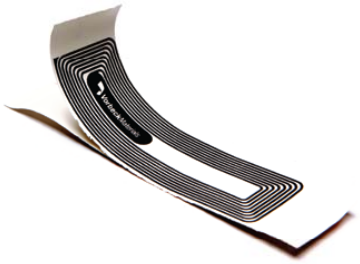


Y. Zhang *et al.*, Nature **459**, 820 (2009)

- New thinking: under research
  - BiSFET, tunnel FET, Veselago lens device: both BiSFET and tunnel FET are predicted to have very low switching energies, but they have not been demostrated experimentally

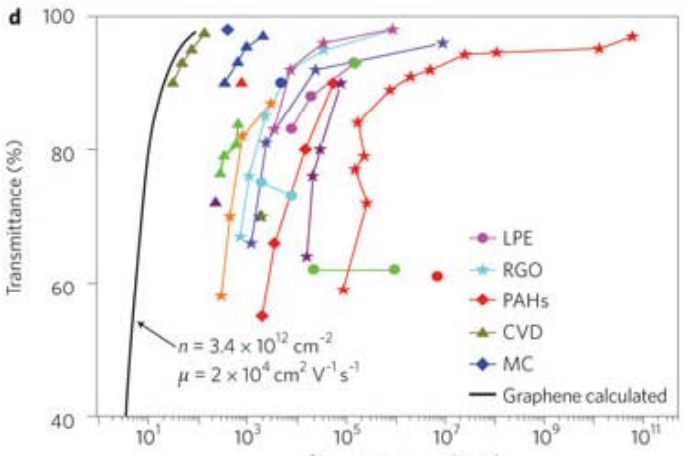
Consumer electronics

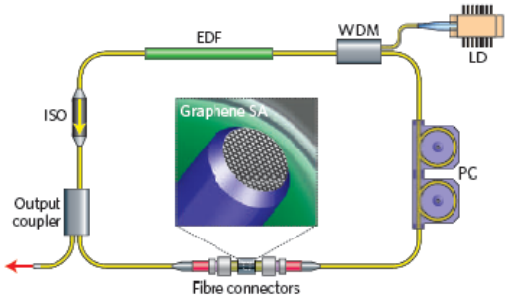
- Printable electronics
  - Thin film transistors with
    μ up to 100 cm^2/Vs (private information):
    no longer slow, still cheap
    → may capture some markets
    from conventional electronics
  - Approaching maturity:
    Vorbeck Materials conducting
    ink on market in 2012



Optoelectronics

- ITO replacement
  - In is a scarce resource with few suppliers
  - Sheet resistance and transparency OK
  - Samsung prototype AMOLED
- Fast lasers, photodetectors, modulators
  - Saturable absorbtion enables fast lasers with sub-ps pulses
  - Unique, universal wideband absorption can be exploited in photodetectors
  - *Etc*. – graphene photonics and plasmonics is one of the fastest growing research areas at the moment

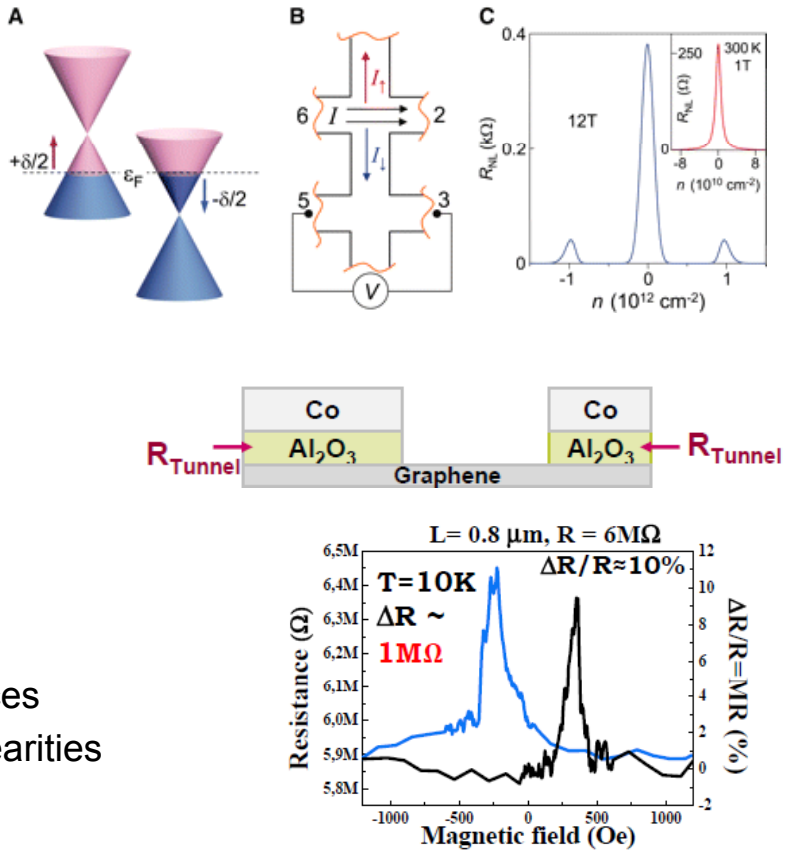




F. Bonaccorso et al. Nature Phot.. 4, 6111 (2010)

Beyond CMOS

- Spintronics:
  - large spin coherence lengths and pure spin currents (D.N. Ababnin et al., Science 332, 328 (2011))
  - large resistance signal for spin-dependent transport in spintronic logic devices (A. Fert, talk in Graphene2020, March 2011)
- NEMS:
  - low mass and large Young's modulus are promising advantages high frequency NEMS
  - larger area implies larger signals than for CNT-devices
  - possibility to shape and to sensitively control nonlinearities by tension yield new design freedoms



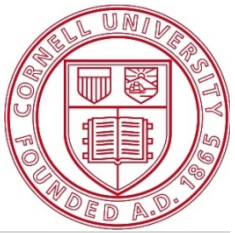
Benchmarking Beyond CMOS Devices

Technology	Graphene
Gain **Signal/Noise ratio** **Non-linearity**	Poor, would benefit from a gap
Speed **Power consumption**	High Low – high mobility, good gate coupling
Architecture/Integrability **(Inputs/outputs, digital, multilevel, analog, size etc.)**	Demonstrated integrability.
Other specific properties	System level integration - multifunctional
Manufacturability **(Fabrication processes needed, tolerances etc.)**	Mostly OK, except for ribbon fabrication Challenges in transferless fabrication
Timeline **(When exploitable or when foreseen in production)**	Optical and printable first (~2 years). Analog a few years later. Digital last. Non-standard devices (BiSFET etc.) not demonstrated yet.

Design For Beyond CMOS

Sandip Tiwari
st222@cornell.edu

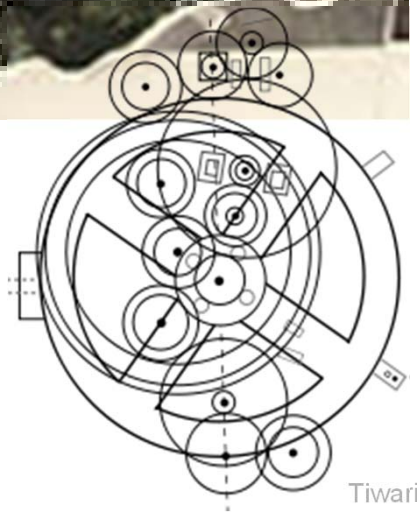
The design process can not be considered effective and successful if
it needs PhD level experts,
or doesn't work robustly,
doesn't produce working products within spec's in first spin,
and is not open for new research breakthroughs that may be useful in technology applications.



Acknowledgements: Collaborators, students, peers, funders (NSF, DARPA, Mellowes Endowment, Hosts), ...

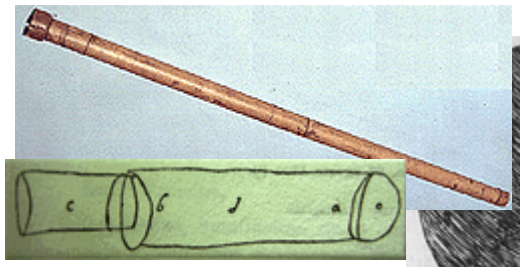
Design is Central to Good Engineering

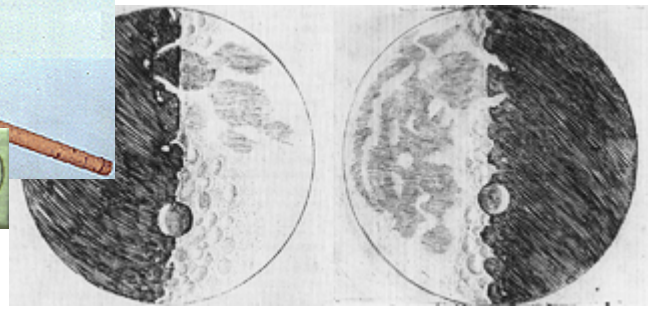
Analog Computing circa 200 BC:
Antikythera mechanism



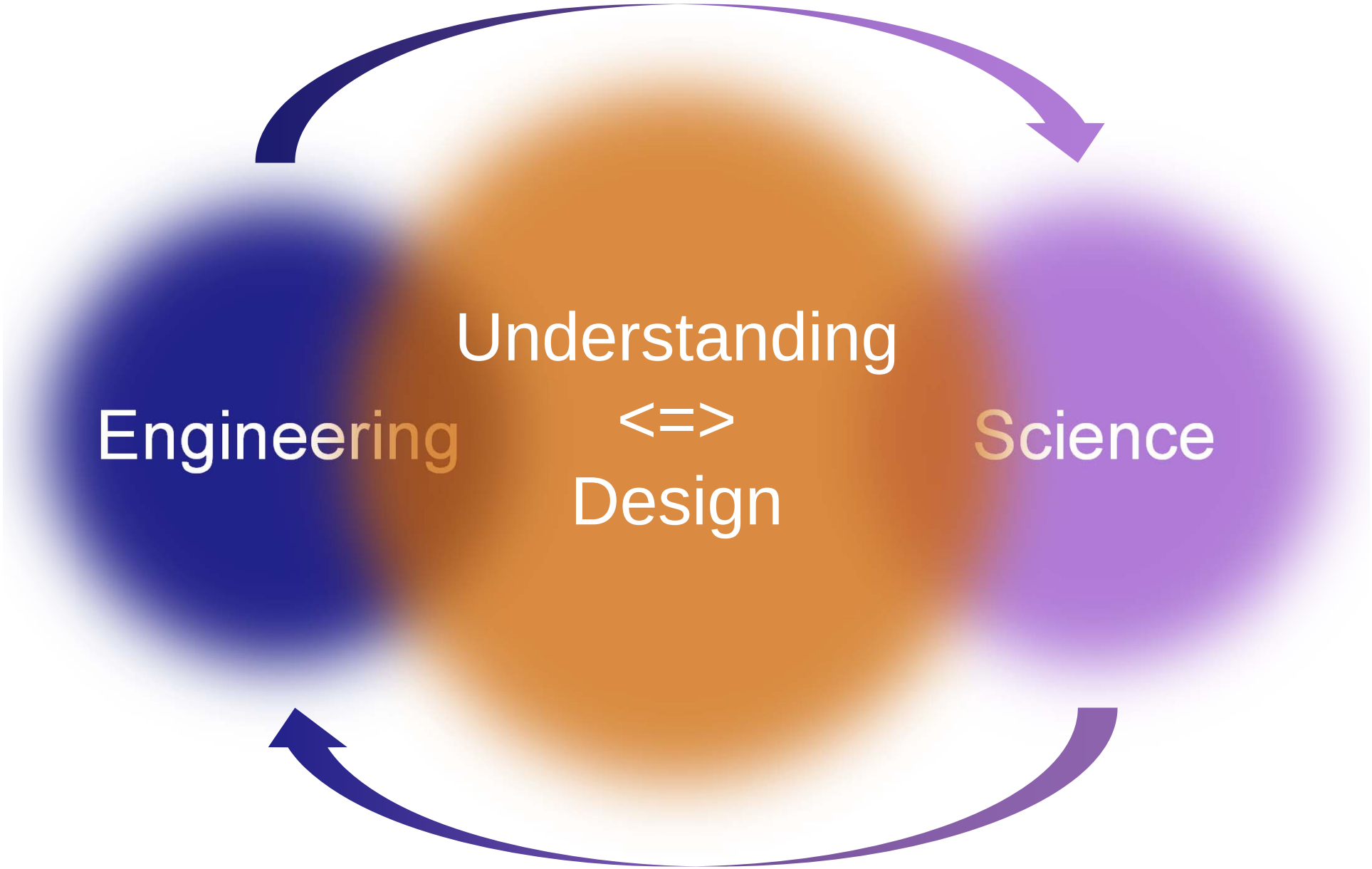
The Modern Era:
Copernicus, …

Galileo





phases of moon



Good Engineering => Good Tools => New Science => New Engineering => New Tools =>

So, what do we do today?

Digital World

High performance microprocessors:

Trillion transistors
hundreds of tools (layout, timing, process, models, noise, power, DRC, LVS, Yield, verification, …)
hundreds of people
2-3 years
hundreds of milllion$'s

Embedded :

Sub-trillion transistors
hundreds of tools (layout, timing, models, noise, power, DRC, LVS, Yield, verification, …)
IP,
10's of people
1-2 years
10's of million$'s

We usually get it right first time around

Analog/Mixed-Signal/RF World

Million transistors
Even more tools
Small-signal, parasitics, tlines, large signal, cross-talk, …

With enough resources, we can design for digital with trillion transistors,

but,

can't design with million transistors.

The objective of design *is* that non-specialists, with sufficient training, e.g., BS/MS, can design without knowing details of technology and everything else, so that designs can function in first pass with reliability and robustness.

This allows many designers (x100 or more) to take advantage of the costly technology infrastructure towards societal benefit. The technology costs are thus amortized.

The design approaches should also balance efficiencies and effectiveness.

And be open to new science breakthroughts

Problems with Current Microelectronics Infrastructure

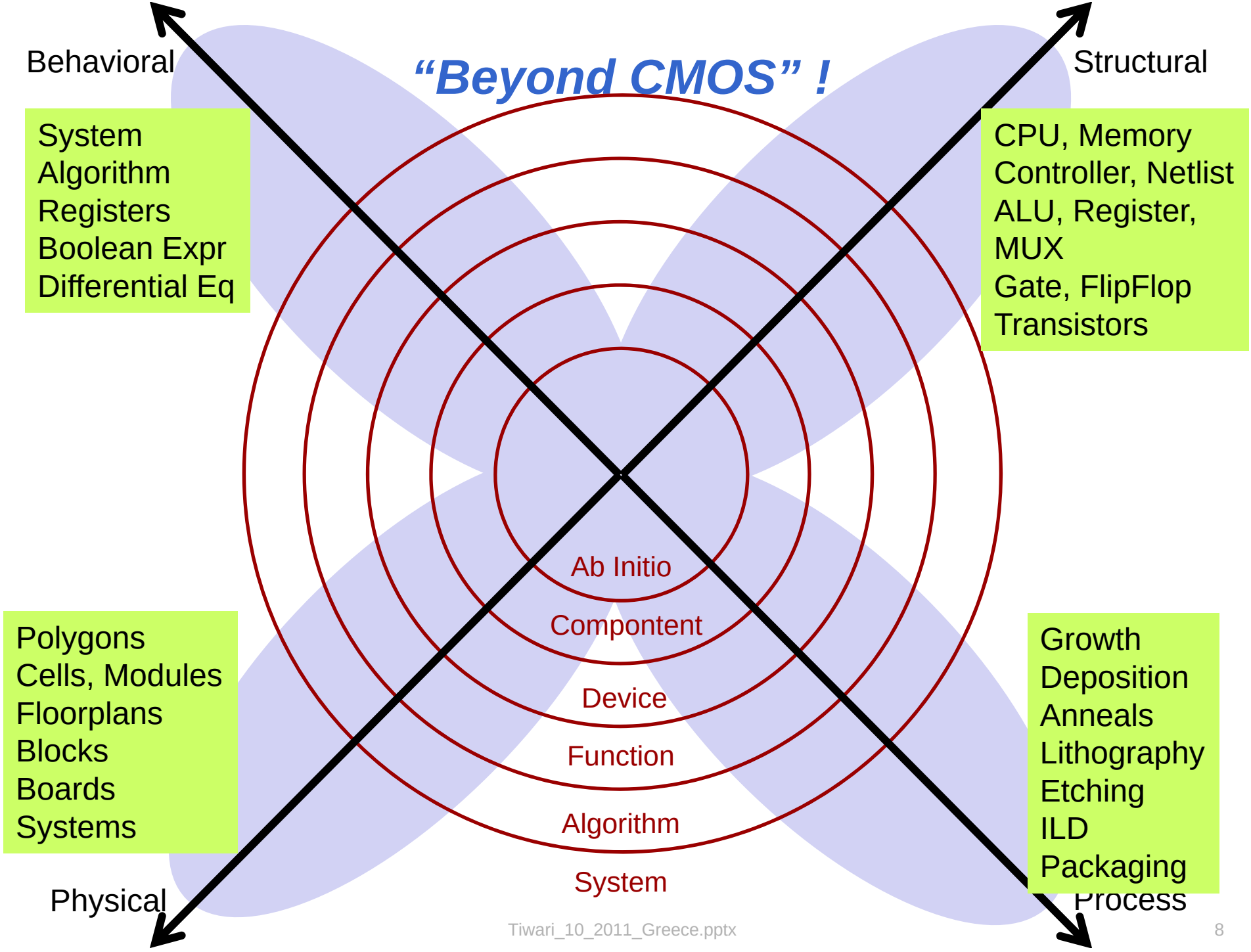
- Designed for digital quasi-static
  - Process models – layout – 2D device – compact model for quasistatic with layout, snm, thermal, noise, statistics, ..
  - Corners for all variations
  - Designed for worst cases
  - Inefficient
- Stochasticity is intrinsic at nanoscale; it is not just a threshold variation
- Quasistatic approaches brake for high frequency
  - In-plane effects– lateral diffusions, capacitances, … parasitics
  - Small-signal effects. …
- New technologies are very difficult to incorporate.
- Every change, e.g., 3D, is a kluged tool to be repeatedly used with base.

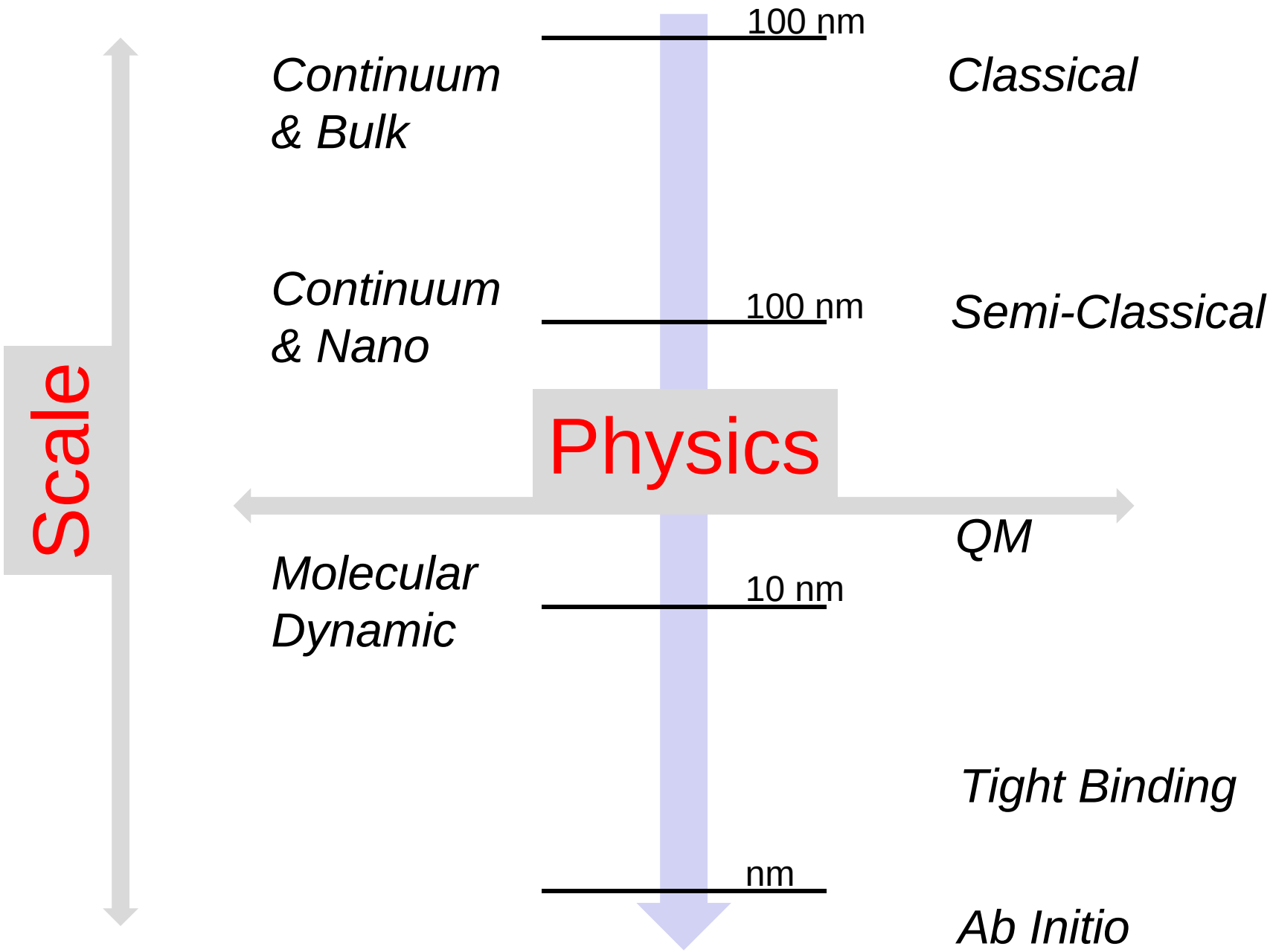
And, the problems beyond?

- Signals are not just I, Q and V in t.
- New signal modalities and their transformations.
- Corners at nanoscale? Stochasticity is intrinsic.
- Heterogeneous integration.
- 2D – 3D
- Abstractions across scales

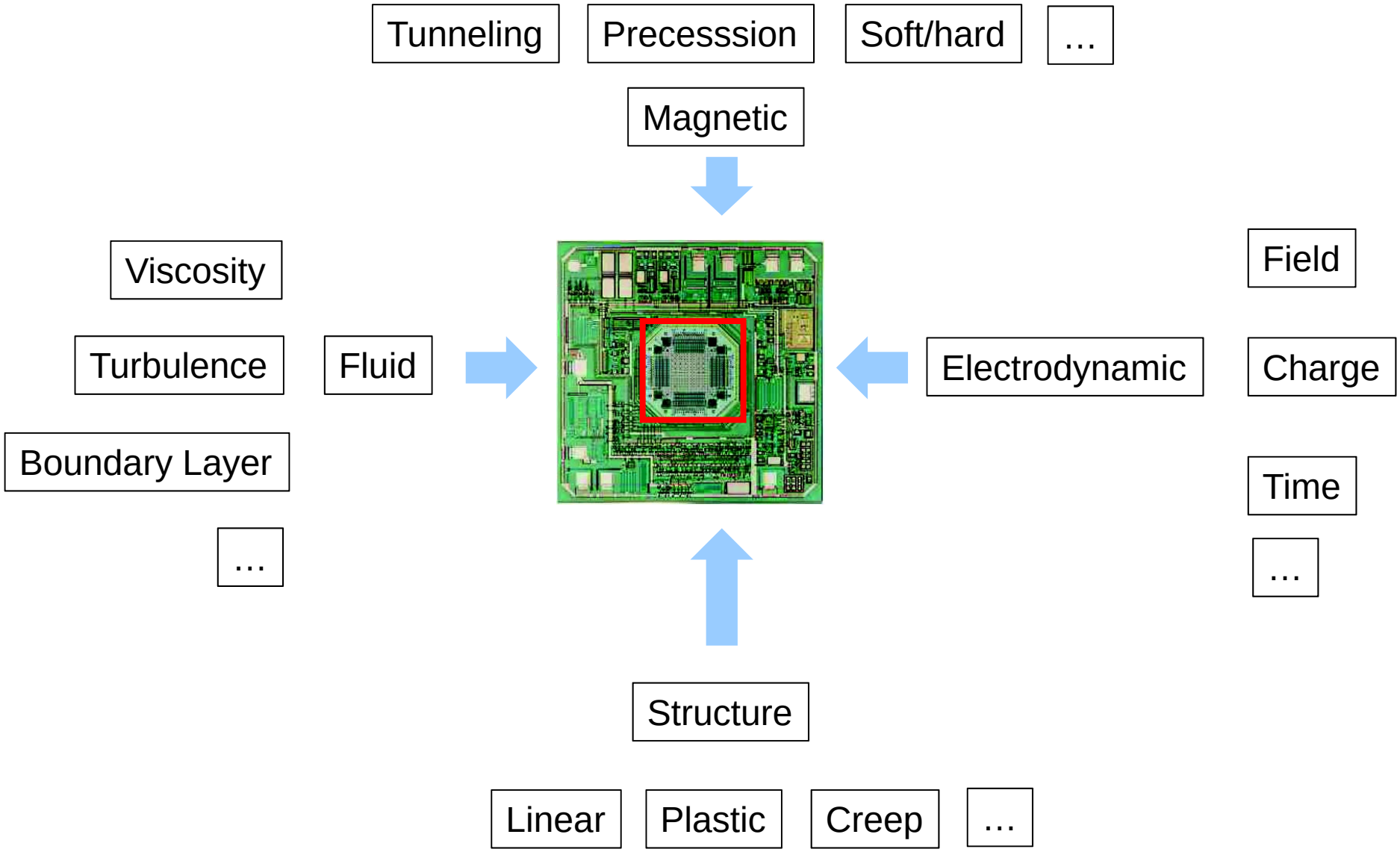
Consequences

- We don’t really know how to judge what works and what doesn’t work?
- What is robust and what is not?
- What energy and power in changing signals?
- What are process technology interactions and effects?
- Thermal, Temporal,

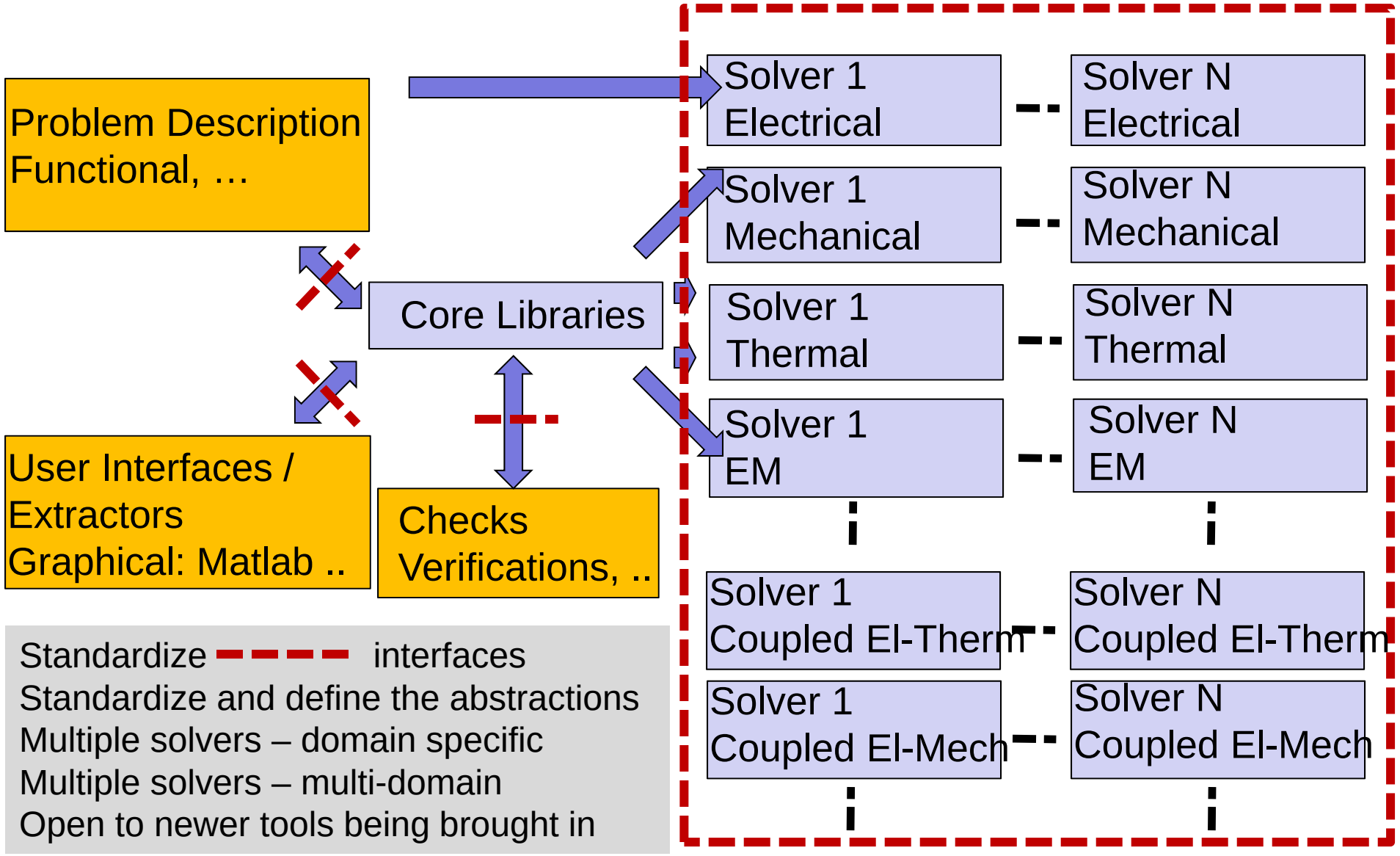

Behavioral
"Beyond CMOS" !
Structural
System
Algorithm
Registers
Boolean Expr
Differential Eq
CPU, Memory
Controller, Netlist
ALU, Register,
MUX
Gate, FlipFlop
Transistors
Ab Initio
Compontent
Device
Function
Algorithm
System
Polygons
Cells, Modules
Floorplans
Blocks
Boards
Systems
Growth
Deposition
Anneals
Lithography
Etching
ILD
Packaging
Physical
Process


Scale
Physics
100 nm
Continuum
& Bulk
Classical
Continuum
& Nano
100 nm
Semi-Classical
QM
Molecular
Dynamic
10 nm
Tight Binding
nm
Ab Initio

An Example: Fluid-Magnetic-Electric-Mechanical



Build A New Open Infrastructure



Standardize ▬ ▬ ▬ interfaces
Standardize and define the abstractions
Multiple solvers – domain specific
Multiple solvers – multi-domain
Open to newer tools being brought in

BENCHMARKING BEYOND CMOS DEVICES

D.VERKEST

imec

BENCHMARKING BEYOND CMOS DEVICES

imec

CMOS SCALING:THE BAD

Switching heat/cm^2 ~ $(V_{DD}/\lambda)^3$ → V_{DD} ↓

Leakage Power ~ $\exp(-mV_T/kT)$ → V_T ↑

Clock $F_{cl} \sim I_{on}/V_{DD} \sim \mu(V_{DD} - V_T)^{0.5}/\lambda$ → Clash

Device variability $\sigma V_T \sim 1/\lambda$ → σF_{cl}

Interconnect RC delay

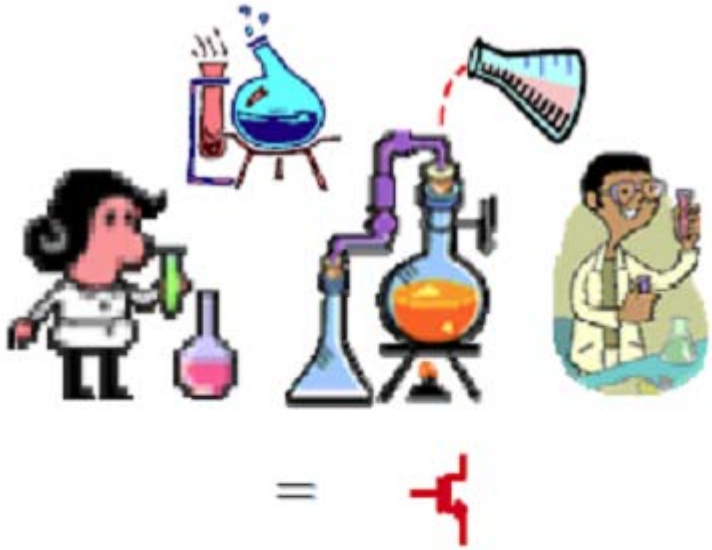
CMOS SCALING: THE GOOD

- "Zero" static power: symmetric n and p FET
- Simple (planar) layout strategy (litho compatible)
- Symmetric I/V → bidirectional switch
- Gain: signal restoration, noise margin, RF and analog
- W/L sizing → Fanout 1 ... 10^6
- Connectable by 10+ wiring layers
- Low manufacturing cost: < 1 n$/transistor
- Design technology and IP libraries
- Versatile: logic, storage, interconnect, I/O, analog, ...

→ **complete System**-on-Chip

BENCHMARKING BEYOND CMOS DEVICES

Beyond CMOS device inventor



Hey, here's a *great* new device …

- It's really cool! It looks useful!
- We actually made one! It worked!

SYSTEMABILITY

The CMOS designer

… but I can't do ***design*** with them

- I don't understand them.
- You can't characterize them, model them, simulate them, make them in volume, . . .

Source: W. Joyner, IBM

SYSTEMABILITY

The ability to economically design and manufacture reliable systems from the interaction of devices fabricated in a given technology.

SYSTEM = COMPUTATION, STORAGE, INTERCONNECT, I/O, (ANALOG)

Every contender

- Must add value to one or more of the 4 system functions and be compatible with the others
- All-in throughput/Watt and/or transactions/Joule must beat CMOS at time of manufacturing at equivalent or lower cost
- System level manufacturability, reliability, testability must beat ultimate CMOS solutions
- Room temperature operation is mandatory
- Device variability must be mitigated and modeled and cost efficient error resilient design solutions must be available
- Design methods and tools must be in place supporting design from device to system. Design tool development time is 3x technology development time.

BENCHMARKING BEYOND CMOS DEVICES

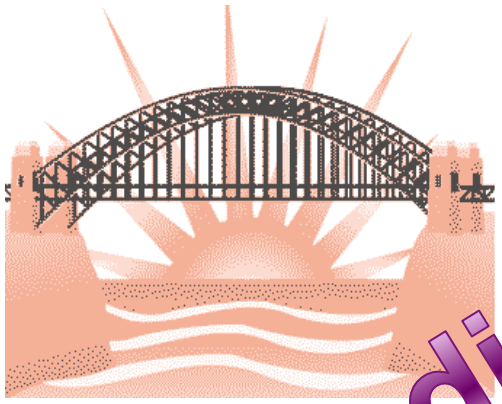
Beyond CMOS device inventor

Hey, here's a *great* new device …

- It's really cool! It looks useful!
- We actually made one! It worked!

Pathfinding

The CMOS designer

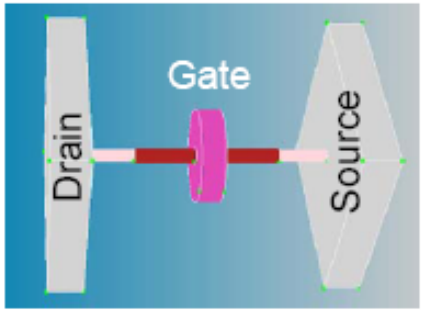


… but I can't do ***design*** with them

- I don't understand them.
- You can't characterize them, model them, simulate them, make them in volume, . . .

Source: W. Joyner, IBM

IMEC INSITE PATHFINDING INITIATIVE
LINKING PROCESSES, DEVICES, CIRCUITS, SYSTEMS



Architecture + models (TCAD)

Simplified circuit models

SlewAxis = [12.5 125 250 625 1250] ps

TDELAY (ns) =
[0.006254 0.015746 0.031686 0.068524 0.164307
0.019463 0.032747 0.050290 0.089016 0.185832
0.028944 0.046620 0.067449 0.107620 0.207008
0.045504 0.069108 0.096166 0.138539 0.246567
0.068189 0.122788 0.162575 0.229775 0.355785] ;

TTRANS (ns) =
[0.011796 0.037772 0.081873 0.184887 0.461113
0.021729 0.045990 0.087022 0.189108 0.463147
0.031871 0.057616 0.098460 0.198298 0.470681
0.047394 0.079744 0.122761 0.208534 0.484796
0.087580 0.131710 0.187365 0.291257 0.545080] ;

LoadAxis = [1 50 100 200 500] pF

Digital speed

Layout Strategy!!!

Place/route incl. interconnect

SNM
WM
I_{read}
I_{cell}
I_{BL}

MC

Yield (V_{dd})

Statistics: $\sigma_{\Delta Vt}$, $\sigma_{\Delta\beta}$

BENCHMARKING BEYOND CMOS DEVICES

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BENCHMARKING BEYOND CMOS DEVICES

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NANO-TEC: https://www.fp7-nanotec.eu/

CORDIS FP7 ICT new NANO-TEC partners:
http://cordis.europa.eu/fp7/ict/newsroom/home_en.html

NANO-TEC partners:

Catalan Institute of Nanotechnology: www.icn.cat

VTT Technical Research Centre of Finland: http://www.vtt.fi/

Edacentrum GmbH: http://www.edacentrum.de/index_js.html

Chalmers University of Technology: http://www.chalmers.se/en/

Institute for Electron Technology: http://www.ite.waw.pl

Delft University of Technology: http://www.tudelft.nl/

Forschungszentrum Jülich GmbH: www.fz-juelich.de

National Centre for Scientific Research: www.demokritos.gr

University College Cork, National University of Ireland: www.ucc.ie

École Politecnique Fédérale de Lausanne: www.epfl.ch

Laboratoire d'Analyse et d'Architecture des Systèmes: http://www.laas.fr/

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