# Bridging Technology and Design in More than Moore

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### Outline

- Evading Moore's Law
- From 2D IC to 3D Extended CMOS
- Novel functionality enabled by 3D integration:
  - RF MEMS
  - TSV for RF applications
  - 3D integrated devices
  - Sensing
  - CNT
  - Silicon nanowires
  - Optics
  - Energy harvesting

### **3D Extended CMOS**



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### SoC vs. SiP

	DSP Passive (R, L, C) Embedded passive Memory CPU		
System on Chip (SoC)	System in Package (SiP)		
Conventional CMOS integration "More Moore"	Heterogeneous integration "More than Moore"		
<ul> <li>✓ Advanced integration based on the size reduction</li> <li>✓ Cost reduction</li> </ul>	<ul> <li>✓ Flexiblility</li> <li>✓ More functionalities</li> <li>✓ High density</li> </ul>		
× Technological compatibility	× Complex design of system, circuit, package and board designers		
Digital, analog, mixed signal into a single chip → Planar or stacked	CMOS, RFICs, MEMS, Optics, Energy in a single package → Wire bonding and flip chip		

### **3D IC stacked with TSVs**

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# System on System (SoS)

Each die can be designed and fabricated with dedicated and optimized technology to efficiently:

- Enhance the performance of SoS
- Optimize individual functions within SoS
- Reduce SoS power consumption



S.-J. Lee, IEEE SOC Conf 2009

# **Heterogeneous Functionality**

### 1) RF MEMS

Beam steering concept for complex WSN

□ 3D integrated inductors for RF tunable filters

□ Planar filters and UWB tunable LNA

2) Sensing

□ CNT sensing

□ Si nanowires sensing

3) Optics

□ Opto-electronic and Photonics

4) Energy scavenging

# **Heterogeneous Blocks for 3D**

### Heterogeneous integration components:

- MEMS & RF transmitter
- Sensors (image, acceleration, pressure, bio, etc)
- Optics (photonics)
- Energy Scavenging
- Memories
- Logic circuits
- Processor
- Power ICs



# **3D Heterogeneous Integration**

New application specific technologies for heterogeneous integration of complex advanced microsystems

- 3D integrated antenna and RF MEMS
- Sophisticated new nanosensor systems
   Highly reliable and robust 3D processes
   Fragile mechanical structures in MEMS/NEMS
   Stress induced by TSV and bonding system
- Efficient system design support Architectural design of heterogeneous systems Tool set to predict functionality (incl. test devices)



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### **Wireless Sensor Networks**

Specific optimized 3D-technologies for the integration of the different sub-modules (MEMS, ICs, memories, antennas and power modules)



e-CUBES concept for space applications (sensor node or satellite) with multifunctional layers

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# **3D Integrated Antenna & RF MEMS**

### Antenna array prototype test chip

- 2 PCB laminated of different thicknesses to accommodate the Si core (300 mm).
- PCB board designed to measured the chip connecting by wire bonding the RF signal and the DC biasing signals



M. Fernández-Bolaños et al., Microelectron. Eng., 2010.

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# **3D Integrated Antenna & RF MEMS**

### Future RF MEMS on TSV with 3D vertical interconnections



Antenna-Phase Shifter 3D Integration for beam steering applications







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### **Other 3D Integrated RF MEMS Examples**

### Ku band miniaturized bandpass filter using TSVs



J. Zhu et al., Microsyst. Technol. (2010) 16:1045-1049

RF MEMS heterogeneous chip integration with Au-Au thermocompressive bumpless interconnections



T.-Y. Chao et al., IEEE Trans. on Electron Devices, v. 57 (2010)

### **Nanotube Gas Sensors**

#### • Molecular detection:

- Current and Vt modulation (SWCNT FET)



C. Hierold, ETH Zurich

### • Conductance sensing (Si nanowire)



F. Patolsky, Materials Today 2005

#### • Gas detection:

- Capacitive & conductance sensing (capacitive CNT arrays)



### $\circ$ Mass sensing (NEM resonator)

NEMS Array	Cal Tech (Zeptogram Microresonators)		Achievement 8/25/07
2222222	ing or	Mass Responsivity	5 Hz/ag
3 <del>33333</del> 3	Chemisorb Resonato	Mass Resolution	~10 <sup>-19</sup> g (100 zg)
		Operating Pressure	1 atm (760 torr)
	Detector Response Time		< 20 ms
	No. of Sensor Elements		25,000
	Power Consumption		~100 mW
	Size		< 1 cm <sup>3</sup>

Y. T. Yang, Nano Lett 2006

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# **CNTS Arrays on TSV wafer**

- Vertical and horizontal aligned CNTs during the same synthesis
- Horizontal alignment in the gas flow direction
- Similar density for vertical and horizontal CNT mats (1012 tubes/cm2)









A. Arun EPFL PhD thesis, 2010

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# **CNT Arrays for Gas Sensing**

#### • Horizontal and on-site growth of CNT arrays by CVD :

- CNT growth initiated perpendicularly to catalyst surface



- Material selective CNT growth



#### • Selective gas detection through CNT functionalization and multiple readouts:



H.Guerin et al., 37th International Conference on Micro & Nano Engineering MNE 2011

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# **SWNTs on CMOS**



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# Capacitor: CNT on metal (TiN & AI)



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### **Negative Capacitance MOSFET**

#### **Novel Ferroelectric Transistor**

- Internal voltage amplification due to negative capacitance in Fe-FETs
- Experimental demonstration of the subthreshold swing below 60mV/dec



TEM picture of the gate stack

A. Rusu, G.A. Salvatore, D. Jiménez, A.M. Ionescu, Metal-Ferroelectric-Metal-Oxide-Semiconductor Field Effect Transistor with Sub-60mV/ decade Subthreshold Swing and Internal Voltage Amplification, IEDM 2010, San Francisco, December 2010

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## **Strained NWs as CMOS boosters**

Suspended Si nanowires for innovative stress-based nanoelectronic applications

- Elastic local buckling as CMOS booster: **1.2-5.6 GPa** on a single wafer
- Deeply scaled Si nanowire MOSFETs by stress-limited oxidation (~4 nm cross-section)
- ALD high-k/metal-gate stack: strain engineering and EOT scaling



Ultra-strained array of GAA Si NWs (~5.6 GPa), M. Najmzadeh, IEEE ISDRS 2011, Maryland, USA.



GAA deeply scaled Si NW MOSFET with ALD high-k/metal-gate stack (W~4 nm), M. Najmzadeh, IEEE ESSDERC 2011, Helsinki, Fi.



GAA Si nanowires as high temperature performance MOSFETs, M. Najmzadeh, IEEE DRC 2011, CA, USA.



3D TCAD Sentaurus simulation of GAA NWs for transport analysis, M. Najmzadeh, SSE 2012.



### **3D Si nanowires sensors**

- New concept in e-BRAINS: stacks-of-stacks
- 3D stacking of SiNWs in etched (microfluidic) cavity





M. Bopp. EPFL PhD thesis, 2010.

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### Si Nanostructures as Biosensor

Vertically Stacked Si Nanostructures





### Si Nanowire Bio-Sensors

### Nanotera Project on Silicon Nanowires Bio-sensors



O. Knopfmacher, Nano Letters 10, 2268 (2010)

S. Rigante, L. Lattanzio and A. M. Ionescu, FinFET for High Sensitivity Ion and Biological Sensing Applications, Microelectronics Eng (2011)

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# **3D Opto-electronic Integration**

Requirements:

High performance variable real-time signal processing Functionalities:

Sensing moving speed:

integration of image sensor, MEMS accelerometer and RF IC Computing:

3D Memory and 3D processor

High speed information networking

Optical interconnects:

Photodiode and surface emitting laser (VCSEL)

Heat sinking from power consumption VLSI: Micro-fluidic channels



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### **3D Opto-electronic Integration**



K.-W. Lee, IEDM 2009

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# **Photonic Integration**

«Siliconize» Photonics

#### (a) heater pn phase shifters M Light Source Guide Light Modulator input 2x1 MMI output 1x2 MM ·WHI on-chip resistor RF source Low-cost Assembly Intelligence Photo-detection (b) Traveling-wave electrodes ground pround colde S SACIETY A. Liu, MPW/APMP 2008 Silicon Evanescent Laser (b) p contact (a) p-InGaAs p contact p-InP cladding ..... ...... III-V Mesa III-V p- AlGaInAs SCH ----H+ H+ III-V region proton proton Region n contact AlGaInAs MQWs n-InP buried oxide n-InP/InGaAsP SL silicon substrate ----SOI **Buried** Oxide silicon wavequide optical mode Region Si Substrate not to scale 10 µm

#### **Optical Silicon Modulator**

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J. E. Bowers, CLEO 2007

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# **3D Scavengers**

Autonomous micro-generators are in demand for a wide range of electronic system applications that harvest energy from the environment require to be located close to the source, examples:

- Walking (piezoelectric)
- Body Heat Miniaturized
- Thermoelectric Devices



J. P. Carmo, POWERENG 2009

N. S. Shenck, IEEE Micro 2001

# Conclusions

The future of Nanoelectronics could be foreseen as a combination technology and design in More than Moore with the heterogeneous integration of a large variety of technologies, and their exploitation in System-On-Chip, System-In-Package or System on System, mearging various discrete subsystems using different optimized maufacturing process

### **Open questions:**

- What are the requirements from Smart Systems to 3D?
- What advanced packaging technologies? Cost?
- What are the advantages of RF MEMS and what functionalities and performance by their heterogeneous integration with CMOS?
- Similar question for 3D optics and sensors.
- Is heterogeneous integration the enabler of life after CMOS?

### Thank you for your attention!

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