Technology and Design challenges in future low power memory devices and circuits

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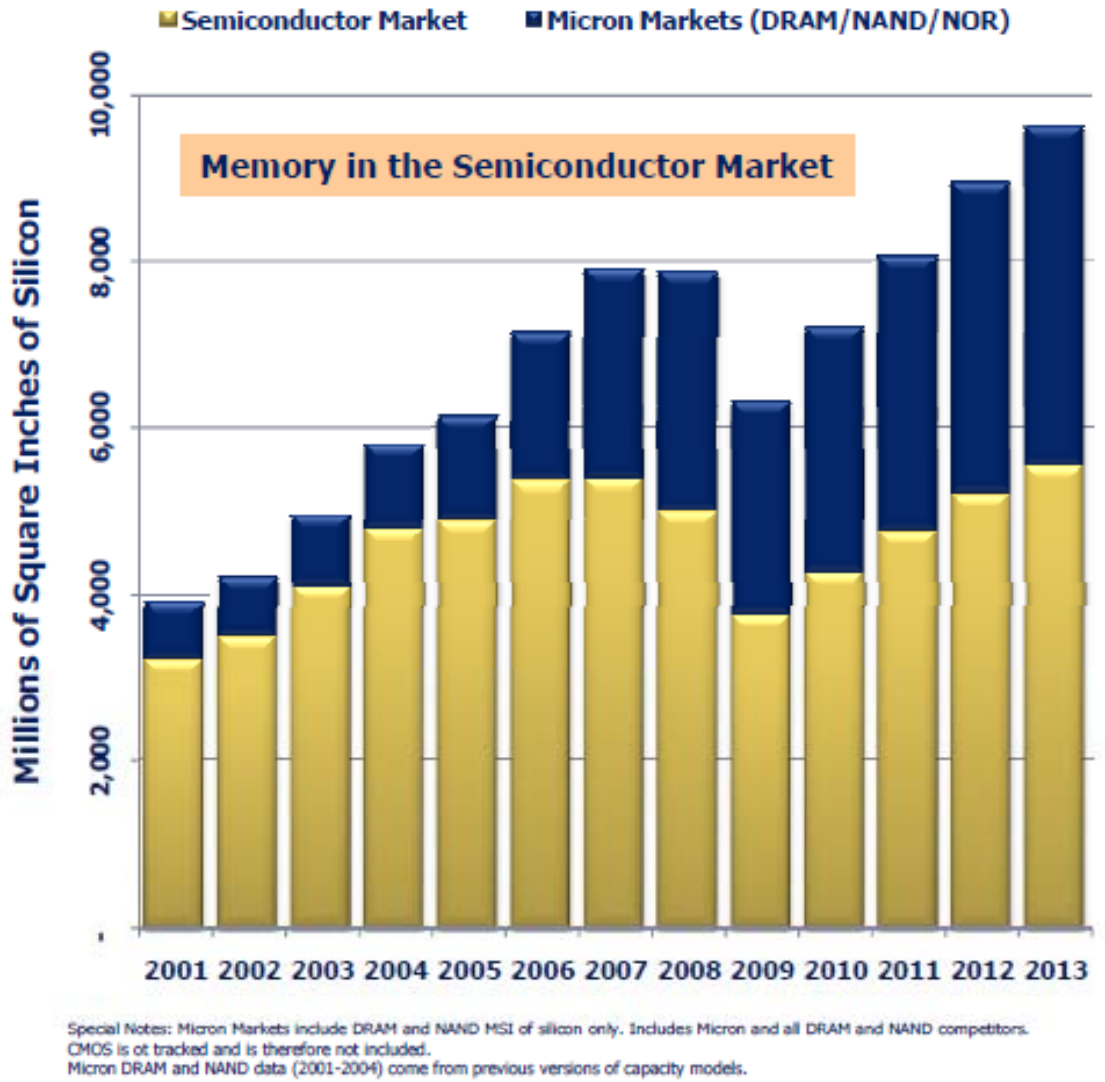
Embedded Tutorial presented by the NANO-TEC Project:
"BEYOND CMOS - BENCHMARKING FOR FUTURE TECHNOLOGIES"

Outline

- **Introduction**
  - **Beyond the wall**
- **Challenges and Opportunities**
  - **Managing variability**
  - **Low power memory devices**
  - **Neuromorphic systems**
- **Summary**

Why Memory market is important?

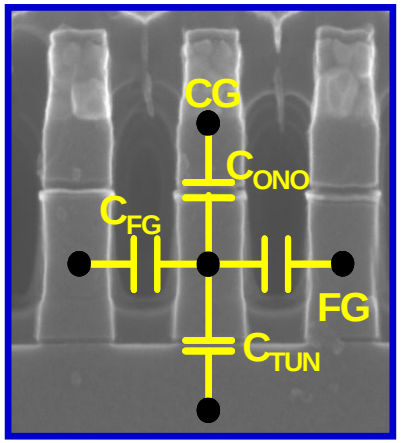
- **Memory is better and better the oil moving the technology industry**
- **Nearly half of silicon across semiconductor industry goes towards manufactory memory**



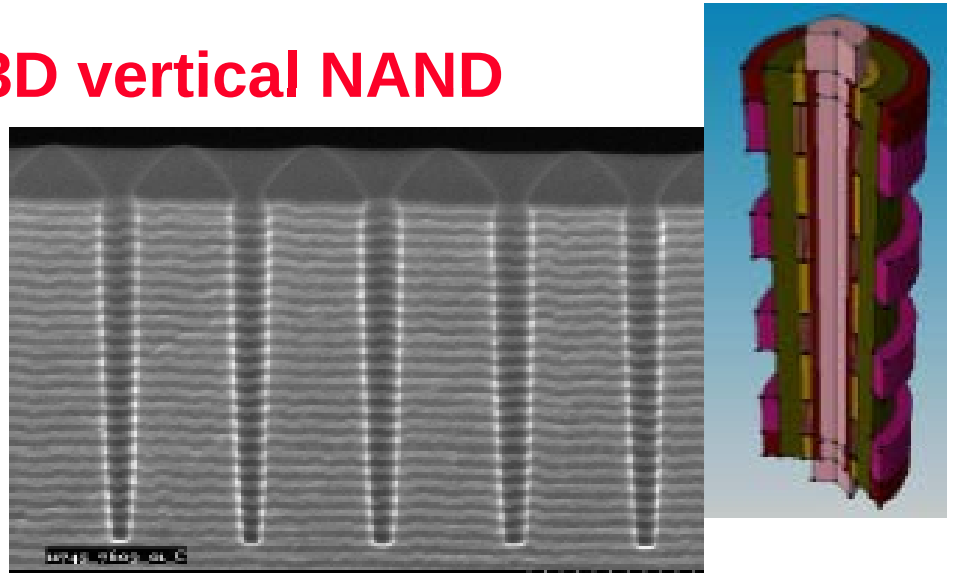
Flash memory: scaling issues

Physical limitations against the Moore's Law:

- **Dielectrics scaling: reliability issues**
- **Interferences between adjacent cells**
- **Noise: RTS**



Next step: 3D vertical NAND



...allows continuing the cost level scaling

What beyond the ‘wall’?

- **Just need to figure out when NAND hits the wall and be standing on tracks with a better technology**
- **Technology needs to be competitive in most metrics**

Alternative memory concepts

- **Moving Atoms**
  - **PCM, CBRAM, RRAM (Filament, Metal Oxide), FeRAM, CNT, Molecular....**
- **Moving Spins**
  - **MRAM, STTRAM, Racetrack...**

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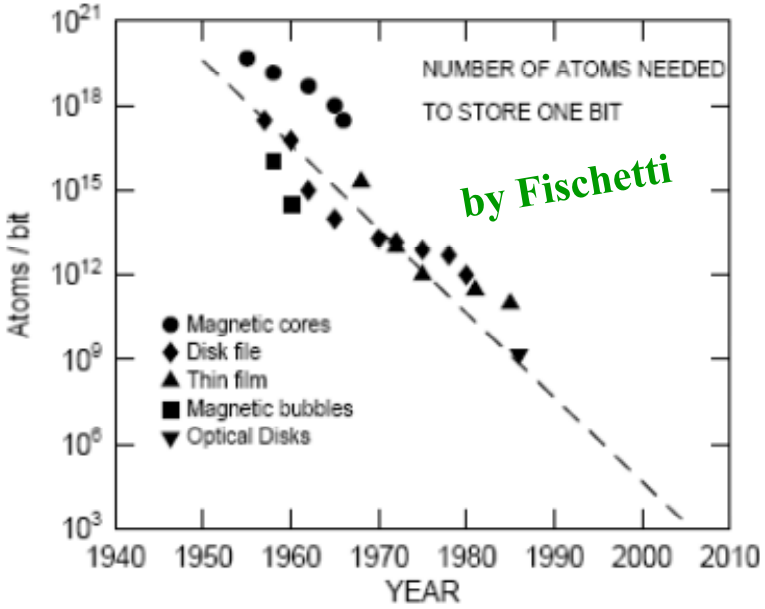
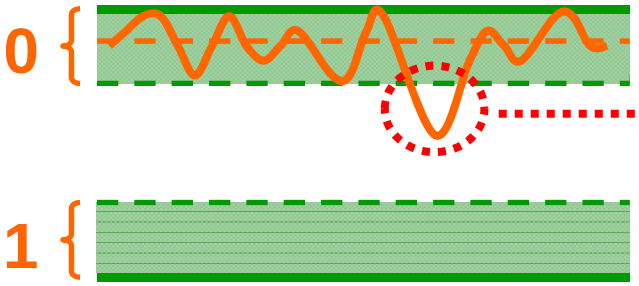
Noise/Signal ratio limits scaling

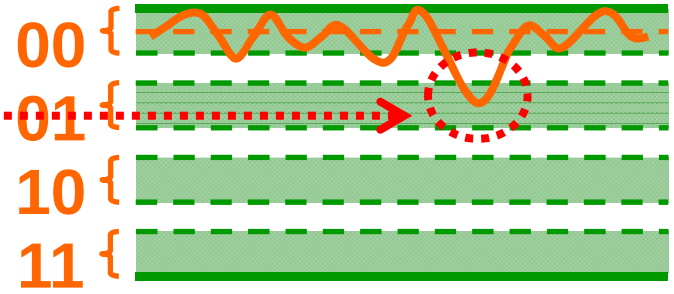


Nowadays atomic scale fluctuations can alter the information bit due to the cell scaling

SINGLE LEVEL

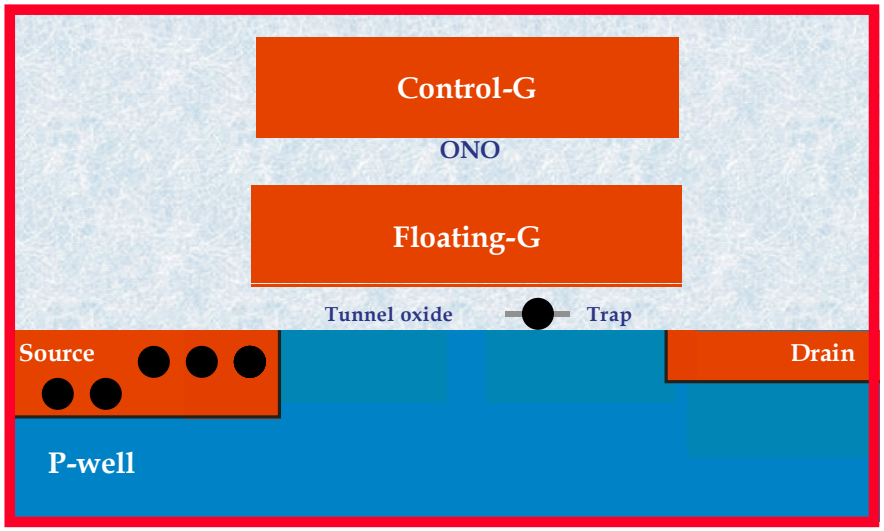


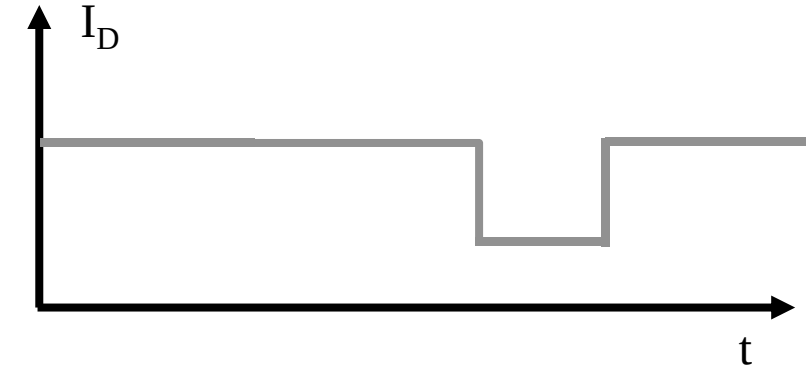
MULTI LEVEL

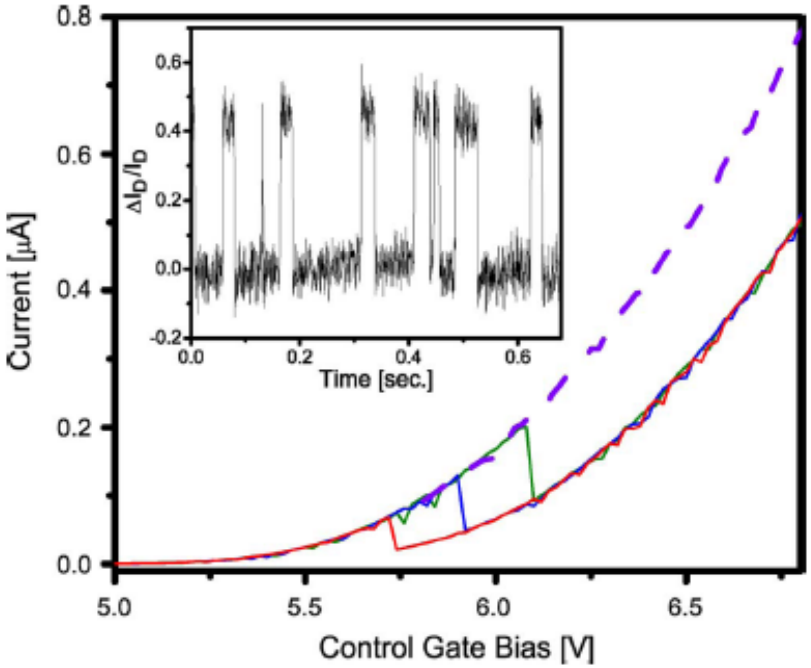


Noise can leads to a wrong readout **in** multi-level **devices**

Random Telegraph Noise



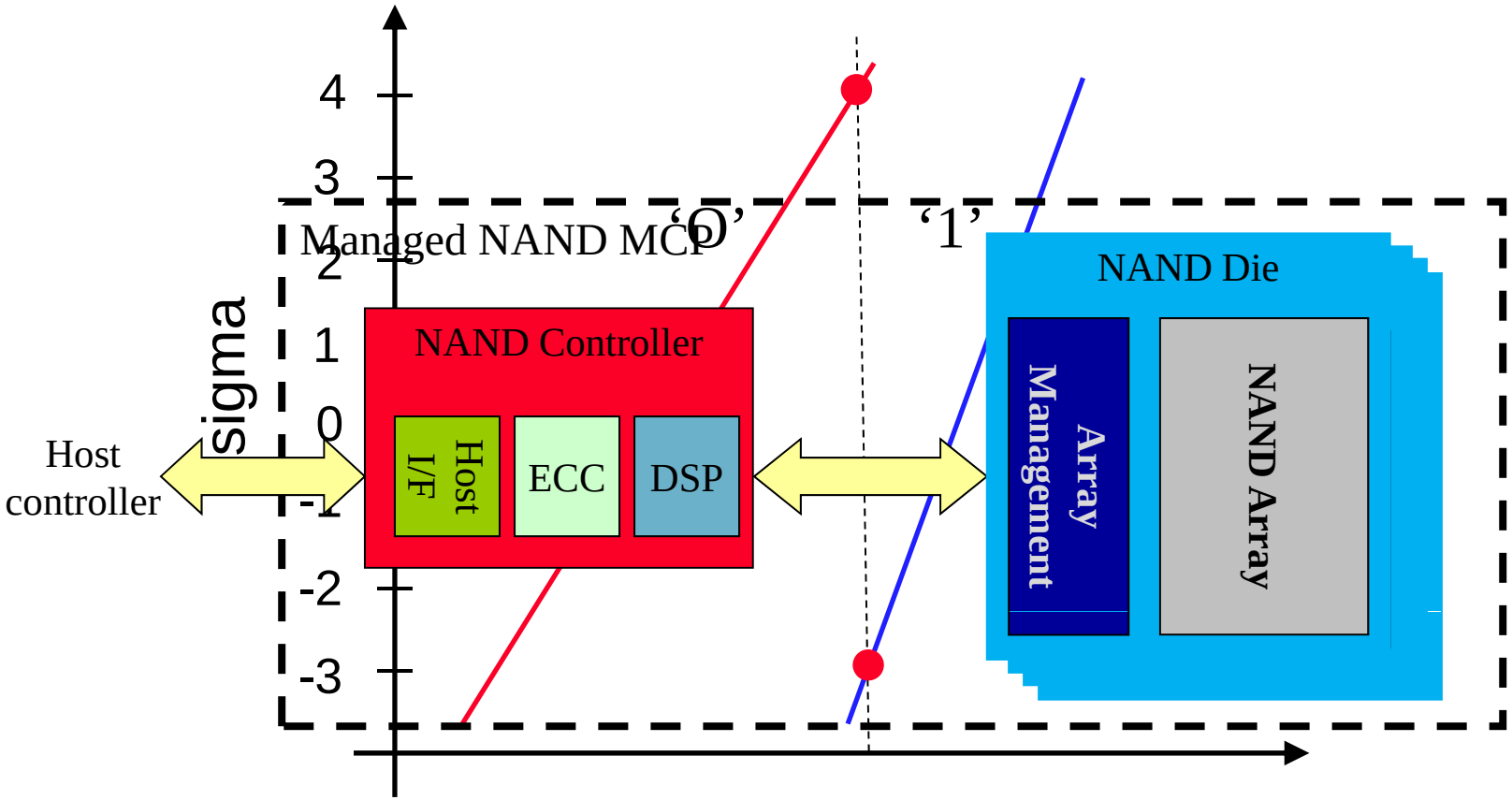




Giant RTS phenomena
in nanoscale FG devices

P. Fantini *et al.*, EDL **28** 1114 (2007)

Managing variability: e-MMC



- **Challenge: communication between two world running with different speed**

Challenging the power scaling

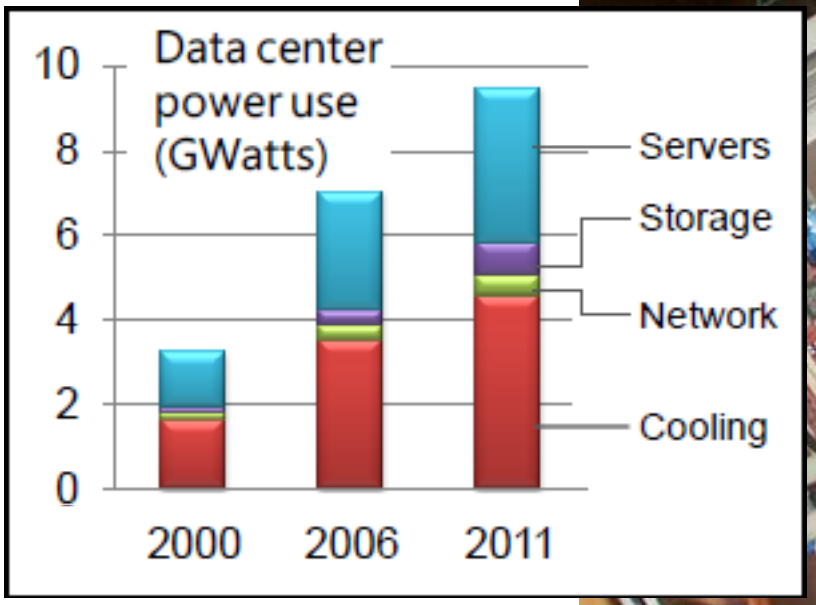
20 Watts

200 KWatts

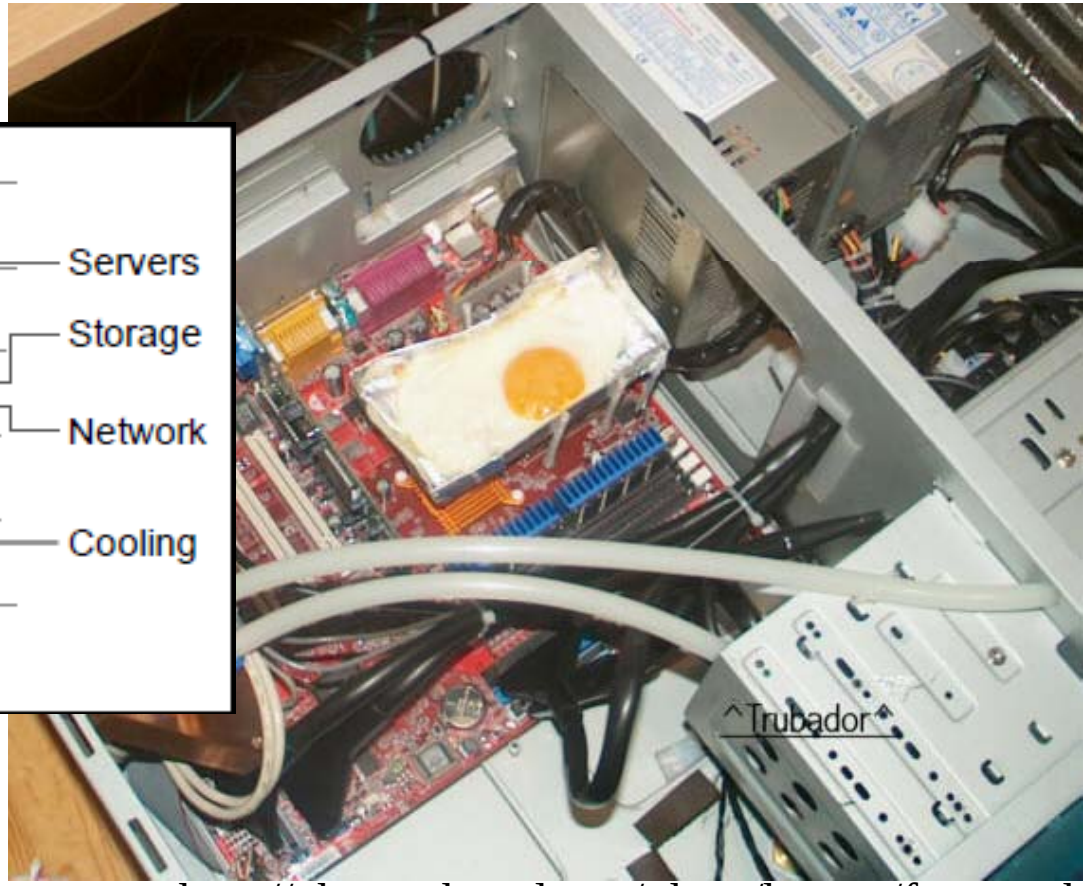
1e4x

conventional Moore's Law size scaling can get us ~10x

Electronics waste much power



E. Pop, Nano Research 2010

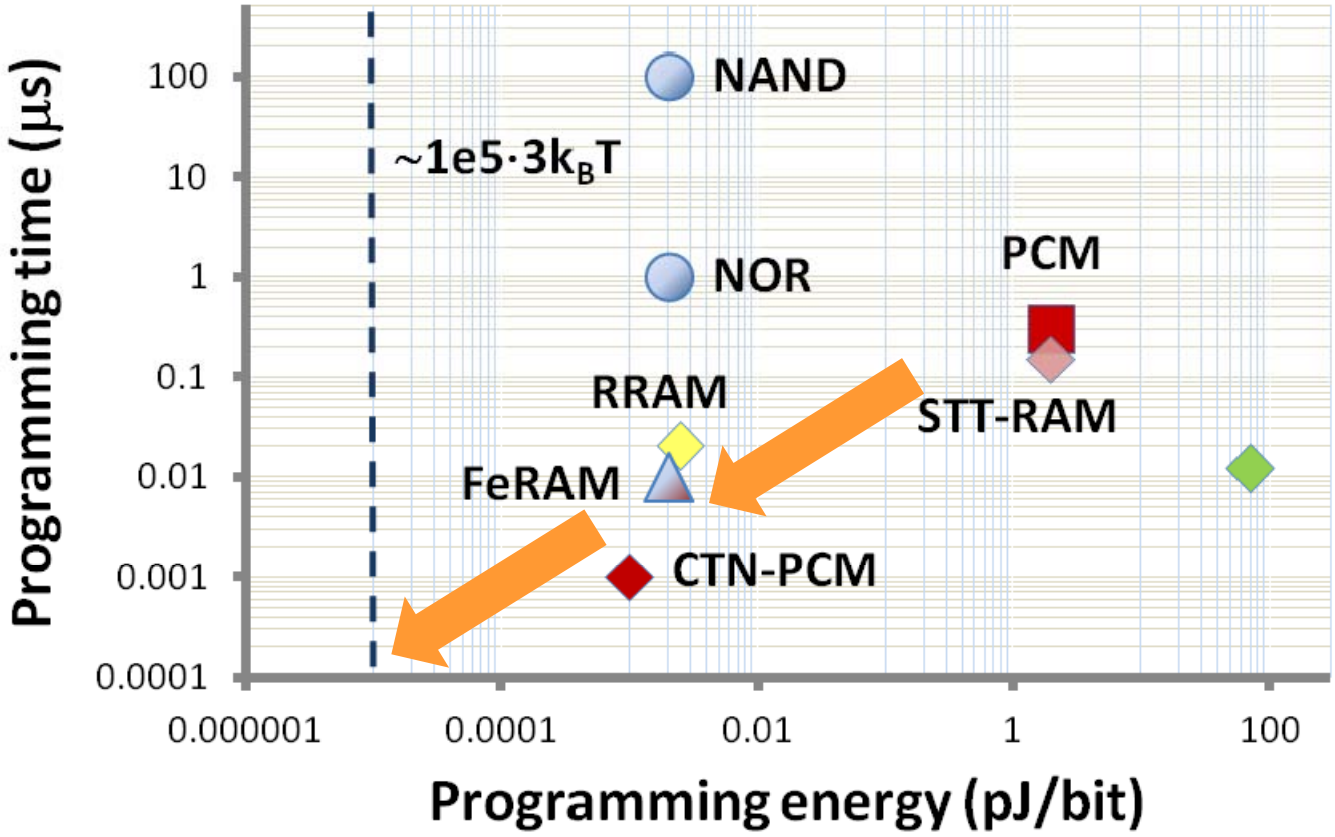


http://phys.ncku.edu.tw/~htsu/humor/fry_egg.html

energy limits performance from battery to powerful CPUs (heat sink)

Power consumption of memories

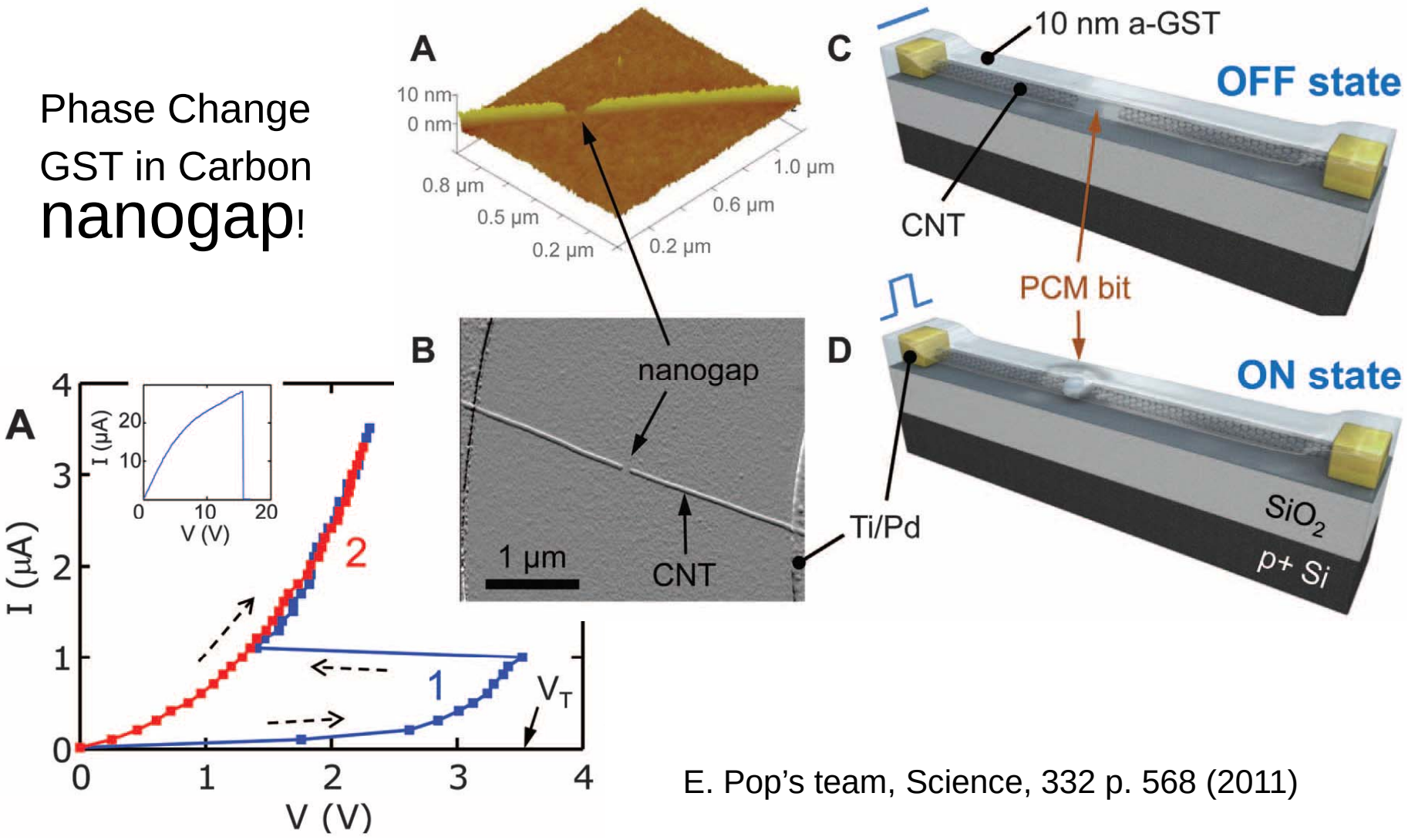
- **Trade-off between speed and energy**



Much room to tear down the energy consumption

Low power PCM cell

Phase Change GST in Carbon nanogap!



E. Pop's team, Science, 332 p. 568 (2011)

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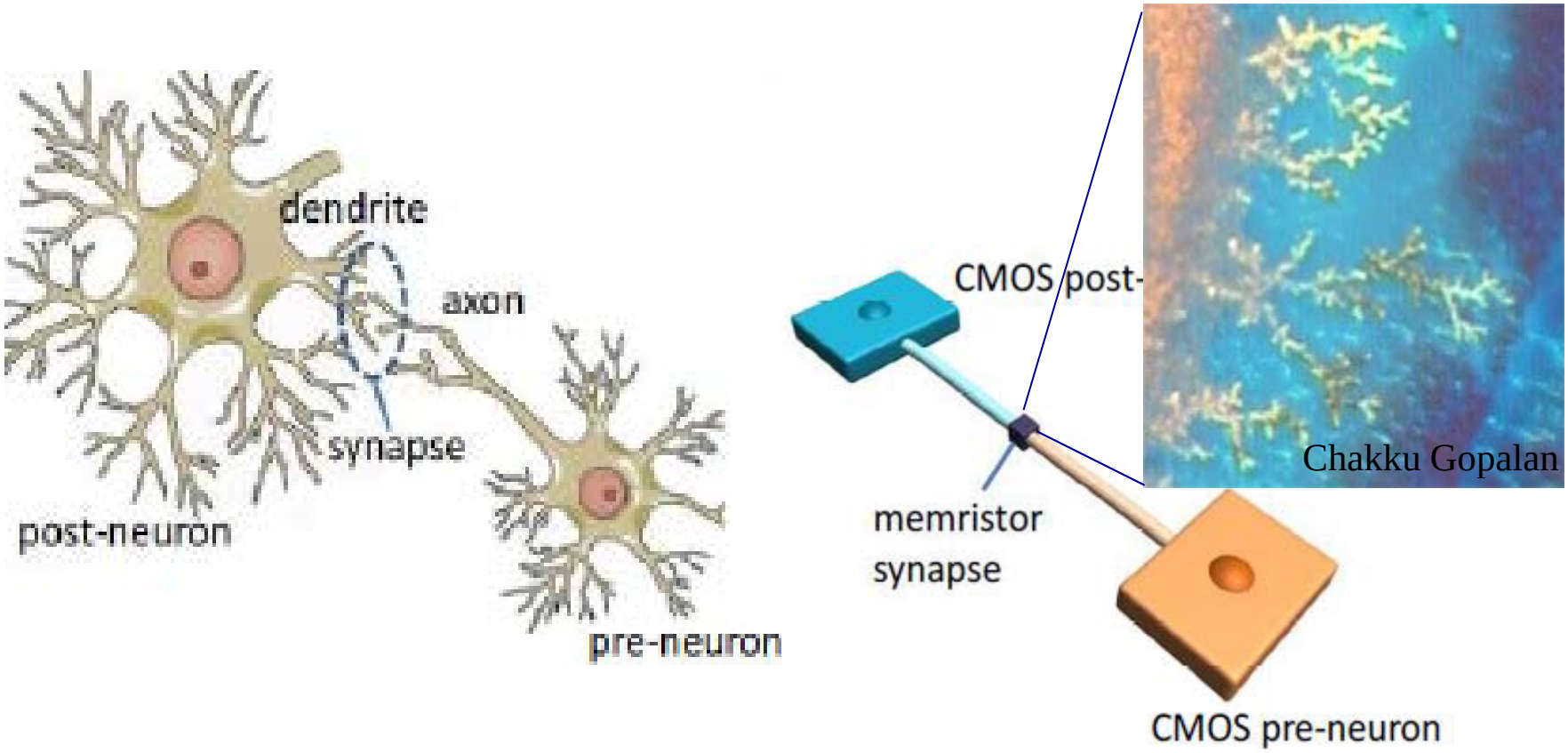
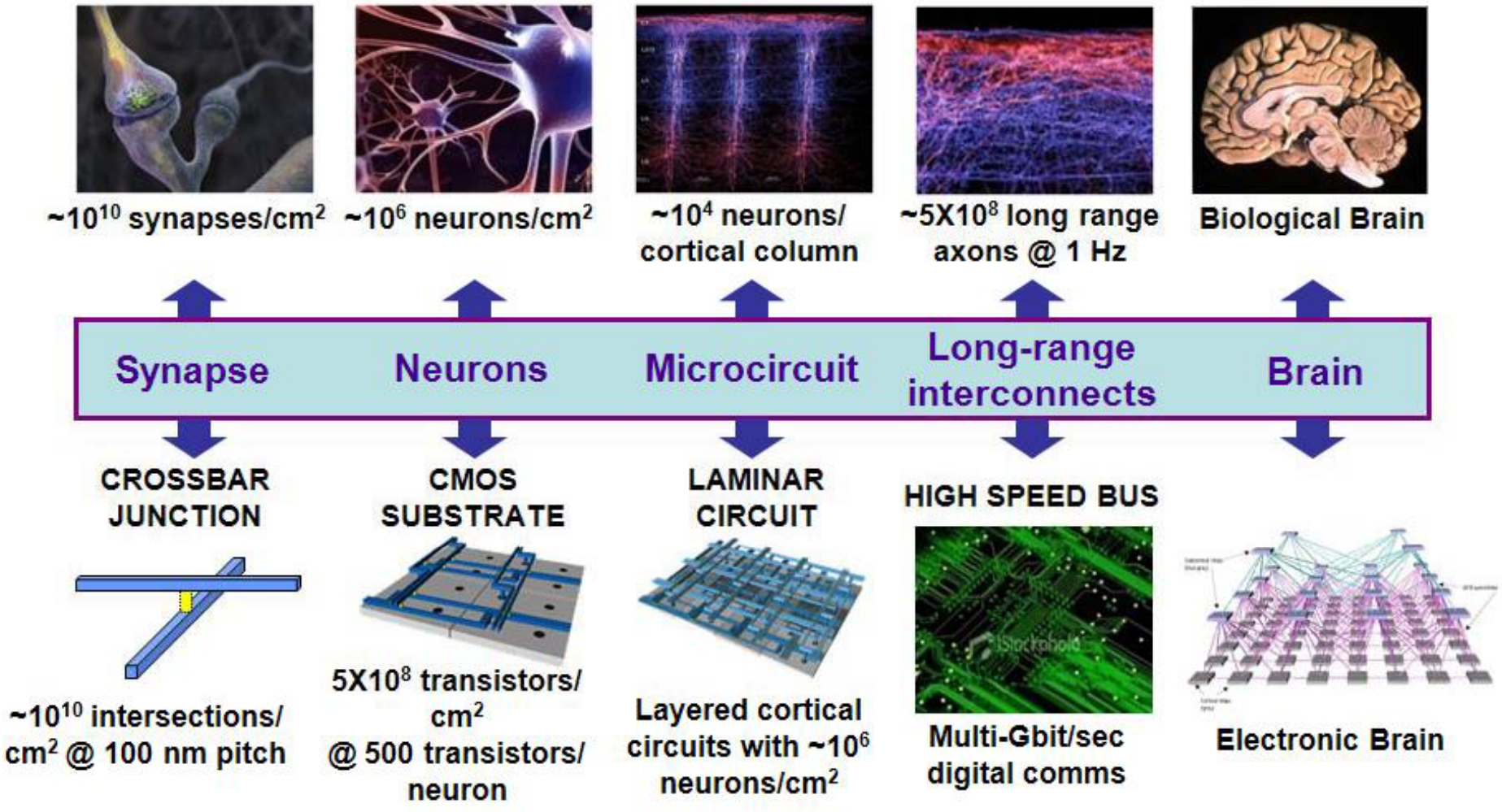
Synaptic characteristics of Memristor



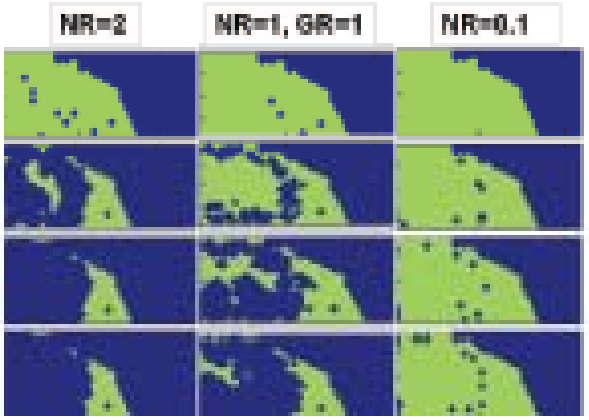
- **The history-dependent resistance in the Memristor can be used as a synapse**

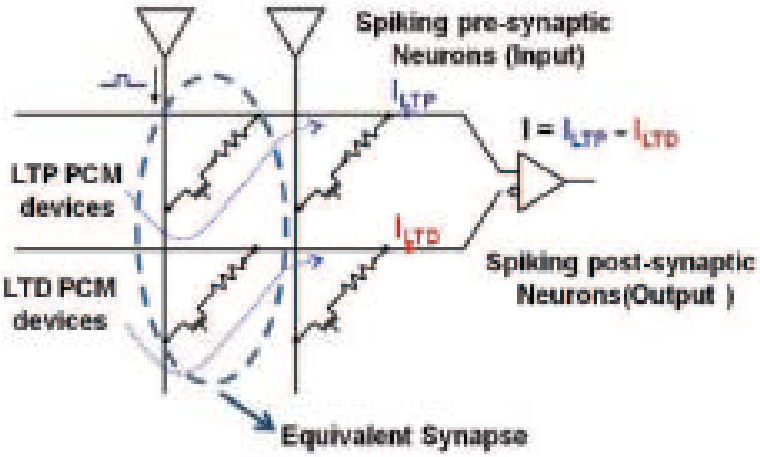
Neuromorphic systems

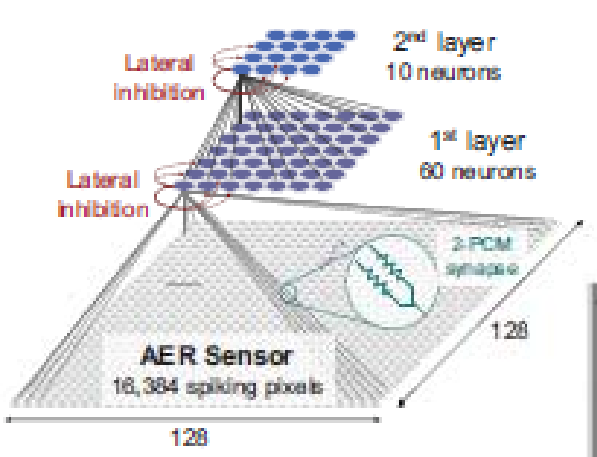


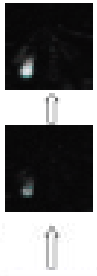
http://nextbigfuture.com/2011/07/darpa-synapse-phase-2-targets.html

PCM as synaptic systems



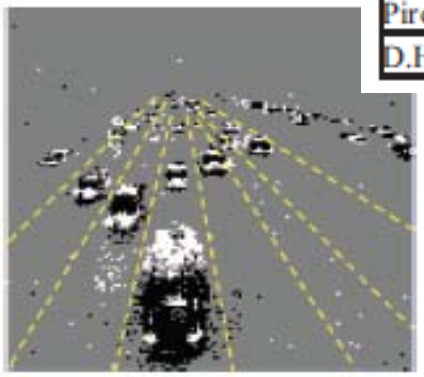






Detection by 2nd neuron layer

Detection by 1st neuron layer



PCM Technology	Ereset (pJ)	Eset (pJ)	System power (µW)
This paper (GST-PCM)	1552	121	112
Jiale,VLSI-2011	1.2	0.045	0.056
F.Xiong, Science-2011	0.1	0.03	0.02
Pirovano, ESSDERC-07	24	4.9	3.6
D.H.Im, IEDM-2008	5.6	0.9	0.68

Leti, IEDM 2011

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Conclusions

- **Looking at the future, any ‘universal’ memory has been presented**
- **...but appealing Challenges and Opportunities for the new nano-electronics market:**
  - **New design strategy to manage the intrinsic nanoscale variability (eMMC)**
  - **Much room for power scaling (~ 1e4x) of new technologies**
  - **New memory technologies as building blocks of Neuromorphic systems**