Embedded Tutorial:

"BEYOND CMOS - BENCHMARKING FOR FUTURE TECHNOLOGIES"

Moderators:

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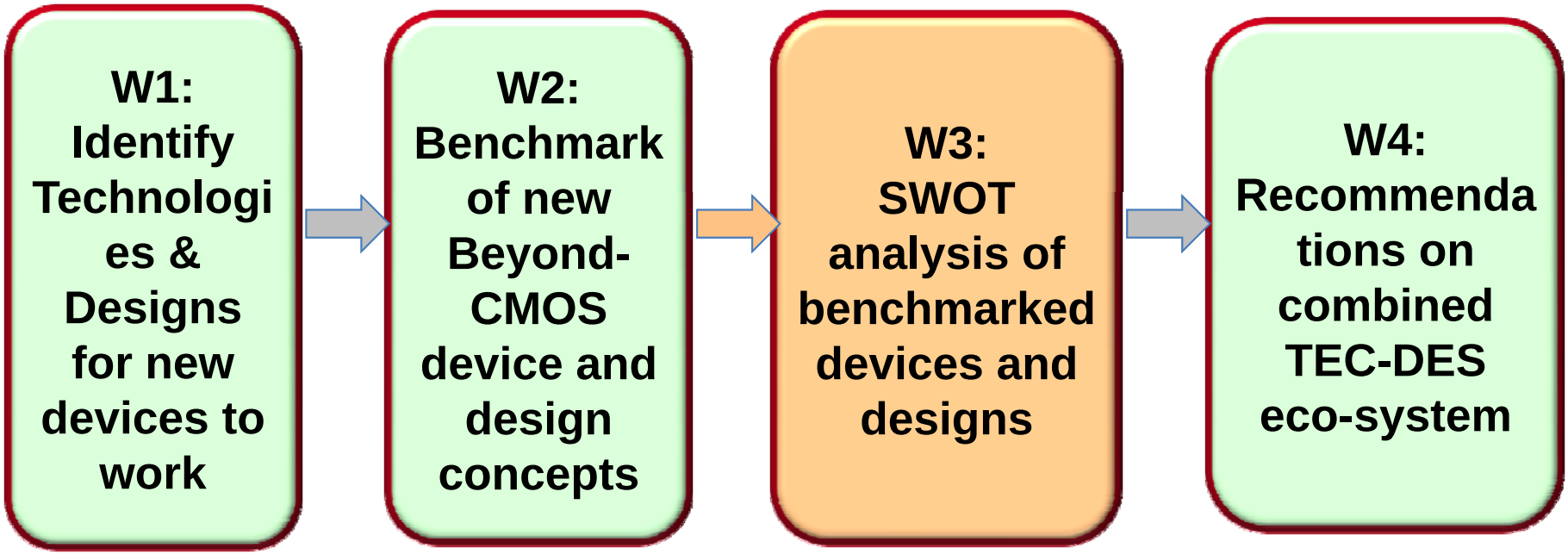
NANO-TEC has received funding from the European Community's Seventh Framework Programme (FP7/2007-2013) under grant agreement n° 257964

About NANO-TEC

AIMS

- To identify the next generation of (emerging) device concepts and technologies for ICT.
- To build a joint technology-design community to coordinate research efforts in nanoelectronics.

NANO-TEC timeline



Presentations

- **Emerging Technologies: More Moore and More than Moore**
  - Dr Mart Graef, Delft University of Technology, The Netherlands
- **Technology and Design challenges in future low power memory devices and circuits**
  - Dr Paolo Fantini, Micron Semiconductors, Italy
- **Bridging Technology and Design for Beyond CMOS**
  - Prof Paolo Lugli (tentative), Technical University of Munich, Germany
- **Bridging Technology and design in More than Moore**
  - Dr Wladek Grabinski, EPFL, Switzerland
- **Benchmarking for Beyond CMOS technologies**
  - Prof Jouni Ahopelto VTT, Finland

Emerging Technologies: *More Moore* and *More than Moore*

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Overview

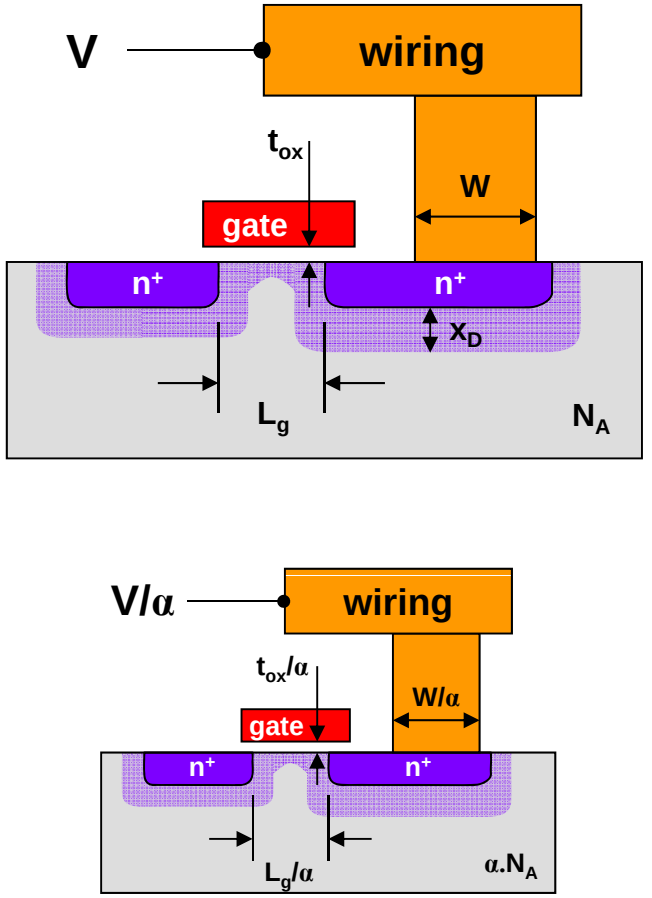
Beyond CMOS:

What is new about emerging technologies?

- **Miniaturization**
- **Parameterization**
- **Diversification**
- **Designability**

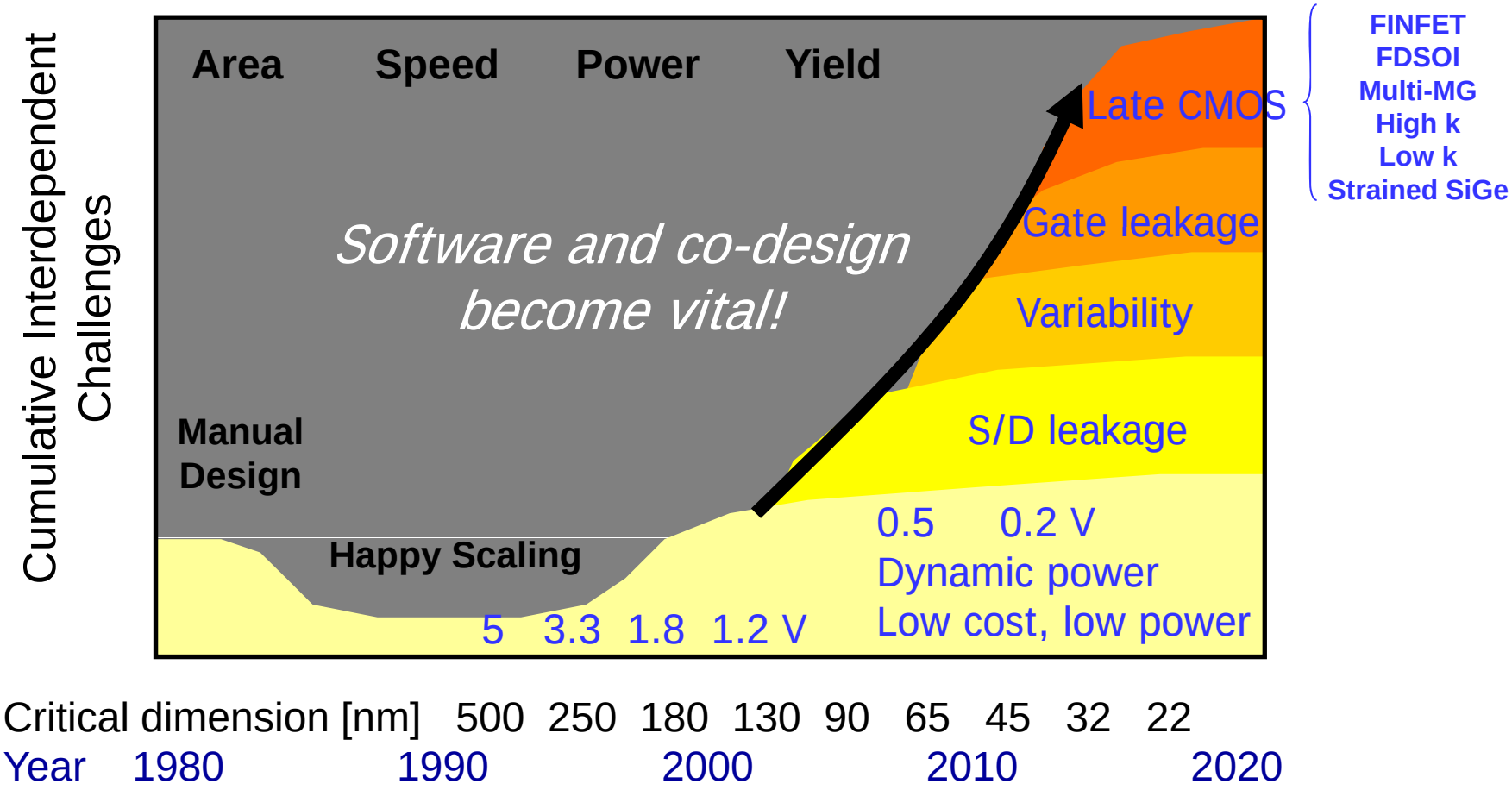
Constant Field Scaling

dimensions t_{ox}, L, W	$1/\alpha$
doping	α
voltage	$1/\alpha$
integration density	α^2
delay	$1/\alpha$
power dissipation/Tr	$1/\alpha^2$

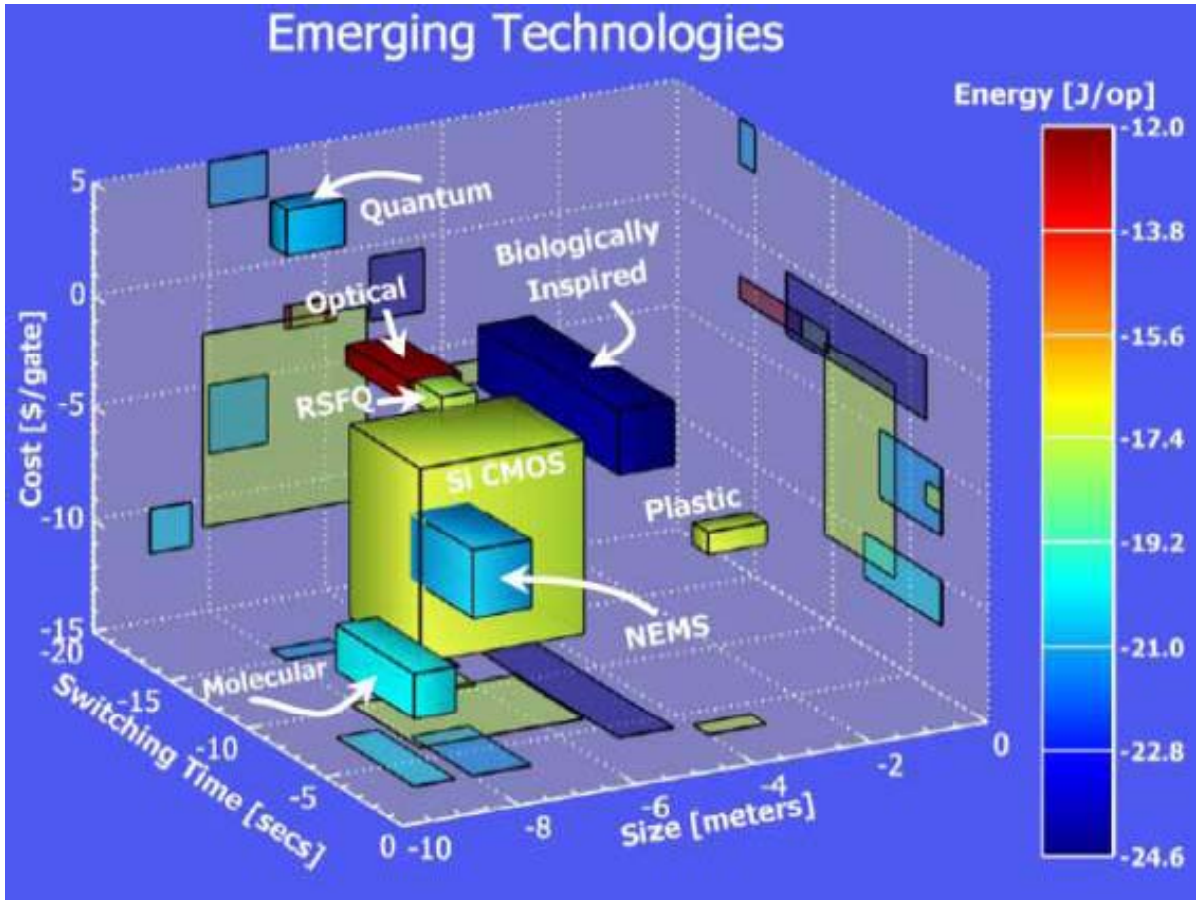


Source: More than Moore White Paper, ITRS (2011)

More Moore: Increasing complexity

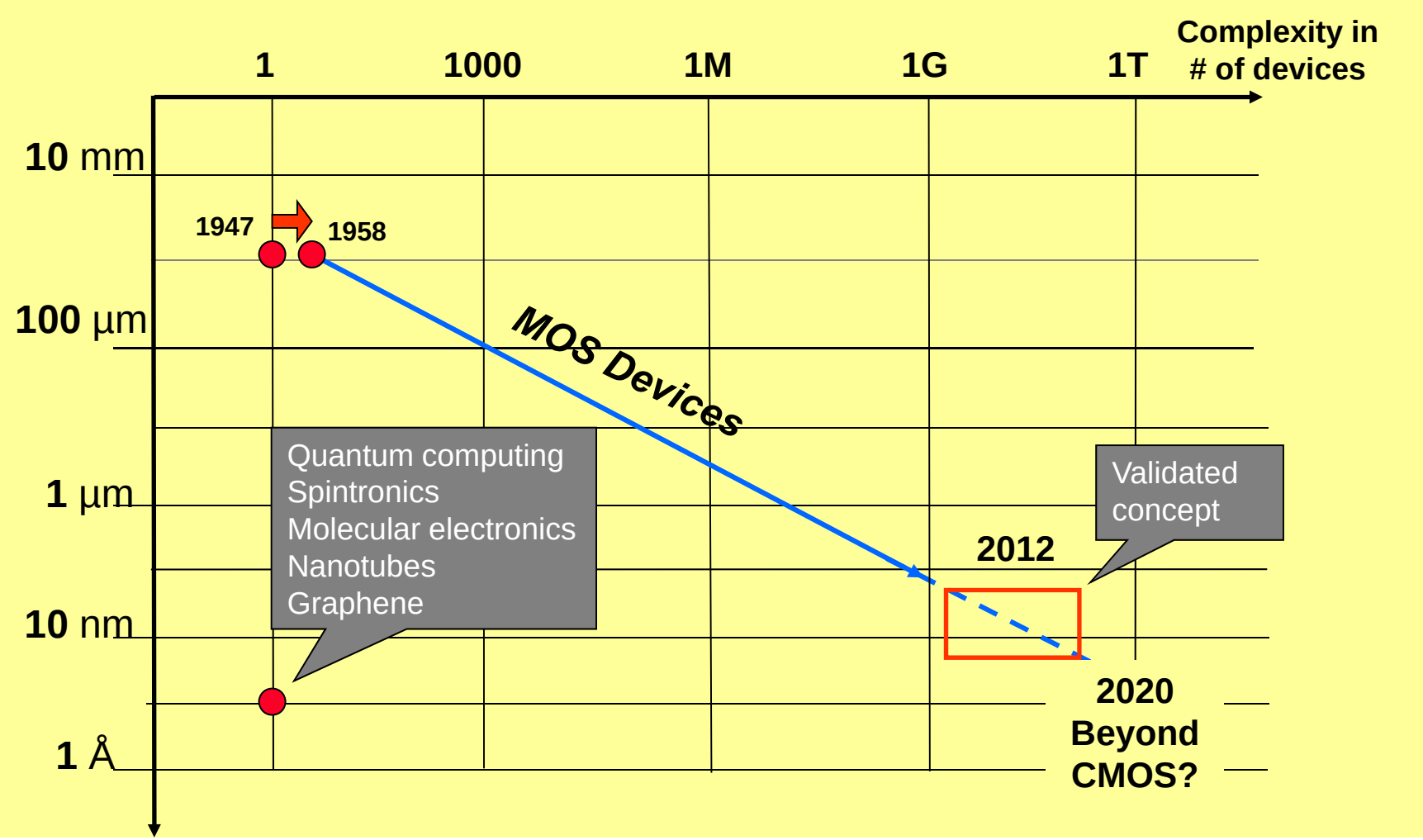


Parameterization of emerging technologies



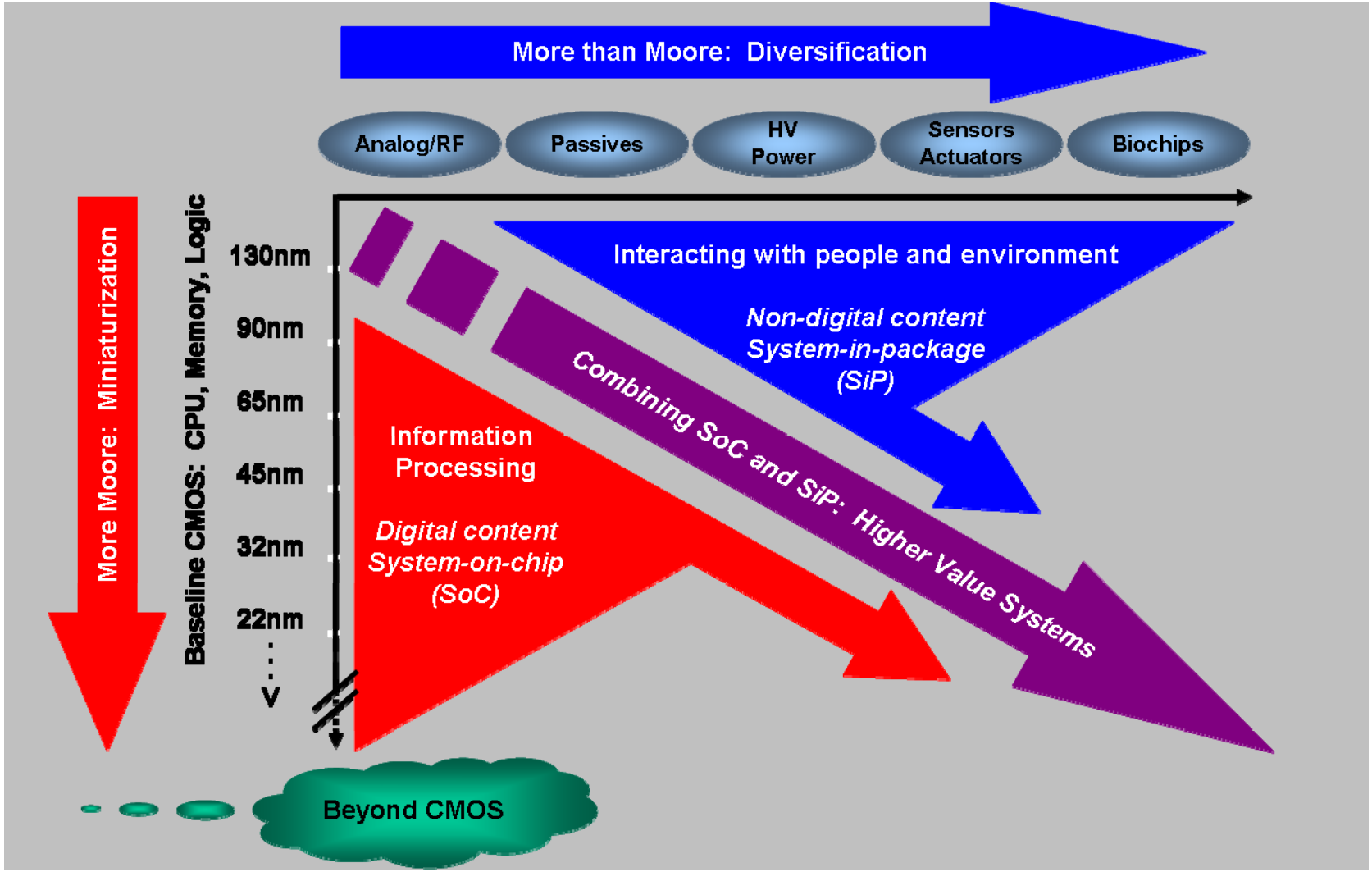
Source: ITRS

Reaching dimension/complexity limits



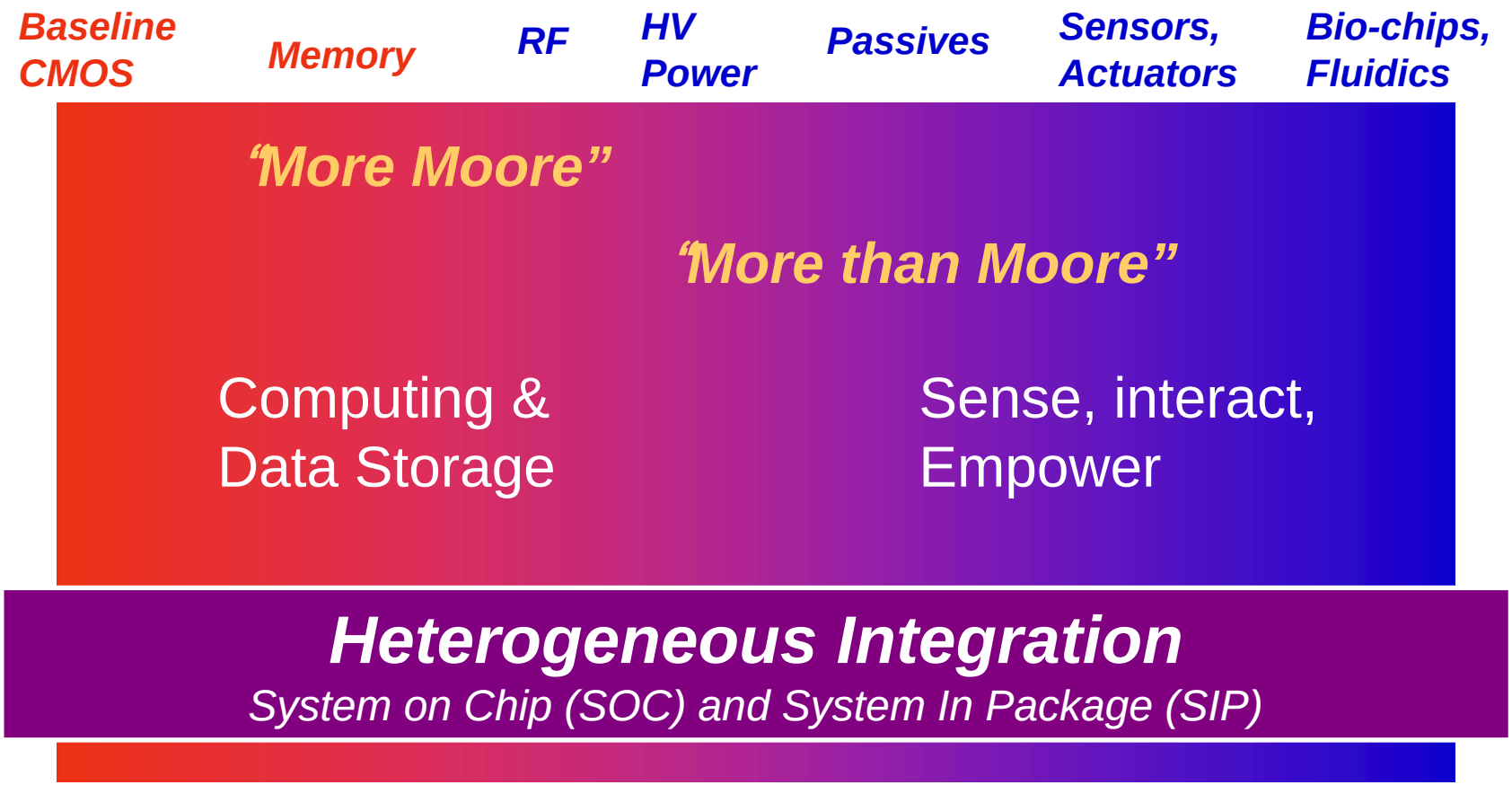
Source: STMicroelectronics

“More Moore” & “More than Moore”



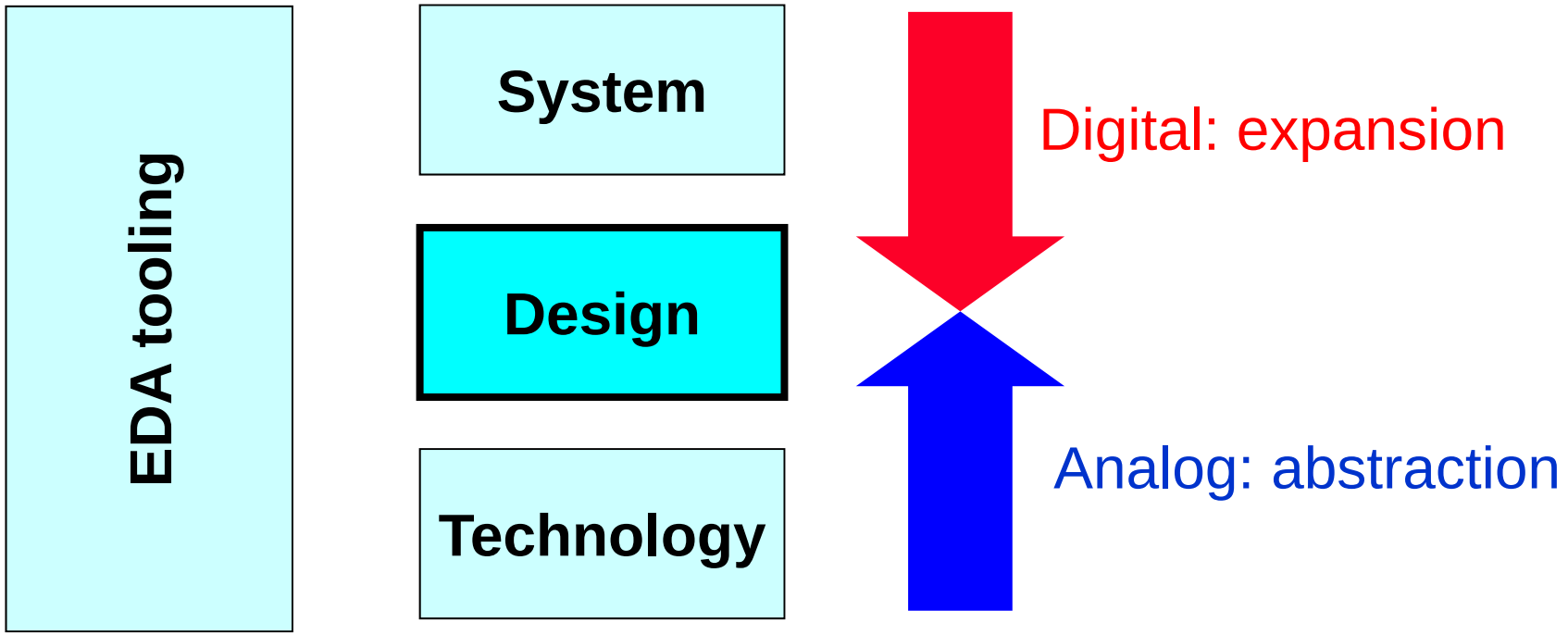
Source: ITRS (2011)

“More Moore” & “More than Moore”



Source: ENIAC

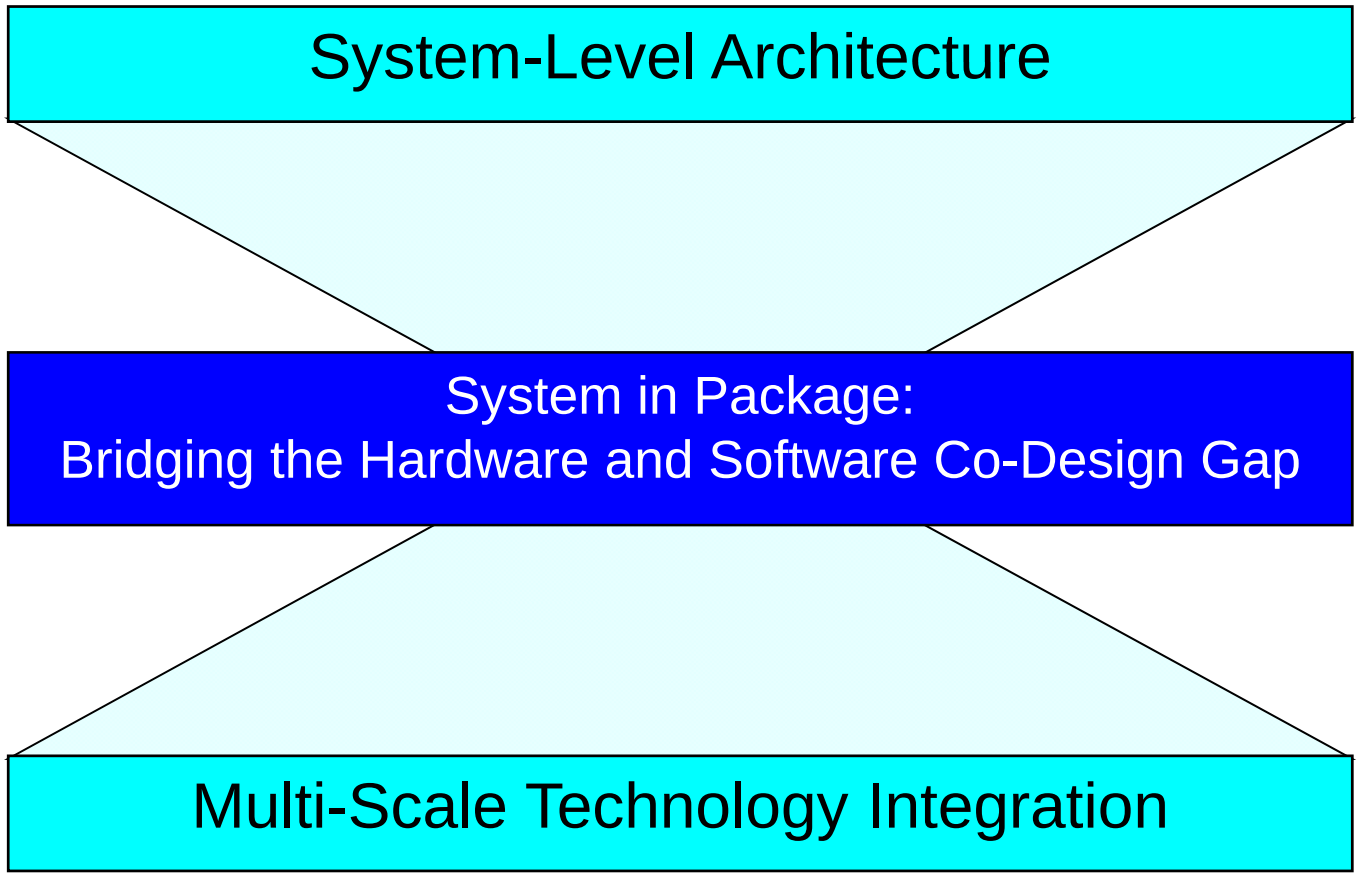
Design Hierarchy



- **Analog and digital approach design from opposite directions**
- **Mixed-signal: need to “meet in the middle”**

Source: Maarten Vertregt, NXP

MM & MtM: The Co-Design Callenge



MM & MtM: Design Aspects

- **More Moore:**
  Design technologies that enable equivalent scaling (high performance, low power, high reliability, low cost, high design productivity)
  - Design for variability
  - Low power design
    (sleep modes, hibernation, clock gating, multi-VDD, ...)
  - Homogeneous and heterogeneous multicore SoC architectures
- **More than Moore:**
  Design technologies that enable functional diversification
  - Heterogeneous system partitioning and simulation;
  - Analog and mixed signal design technologies for sensors and actuators;
  - New methods and tools for co-design and co-simulation of SiP, MEMS, and biotechnology