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Coordination Action
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Ecosystems Technology and Design for Nanoelectronics

NANO-TEC

Deliverable D6.7 Presentation of main achievements of the NANO-TEC Workshop Series.

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Recommendations on Beyond CMOS Nanoelectronics Research

Compiled and edited by the NANO-TEC project

December 2012

Recommendations on Beyond CMOS Nanoelectronics Research

Compiled by the EU FP7 ICT project NANO-TEC, based on presentations and discussions during the workshop series held between January 2011 and November 2012.

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Executive Summary

This document contains the recommendations arrived at during the discussion and consultation process organised by the project NANO-TEC. It is anchored in the grand technological challenges in information processing, communications, based on memory and logic devices, circuits and architectures with a view to the time when CMOS scaling begins to loose some of its advantages over emerging nanoelectronic technologies.

To prepare for the future, Europe needs a strong R&D competence in Electronic System Design to integrate technology in emerging design processes. It is in this context that the European Commission funded the Coordination Action project NANO-TEC, to help to establish a joint design and technology community in Nanoelectronics in Europe, from the combined technology and design perspectives in the field of Beyond CMOS. Thus the **scope** of NANO-TEC is basically two-fold:

(i) To bring the design and technology community closer in Beyond CMOS research in order to strengthen R&D in Europe, and
(ii) To document the vision, recommendations and needs of the Beyond CMOS research community in the context of European-level research.

The **main activity** was based on interactive discussions in a workshop series. The four NANO-TEC workshops were:

1. *Identification of the main requirements for future ICT Devices*, Granada, Spain January 20–21, 2011,
2. *Benchmarking of Beyond CMOS device/design concepts*, Athens, Greece 13-14 October 2011, for which a special methodology was prepared,
3. *SWOT Analysis of the Technology-Design Ecosystem***,** Lausanne, Switzerland, May 30-31, 2012, in which all the discussed technologies were analysed.
4. *Discussion of draft recommendations,* Barcelona, Spain, November 6-7, 2012, where this document was discussed.

Overall 132 people participated in the NANO-TEC workshops, most of them more than once and several joining the four workshops. The regional distribution was as follows: 92% Europe, 7% USA and 1% Asia. The corresponding affiliation type were: 45% academic, 40% research organisations, 11% industry and 4% others.

The discussions considered CMOS compatible technologies involving charge-based devices and their potential interface with this prevailing technology, other existing technologies and humans. Non-charge-based devices and emerging technologies were discussed in the general context of RTD. In general the discussants attempted to ask the “right questions”: (power and not speed, not necessarily a new switch but cleverer switches, limits of binary computing, etc.).
For the *benchmarking* exercise, a new methodology was developed in order not to exclude potential future functions while tracking common aspects, such as power consumption. During the *SWOT analysis* business niches and opportunities were identified.

The second aim of bridging the gap in research between the communities of Design and Technology in Beyond CMOS was addressed in Panel discussions and working groups as

well as in specialist talks. At present it is possible to identify systematic work in the phase of a learning period in design and technology joint effort in evolutionary RTD. However, such learning period still has to start in the more disruptive RTD in Beyond CMOS.

The presentations, discussants interventions, rapporteur reports, working group material and workshop reports are all available to the public at: https://www.fp7-nanotec.eu/.

Recommendations concerning R&D in *state variables*:

- Concerning *all state variables*, be these charge-based or not, it is recommended that research towards a better theoretical understanding of the underlying physics and material science of nano-scale devices is supported towards potential breakthroughs. In particular, the large variance in physical and electronic properties of the concepts and technologies discussed, requires that in addition to a higher level of knowledge, the design and emerging devices communities must work together to assess and exploit the full potential of this device- and system-relevant research area.
- Furthermore, *for most state variables*, the interconnect challenge at the nano scale, i.e., connecting to and from nano-devices, is a common one to be overcome theoretically, experimentally and technologically as it affects not only performance, interconnects and architectures but also, and perhaps more importantly, reliability and temperature stability.
- Considering *charge-based state variables*, and in particular *nanowires*, it is recommended that a combination of nanowires technology with III-V compounds and or alternative architecture be explored with view to integrate III-V compound nanowire devices on a Si platform. In the area of *graphene*, emphasis should be placed on the suitability of fabrication and integration constraints in a combined Si-graphene new ICT technology, going beyond sensors and single components. Along the lines of two-dimensional systems, *layered materials* could be explored as alternatives as they exhibit an energy gap. In the light of recent progress, *topological insulators* should be considered earlier rather than later in a targeted research effort. The field of molecular electronics would benefit from strong collaborations between physicists and chemists on the one hand, with the technology and design communities on the other. Concerning *memristive devices*, local heating, which impacts power consumption, needs to be addressed, as well as co-firing, fan-out and scalability bounds. Since highly non-linear processes are involved, work towards an adequate theoretical framework is mandatory.
- Concerning *non-charge-based state variables*, and starting with spin, it is recommended to support research in spin logic as this constitutes a field, potentially able to deliver low power devices towards non-dissipative information processing. Any future program on *NEMS* should include a strong element on understanding contact physics, friction and wear at the nano-scale, all three factors being essential for the development of active power management and logic applications; further miniaturisation of NEMS through technology development and especially improved design and simulation tools to include several aspects of physics.

Recommendations concerning R&D in *new computation paradigms*:

- New computing paradigms are required for information processing including, for example, *neuromorphic computing*, *quantum computing*, chemical and molecular

computing, quantum computing by molecular spin clusters and bio-inspired computing, among others. A practical recommendation in this field is to support research in a "super integrated project" or similar in which solid-state quantum computing and neuromorphic computing could become embedded in digital environments via digital-analogue hardware and software interfaces. The target would be to create useful hybrid systems to, e.g., interact with human users and be capable of adaptive learning. The research could be on fields in which unconventional computing could solve or give a more efficient answer in terms of energy and time. Such a "super IP" should pave the way for important commercial applications in 5 to10 years.

- It is recommended to continue the exploration of *novel computation approaches in general*. In particular, a *comparative and dynamic analysis of the interaction between design and the emerging computation technologies* as an integral part of the R&D efforts would provide Europe with a valuable and probably decisive advantage.

Recommendations on the *Design-Technology interaction*

- This interaction is a challenging one. The consortium finds that strong motivation and support are needed in order to facilitate *communication and cooperation between design and technology actors* from academia and industry. These communities have very different cultures and during the project progress has been made to establish communication and find some common terminology. Bearing this in mind, the consortium recommends that a couple of pilot projects are launched addressing explicitly not only the technical aspects but, above all, methodological aspects of this interactions with one or two well defined examples of novel state variables and a specific application each. The methodology lessons of such projects would be a starting point on the practicalities of meeting the technology-design challenge in Beyond CMOS research.
- A second recommendation is the setting up of a *simple and open infrastructure* for design connecting people and things. Such infrastructure could have an international character beyond EU borders to allow free exchange of knowledge, where the "systemability" of 'Beyond CMOS' devices is a formidable challenge. Furthermore, modelling and simulation of 'Beyond CMOS' devices and circuits have to be developed to gain sustainable knowledge to feed in the design processes.

Recommendation concerning the *involvement of industry*

- At present the willingness of non-European industry to enter in discussions on Beyond CMOS research has a higher profile than that of European ones. It is recommended that industry and researchers in beyond CMOS intensify their interactions to define more clearly the expectations for future Beyond CMOS technologies, future needs and roadmaps of long-term research. An example of this would be a reactivation of the Scientific Community Council towards an exchange of views to strengthen the overall European nanoelectronics research, to include technology readiness levels closer to the proof of concept one.

Recommendations concerning *research infrastructures and education*

- The consortium recommends that measures are implemented to foster the *coordination of all technological facilities* having a significant activity in beyond CMOS research,

in a European network with a single entry point in each country. Crucial to the proposed modus operandi is common access rules and harmonisation of the organisational procedure. The rationale is to take advantage of the complementarity of the ‘beyond CMOS’ research infrastructures and to capitalize on the fields of highest expertise in each country or region.

- Trends in the decreasing number of students in the physical and engineering disciplines did not go unnoticed. The consortium recommends that multidisciplinary *‘Beyond CMOS ‘ Erasmus Mundus programme* be set up to educate a new generation of student in future information processing concepts, including theory of information, binary and non-binary information processing, as well as training the young scientists and engineers in ‘Beyond CMOS’ technologies and design.

Introduction

This document contains the recommendations arrived at during the discussion and consultation process organised by the project NANO-TEC. It is anchored in the grand technological challenges in information processing, communications, based on memory and logic devices, circuits and architectures with a view to the time when CMOS scaling begins to loose some of its advantages over emerging nanoelectronic technologies. The question asked is then what comes after and will Europe play an important role in Beyond CMOS technologies?

The considerations and discussions in the preparative phase of this document took into account the potentials of working with and around CMOS and the possibility to deploy these future technologies "on top of" CMOS, provided suitable design innovations were available. The technological and design approaches that can be considered "disruptive" or far away into the future were also taken into account.

It can be argued that one of the main strength in Europe is the design capability. However, the interaction between the design and the technology research communities working in nanoelectronics, and especially in the Beyond CMOS area, is characterized by a diversity of terminology, modus operandi and the absence of a consensus on main priorities.

To prepare for the future, Europe needs a strong R&D competence in Electronic System Design to integrate technology in emerging design processes. It is in this context that the European Commission funded the Coordination Action project NANO-TEC, to help to establish a joint design and technology community in Nanoelectronics in Europe, from the combined technology and design perspectives in the field of Beyond CMOS. Thus the **scope** of NANO-TEC is basically two-fold:

(iii) To bring the design and technology community closer in Beyond CMOS research in order to strengthen R&D in Europe, and
(iv) To document the vision, recommendations and needs of the Beyond CMOS research community in the context of European-level research.

During the project, several groups of enabling future technologies were identified. Some of them are already more or less CMOS compatible, while some may be able to deliver in a hybrid integration approach with CMOS technology. However, others are disruptive and needs extensive research and development in technology and design, before assessing their usefulness. Needless to say, the coverage was non-exhaustive.

It is no secret that the European infrastructure for Beyond CMOS research, in terms of research facilities, small and medium-sized organizations with large infrastructures, is fragmented. Europe would benefit from stronger collaborations, with new common design rules and best practices among those in several R&D aspects including education and entrepreneurial activities. Through enhanced integration it is expected that investments in expensive equipment will be more efficiently utilized, and establishment of common educations, normalized access policies, forecasting and strategic planning will increase the impact of research in this field. Thus in addition to technology and design issues, the situation of research infrastructure for nanoelectronics was also analysed.

The **main activity** was based on interactive discussions in a workshop series. The four NANO-TEC workshops were:

5. *Identification of the main requirements for future ICT Devices*, Granada, Spain January 20–21, 2011,
6. *Benchmarking of Beyond CMOS device/design concepts*, Athens, Greece 13-14 October 2011, and
7. *SWOT Analysis of the Technology-Design Ecosystem***,** Lausanne, Switzerland, May 30-31, 2012.
8. *Discussion of draft recommendations,* Barcelona, Spain, November 6-7, 2012.

Each workshop drew participants from academia, research organizations, and industry, between 50-70 persons.

The list of all those involved in the process is given at the end of this report. Overall 133 people participated in the NANO-TEC workshops, many of them more than once and several four times. The regional distribution was as follows: 92% Europe, 7% USA and 1% Asia. The affiliation type was as follows: 45% academic, 40% research organisations, 11% industry and 4% others.

The **methodology** of the workshop was based on talks delivered by *invited speakers* on selected subjects and on the ensuing discussions. The strategy followed was first to consider a global nanoelectronics perspective, based on a thorough exercise carried out by the National Science Foundation and the Semiconductor Research Council in 2010 in which senior researchers from the USA, EU and Asia were involved. The topics included charge-based state variables, non-charge based state variables, new computing paradigms, ecosystem technology in Europe and progress in bridging the gap between technology and design.

Since one of the objectives of NANO TEC is to strengthen the fragmented nanoelectronics community it was important that the workshop format would reflect this objective. Hence, discussion time and effort was prioritized over long presentations. As a result, it was decided that the workshops should consist of a mix of short presentations and goal oriented discussions.

A *discussant* was assigned to each speaker with the task of highlighting the key points of the talk and to raise challenge questions. This would then set the stage for group discussions in which all workshop participants were encouraged to take part. In addition, a *Rapporteur* was assigned to each topic with the task of documenting the presentation and discussion. During the second workshop, discussions were further enriched in parallel working groups focusing on the topics presented. The discussions were documented by the rapporteurs.

Figure 1: Prof. Wolfgang Porod (Notre Dame University, USA) in his role as discussant of the presentation on solid-sate quantum computation given by Prof Jaw-Shen Tsai (NEC/Riken Research, Japan) at the Athens workshop.

Panels were organised to advance the discussions on building bridges between technology and design, in addition to specific presentations on design by invited speakers. Panel members presented their views in answer to specific questions, some prepared in advanced and others coming from the audience. The discussions were also documented in the records kept by the rapporteurs.

Figure 2: Prof. Dr. Sandip Tiwari (Cornell University, USA) and Prof. Dr. Lars Hedrich (Johann Wolfgang Goethe University, Germany) during a Panel discussion on Design and Technology.

Figure 3 illustrates the dynamics aimed at during the final workshop, to achieve a set of representative and widely shared recommendations suitable for forwarding to the European Commission.

To conclude, this report gathers the recommendations on Beyond CMOS research at European level to be submitted to the European Commission in January 2013 for consideration as a contribution to the contents of Horizon 2020. We are grateful to all who made possible the presentations, discussions, compilation, formulation and editing of these recommendations to strengthen Nanolectronics research in Europe. All the workshop material is available at: https://www.fp7-nanotec.eu/

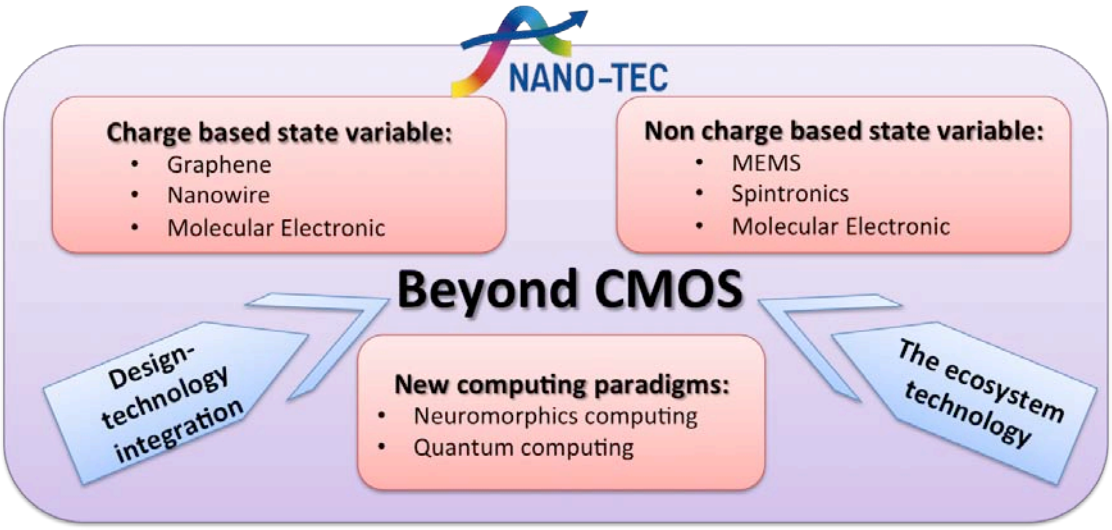


Figure 3: Schematic representation of the frame of reference for the 4th and final NANO-TEC workshop.

Charge-based state variable technologies

Rapporteurs: M Graef (TUDelft) and G Larrieu (CNRS-LAAS)

Abstract:

Emerging Beyond-CMOS device concepts based on charge as a state variable such as nanowire transistor, graphene transistor or molecular electronics may be potential candidates for replacing or extending CMOS are considered. In particular, nanowires, carbon-based electronics, specifically graphene, and a part of molecular electronics are discussed. In this chapter the state of the art is summarised and the technologies are benchmarked. Based on a SWOT analysis recommendations are formulated.

I. Introduction

Emerging Beyond-CMOS device concepts based on charge as a state variable such as nanowire (NW) transistor, graphene transistor or molecular electronics may be potential candidates for replacing or extending CMOS are considered.
New device technologies to replace or extend CMSO will be needed when the conventional architectures reach their physical limit as critical dimensions become smaller than 20 nm. Perhaps the most important issue will be power consumption constraints rather than miniaturisation. In this chapter we summarise the discussions on three charge-based state variables technologies, namely, nanowires, graphene and molecular electronics.

II. State of the Art

Nanowire transistors constitute an approach, which is entirely CMOS-toolset compatible, and can easily be implemented on SOI substrates. The DC performance for a gate-all-around (GAA) device illustrates the benefits of the multiple-gate FET, with enhanced control over short-channel effects. Circuits discussed include a 25-stage ring oscillator with transistor gate lengths within a range varying from 25 nm to 50 nm and a single inverter. These ring oscillators exhibit a delay in the range of tens of ps per stage, with a clear trend in speed vs. nano-wire size, and a speed mainly limited by access resistance and parasitic capacitances. Multiple channel architectures in planar or vertical integration have been implemented. Each approach offers its own advantages, compatibility with planar design for horizontal realisations, ultimately scaled and compatibility with bottom-up NW growth for vertical approach.

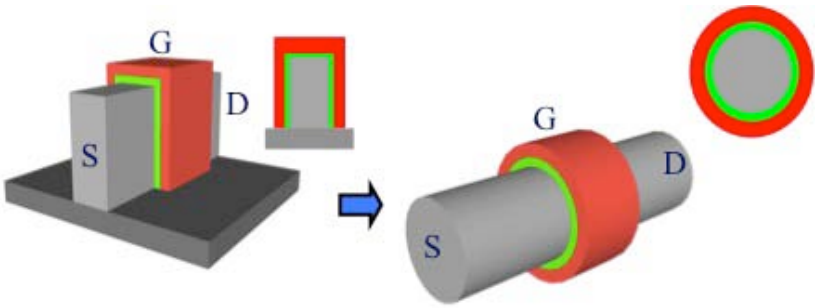


Figure 4. Schematics of multigate nanotransistors. Left: Triple-gate MOSFET and its cross-section. Right: NW-based MOSFET with a GAA (gate-all-around) and its cross-section. (G. Larrieu, Final NANO-TEC Workshop, November 2012, Barcelona).

Tunnel-FETs (TFETs) are CMOS toolset-compatible GAA vertical silicon nanowires. They offer a sub-threshold slope lower than the thermodynamic limit imposed by metal-oxide-semiconductor field effect transistors (<60 mV/dec). However, this extremely low sub-threshold slope is measured over a very limited voltage range. Due to the limited dimensions of the nano-wire, a limited amount of drive current, I_{on}, can be delivered by these devices. Thus, booster technologies, similar to those in place in current CMOS process flows, are implemented in TFETs. Nonetheless, the drive current remains a concern and requires further improvement. Several strategies can be implemented to improve I_{on}, including III-V materials (e.g., InGaAs homojunction) and Ge for bandgap engineering and effective mass reduction.

Graphene is a mono-layer material with very good mobility of up to 200 000 cm²/Vs at room temperature in vacuum, high saturation velocity (4×10^5 m/s) and, in the unmodified state, ambipolarity. The ambipolarity has a strong impact on gain being very small, if no bandgap is opened with additional techniques. These techniques, e.g. chemical modification, nano ribbons or bi-layer graphene, are currently under investigation. It is not clear, which will be the best approach without a degradation of other properties like the advantageous mobility. The resulting I_{on}/I_{off} ratio in the pure case is in the range of 2.10^2. On the other hand, the good mobility offers high-speed devices, which have been already demonstrated in the 300 GHz area and are expected to go up to 1 THz. This opens applications in the RF-analog range.

In **molecular electronics**, two main domains should be considered: single molecules, mainly devoted to fundamental studies at low temperature, and self-assembled arrangements, containing from 10^2 to 10^{10} molecules, which are more stable at room temperature. The molecular switch is the basic element for binary logic consisting of molecules having two stable states separated by an energy barrier. The stimuli can be light, heat, current or electric field. The state of the art in molecular switching is the following: intrinsic switching has been demonstrated, extrinsic switching brings new possibilities but many open questions remain on mechanisms and there are only few practical devices. Finally, molecular logic looks very promising on paper, however, it is difficult to realise partly because the synthesis is complex, the signal level of transport measurements is usually low and three or four contacts are required, the fabrication of which remains untamed.

III. Benchmarking and SWOT analysis

Nanowire-based transistors exhibit an enhanced control over short-channel effects. They are entirely CMOS-toolset compatible. They can be combined with other architecture and material approaches (III-V channel, Tunnel FET …) in order to achieve drastic power reduction (low V_{DD}, steep SS, immunity against SCE), i.e., low I_{off}. The possibility to grow high quality III-V homo or heterogeneous material on silicon is a strong advantage.

However, the challenges are numerous, for example the conformality issues, e.g., gate fabrication, on high aspect ratio nanowires or the large access resistance, which is fabrication strategy-dependent and configuration dependent (vertical vs. horizontal), due to the limited volume of semiconductor (per nanowire) or larger inner and outer fringing capacitances which limits f_T. In NW fabrication schemes, the top-down approach should provide high pattern density, nanowire (fin) pitch, and address the issue of strain relaxation in strained substrates after NW patterning.

Concerning bottom-up grown NWs, minimum NW diameters and NW density are still not competitive with top-down approach. Further developments are needed in order to make NWs

compatible with the top-down approach within the same process flow, which includes insulation, contacts, BEOL, etc. At present, the Tunnel-FET is currently the best candidate for steep slope switch. All-Si Tunnel FETs are limited by large bandgap and III-V heterostructure Tunnel FETs seem to be the best option when an abrupt junction is required. T-FET strengths are in low voltage (low power) and architecture compatibility. The challenges are in the experimental verification needed to optimize devices and in the theoretical modelling which needs improvements to enable prediction of the device performance. For example, the tunnel current is not gate length-dependent. Is this a strength or weakness? Is then a shift in the conventional set of Critical Dimensions needed or can the device asymmetry be used on purpose?

Graphene. Two-dimensional graphene films have generated a huge interest recently as an alternative for channel replacement material in FET structures. Graphene films are well known to behave as high mobility zero band gap semiconductors with high carrier mobilities.

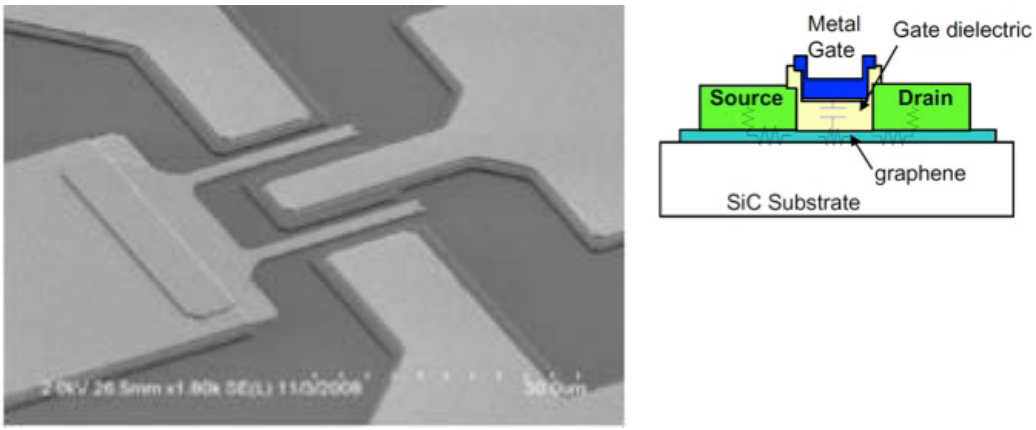


Figure 5. Self-aligned graphene MOSFET. Left: SEM micrograph of a device. Right: Schematics of the device cross-section. (J. Moon, 1st NANO-TEC Workshop, February, 2011 Granada).

From an integration point of view, graphene devices are planar and compatible with CMOS process. However, graphene devices face several critical drawbacks for logic application:

(i) Zero band gap: Because of the zero bandgap, devices implemented on large-area graphene channels cannot be switched off and therefore are not suitable for logic applications. When patterned to sufficiently small ribbon widths, the graphene ribbons begin to display a finite band gap resulting from quantum confinement (2D to 1D). Opening a band gap requires nanoribbons with sub 5 nm width coupled with very well-defined edges. Side roughness or dimension discrepancies would introduce huge mobility degradation and device-to-device variability. Another option to open the gap is to implement strain in large-area graphene, as demonstrated by simulation. From a practical point of view, it will require a global uniaxial strain exceeding 20%, which will be extremely difficult to achieve.

(ii) Variability (material and devices): At device level, it is observed that the mobility is dependent on the host substrate as well as on the gate oxide used (charged impurity scattering largely degrade the mobility).

(iii) Production quality material availability: many techniques with different influences on the final graphene structure exist, e.g. exfoliation, CVD, SiC and chemical synthesis. CVD appears as the most promising technique because it is scalable, transferable, is rapidly developing but the presence of defects in CVD graphene sheet lead to relatively low mobility values (10^3 cm²/Vs).

(iv) Electrical contacts: Contacting graphene device is more difficult than Si device, where one order of magnitude accuracy better than silicon is needed. Graphene seems to interact with anything, which can explain the impact of the environment on its high mobility. Yet, interactions are needed to form a good electrical contact, which seems physically difficult to solve.

Finally, many other applications in, e.g., the More than Moore area should have a higher potential than logic graphene transistors. These include (i) Optoelectronics, where optical applications range from ITO replacement (absorption 2.3% per layer), through solar cells to lasers. (ii) NEMS, low mass and large Young's modulus are promising characteristics for high frequency NEMS and (iii) Spintronics, using large spin coherence lengths, pure spin currents and large resistance signal for spin-dependent transport in spin-based logic devices.
There are several layered materials under investigation as alternatives to bi-layer graphene, e.g., MoS_2, however, these are at a very early stage of material research as is the field of topological insulators.

Molecular electronics: A molecular device offers natural nanometer scale, programmable functionalities activated by light, electromagnetic fields and temperature, and should, in principle, be a low-cost technology. For the single-molecule electronics no application is foreseen in a reasonable time-scale and thin-film molecular electronics tends to be regarded as plastic electronics with some products already commercialized and not exactly as a candidate for Beyond CMOS devices. Self-assembled molecular electronics was further divided into device families in which the self-assembled monolayers (SAM) act (i) as dielectric, (ii) as an active channel or (iii) as a non-linear switch. The most straightforward application for SAMs is to use them as gate dielectrics combined with organic conducting polymers. Transistor behaviour has been demonstrated at reasonable drain voltages but the drain current levels are still small, due to the low conductance per molecule, leading to requirement of relatively large devices. Simple logic gates have also been demonstrated with reasonable gain and low switching energy but performance are very low when compared to silicon MOSFET. In a SAMFET, where the SAMs form the channel of the FET, true saturation appears difficult to reach. Finally, the stability at room temperature remains very poor.

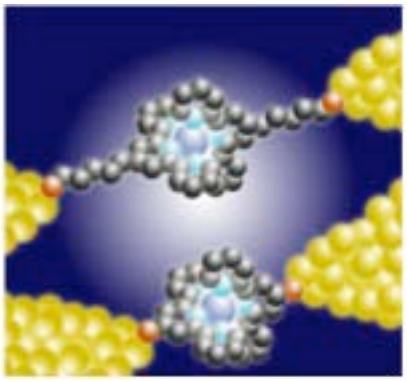


Figure 6. Single-molecule circuit element. (D. Villaume – 2nd NANO-TEC Workshop, October 13-14, 2011 Athens)

IV. Recommendations

Recommendation 1
With respect to nanowires, it is recommended to take measures towards a better theoretical understanding of the underlying physics and material science. In particular, the interplay of the physical properties of nanowires (electronic, optical, thermal, mechanical, e.g., strain,

interfaces, interface states, surface chemistry) and associated metrology, still require targeted investigation to ascertain their effect on device operation and on variability, both of which impact on architectures and integration prospects. The combination of nanowires technology with III-V compounds or alternative architecture (TFET) should be regarded as a promising beyond CMOS device, where a particular attention on the CMOS compatibility, for example III-V integration on Si platform, is required.

Recommendation 2

It is recommended to establish a non-zero gap graphene-nanoelectronic program with specific quantitative targets for graphene-based technologies to assess the possibility and test the suitability of fabrication and integration constraints for a combined Si-graphene new ICT technology, beyond sensors and single components. Other promising layered materials could be explored as alternatives. The exploration of device-relevant physics of topological insulators should be considered earlier rather than later.

Recommendation 3

With respect to molecular electronics for information processing of the post CMOS era, it is recommended to foster more interaction between the design and devices communities is essential to exploit the full potential of molecules properties. For analog applications, especially sensing, a connection between molecular electronics and flexible electronics may provide new possibilities with a better maturity level. It is essential that strong collaborations are established between physicists and chemists with the technology and design communities.

Non charge-based state variable technologies

Rapporteurs: J Ahopelto (VTT) and P Grabiec (ITE)

Abstract

The devices based on state variables other than charge discussed in the workshops included MEMS/NEMS switches and sensors and spintronic memories, spin logic and new phenomena, such as spin Hall effect and topological insulators. The MEMS/NEMS were not benchmarked mainly because of the application-oriented nature and diversity of the devices. Applications for Beyond CMOS were identified as low noise relays or power switches and in adding functionalities to future data processing systems through monolithic or heterogeneous integration. The main focus for spintronics was on various types of memories some of which are already commercially available. Spin logics is still to emerge with a promise of very low power consumption. The material issues are crucial and a new paradigm for architecture is needed, proving the importance of strengthening the technology-design community.

I. Introduction

The area of non-charge based devices covers a variety of devices and technologies out of which the most distinctive are MEMS/NEMS and spintronics.

MEMS/NEMS constitute originally a technology which, based on the fabrication processes dedicated to CMOS development, evolved in the last 30 years into its own, becoming a large field, mainly differing from the CMOS one by having the main focus on integrating diverse functions per chip instead of miniaturisation. Nowadays, both miniaturisation and increasing diversity exist in this technology, contributing not only to More than Moore but also, to some extent, to the Beyond CMOS domain.
Generally, MEMS/NEMS are produced using modified integrated circuit (IC) fabrication techniques and materials. The role of MEMS/NEMS in ICT can be seen as integrating sensors, oscillators and moving parts with added functionalities, either monolithically or more common, via packaging, i.e., heterogeneous integration together with integrated circuits. MEMS are a subject of strongly application-driven work and their realisation follows a path starting from the desired application, the required set of functions to be integrated, the properties leading to these functions and only then design and realization are carried out.
The use of the third dimension is one of the most important characteristics and must be exploited as much as possible. The main advantages are the possibility to: (i) integrate specific functions, (ii) enhance performance and (iii) miniaturise a complete system.
With MEMS it is possible to mimic the reality, mixing movement, forces and electrical stimulation, and this gives a possibility of testing, for example, cells in conditions very close to the real environment, as in the test of cardiomyocytes plated on a stretchable multi-electrode array, miming the heartbeat.

Spintronics can be considered as a rather mature, widely accepted technological concept in information storage based on giant magneto-resistance (GMR), tunnel magneto-resistance (TMR) or on devices for MRAM. Fundamental phenomena are well understood and form a solid basis for further developments based on recent discoveries.
An essential advantage of spintronics as a concept is the realization of non-volatile and low dissipation memory devices, since they rely only on spin dynamics. In current developments

spintronic devices, e.g., memories, can be integrated on CMOS, providing a compact solution for integrated circuits.
The earlier challenges related to memory aspects seem to be mostly solved. At present, the opportunity to define new perspectives, e.g., the use of classical spintronics in logic devices beyond information storage has to be taken into considerations. Novel aspects of spintronics based on new physical discoveries, i.e., spin logics, spin Hall effect, spin Seebeck effect, etc., are still in their infancy with real application opportunities to be identified.

II. State of the art and limitations

The role of **MEMS/NEMS** is probably better appreciated in the context of integrating sensors and functionalities, via monolithic or heterogeneous integration, with main-stream ICT devices. MEMS/NEMS development is strongly application-driven and the design and realisation are carried out based on the desired set of functions to be implemented and integrated, as shown in Figure 7.

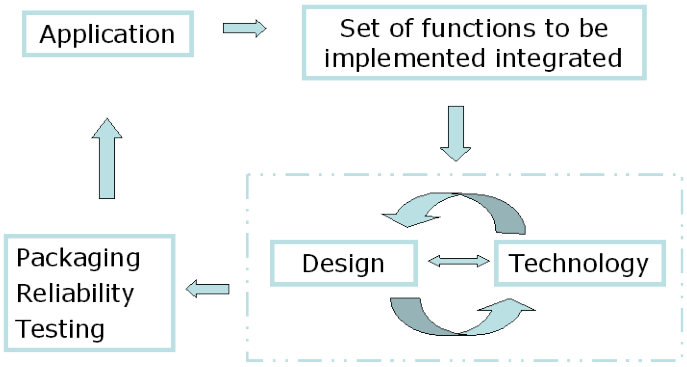


Figure 7. Schematics of the MEMS/NEMS realisation process.

In Beyond CMOS and More than Moore, it is switching that makes MEMS/NEMS attractive due to the promised low insertion losses, better non-linearity and lower noise compared to those of semiconductor switches. However, the electrostatically driven switches need typically very high actuation voltages, of the order of tens of volts. Recently, news from the Fraunhofer Institute for Electronic Nanosystems ENAS [1] reported switching time < 10 microsecond and 1 billion switching cycles. Also, attempts to reach low driving voltages have been reported. In Figure 8 a nanowire-based NEMS switch with operating voltage of 1-2 V is shown.[2]

An interesting long-term approach is to use conformational changes of molecules to provide NOEMS action. On/Off ratios of up to 7000 in conductance due conformation changes triggered by light have been reported.[3]

[1] 13.08.2012 Category: Ausgabe 47, Technology, Fraunhofer ENAS
[2] Y. Qian et al., Appl. Phys. Lett. 100 (2012) 113102.
[3] K. Smaali et al., ACS Nano 4 (2010) 2411-2421.

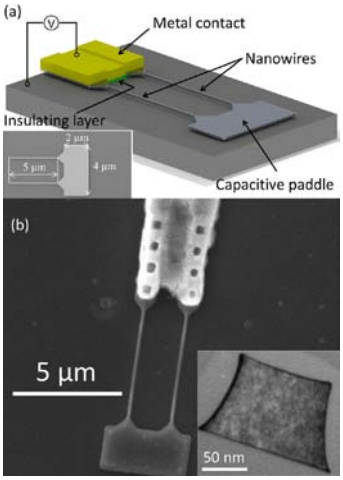


Figure 8. Nanowire-based NEMS switch with operating voltage of 1-2 V.

Although MEMS switches are highly nonlinear, circuits for data processing based on MEMS switches were not reported in the NANO-TEC workshops. In the literature some simple logic units can be found. In Figure 9 is shown an inverter realised using two MEM switches.[4] The operating voltage is again relatively high.

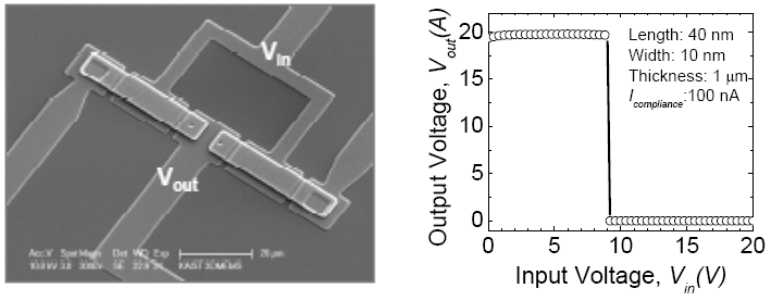


Figure 9. SEM image of an inverter based on MEM switches and the corresponding voltage transfer curve.

Regarding **spintronics**, memories based on GMR/TMR for HDDs have been in the market already from 90's, and MRAMs are commercially available. The emerging memory devices include improved MRAMs, i.e., spin transfer torque MRAM (STT-RAM) and thermally assisted switching MRAM (TAS-MRAM) which are expected to be commercially available in about five years. The integration of MRAM elements on CMOS circuits has been demonstrated, potentially enhancing the integration density at chip level. Furthermore, RF applications based on spin polarised magnetisation oscillations are promising for microwave generation and telecommunication.[5]

Candidates for spin logics include, for example, devices based on spin accumulation and switching of the direction of magnetisation, see Figure 10. These approaches can provide a new paradigm for computing architecture by reconfigurable logic circuits and by combining switching and memory elements. The implementation of these devices is expected to take still 5-10 years.

[4] Weon Wi Jang, O Deuk Kwon, Jeong Oen Lee, and Jun-Bo Yoon, IEEE Asian Solid-State Circuits Conference, November 12-14, 2007, Jeju, Korea.
[5] J. A. Katine et al., Phys. Rev. Lett. 84 (2000) 3149-3152.

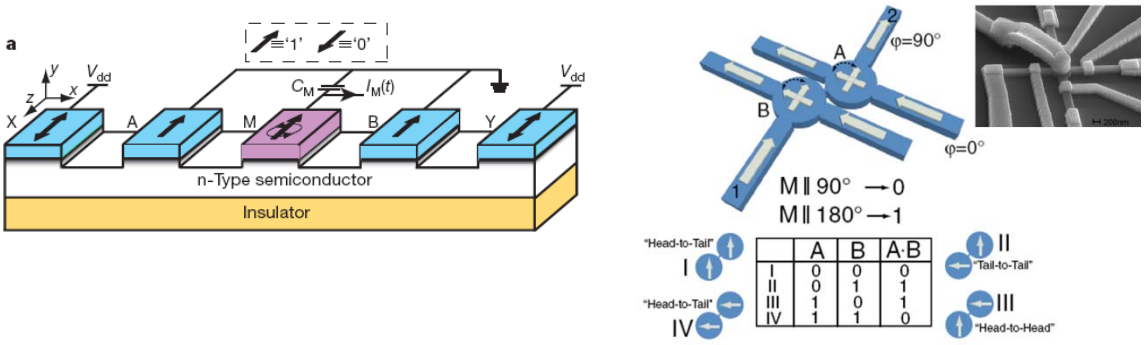


Figure 10. (left) Design of the reprogrammable magnetologic gate. The inputs are the magnetization directions of the contacts.[6] (right) Electrically programmable memory and logic device based on ferromagnetic (Ga,Mn)As semiconductor.[7]

Recently, experimentally observed spin Hall effect and topological insulators have shown potential for non-dissipative operation. However, applications can be only expected in time scales longer than ten years.

III. Benchmarking and SWOT analysis

Neither benchmarking nor SWOT analysis were performed for **MEMS/NEMS** devices with Beyond CMOS applicability in mind due to the strong application-dependent nature of the R&D work and the diversity of the devices. Below some of the IC-relevant comments from the workshops are summarised.
Microswitches with adequate and stable performance characteristics are necessary for relay-based ICs to be practical. The on-state contact resistance for this application should be as low as possible and device endurance should exceed 10^{14} on/off cycles, e.g., so that a relay-based microcontroller for embedded sensor applications could operate reliably for ten years at a clock frequency of up to 100 MHz and average transition probability of 0.01. A proper understanding of electromechanical (EM) contact physics, friction, and wear at the nanometer scale is essential for the development of reliable microswitch active power management, and logic applications. Since relays can be used in conjunction with MOSFETs, e.g., to gate the power supply to CMOS circuitry blocks, the co-integration of relays with CMOS circuits may be advantageous in some applications.
For integration the most important point is to manage complexity. Monolithic versus heterogeneous solutions must be considered. Performance has to be considered versus costs and versus volume. Integration is a key point, because the "user" wants a system with several functions.

The historic drive for **spintronics** originates from the hard disk drive industry. Within the domain of spintronics, mainly memory applications, representing near future applications, were benchmarked and long-term logic applications were briefly discussed. Applications can be found in non-volatile memories in which it will be hard to beat flash NVM (now at 19 nm) in device density, but for power consumption and speed, spintronics will be advantageous.

[6] H. Dery, P. Dala, L Cywinski, L. J. Sham, Nature 447 (2007) 573-576.
[7] S. Mark et al., Pys. Rev. Lett. 106 (2011) 057204.

Gate arrays (FPGA) are obvious applications for spin torque. This enables integration of logic and memory. Examples are video tracking and imaging.
The reliability related to noise, fluctuations and scaling may be an issue for thermally assisted MRAMs. There is no single solution possible, since this issue is associated with the "electromagnetic recording trilemma". Another interesting question raised was could spintronics be an option for spatial computing (rather than in the time domain)? This was considered to be a rather "esoteric question", which would require substantial exploratory research.

Spintronics holds high potential for memory applications, i.e., the HDD market. This is very close to industrialization, with a timeline of a few years, and as such it does not qualify for 'Beyond CMOS'. Today, most resources go to STT-MRAM. Spin torque is unlikely to replace conventional memories, but it appears as a suitable option for some (large) niches, e.g. applications requiring flash/DRAM combinations. Spintronics can be considered as a 'tool box' that provides an entry point for other spin transfer device options. Within the domain of spintronics, novel devices concepts based on magnonics and spin caloritronics have a high potential for various applications (e.g. microwave detectors). Benchmarking for these devices has yet to be done.

IV. Recommendations

Recommendation 1
Research related to spintronics in the field of Beyond CMOS should focus in the short term on research closer to industrial applications. These include RF components with increased power output, demonstration of phase-locking of tens of oscillators and fundamental understanding of nonlinearities. Spin logics forms another potential field, especially for low power devices. Magnetization switching and pure spin current generation are interesting candidates for non-dissipative information processing. Here, further material research and design development are needed.

Recommendation 2
To develop truly disruptive new concepts in the long term it is suggested that spin Hall effect and topological insulators will be thoroughly investigated. For the devices, focus and resources on materials and device design is required.

Recommendation 3
Molecular spin clusters have great potential for encoding quantum bits, and they are considered to be emerging candidates among solid-state electron spin systems for the development of quantum architectures together with nitrogen vacancy centres in diamond. Thus it is recommended to include molecular spin clusters in future programs on quantum information processing.

Recommendation 4
It is recommended that a future program on non-charge state variables contains a strong technology component to address the outstanding technology-related issues. These include large variance in physical and electronic properties, interconnecting nanoscale objects (a common issue for almost all low dimensional and nanosized structures), and solve the problems related to reliability and temperature stability.

Recommendation 5

High performance and stable NEMS switches are necessary for relay-based ICs. The on-state contact resistance should be as low as possible with reliability exceeding 10^{14} on/off cycles. Reliability issues for NEMS switches include permanent stiction (nano-scale physics), contact wear and plastic deformation, and environmental effects. It is recommended that any future program on NEMS should include a strong element towards the understanding of contact physics, friction and wear at the nano-scale, all of which are essential for the development of active power management and logic applications.

Recommendation 6

To increase the functionality of Beyond CMOS devices via heterogeneous integration with NEMS, further miniaturisation through technology development and especially improved design and simulation tools to include the nano-multi-physics are essential and should form part of a next research program. The increase complexity must be considered taking into account reliability, production and cost related issues.

Technology and Design of new computing paradigms

Rapporteurs: G Fagas (Tyndall), C M Sotomayor Torres (ICN), G Wendin (Chalmers) and D Winkler (Chalmers)

Abstract:

Of the several alternatives to prevailing computational techniques, this chapter considers two of them: quantum computing and neuromorphic computing. They have been discussed in the frame of first following a hybrid approach to explore the compatibility with Si technologies as a first step and later in the context of a change in computation paradigms.

I. Introduction:

Unconventional methods for information processing (non-digital, non-Turing) hold great promise for future opportunities in solving a range of problems not easily handled by digital computers of today. Examples of current interest are quantum computing, neuromorphic computing, chemical computing, molecular computing, biocomputing and amorphous computing, some of them providing opportunities for self-assembling and self-organising computers[8]. In this chapter we will focus on quantum computing and neuromorphic computing.

Quantum computing: Although only a fairly limited number of algorithms are available for quantum information processing (QIP), the technology may have a fundamental impact on society and science. The field is moving quickly, and any success in this area would find early adopters. Opportunities and challenges of today include the possibility to engineer a small functional quantum system to demonstrate its superiority to classical computers and to implement codes to demonstrate quantum error code correction (QEC), necessary for large-scale applications, respectively. There are no quantum computers yet. QIP experiments are going on with up to 15 (spin) qubits in molecules (NMR), ion traps, optical lattices and solid-state devices and, although there is steady progress in many areas, large-scale quantum computing (QC) is far away. Still, competitive quantum simulation (QS) may be around the corner.

The present technological focus is on hybrid systems to take advantage of the best properties not found simultaneously in pure systems, namely, high speed (operation) and long coherence time (memory).

The present QIP focus is on quantum simulators (QS) to simulate static and dynamic properties of small physical and chemical systems with useful accuracy. In the long run, solid-state systems may have an edge via technological scalabililty. Solid-state qubits comprise: superconducting Josephson-junction (SC-JJ) based (charge, flux and phase), quantum dot (QD) (charge, spin), and impurities in crystallites and in molecules (electron spin and nuclear spin). In principle one might also add atoms and ions in solid-state microtraps, probably essential for future large-scale systems. Currently, the most successful solid-state approaches are *JJ-based Transmon qubit - resonator (cQED) systems (30 mK)* and *spin-based NV centres in diamond (300 K).* The recent development is impressive and promising.

[8] Expert Consultation Workshop 30 November 2009 on "Unconventional Formalisms for Computation", ftp://ftp.cordis.europa.eu/pub/fp7/ict/docs/fet-proactive/shapefetip-wp2011-12-05_en.pdf

At present the main areas of activity at the international frontline are teleportation, measurement-based feedback and feed-forward, quantum error correction (QEC) and simulation of quantum system. Of these quantum error correction (QEC) is of critical importance.
A US collaboration among IBM and others is determined to develop and test a superconducting cavity-QED approach with 13 transmon qubits + ancillas and 4-qubit parity measurements within 4 years. Together with similar efforts in Europe, this may determine the roadmap for the next 5-10 years.

Neuromorphic computing. Based on the theory of nonlinear dynamic systems, Professor Leon Chua (UCB) introduced the concept of memristive devices in 1970s. Like an ordinary resistor, a memristive device would create and maintain a safe flow of electrical current across a device, but unlike a resistor, it would "remember" charges even when it lost power. This would allow it to store information, i.e., serve as computer memory. In May 2008, Hewlett Packard announced that redox-based resistive switches, which are investigated since the late 1990s, can be elegantly described as memristive devices. One of the potential key applications of memristive devices is in Neuromorphic Computing. Memristive devices fall generally under four types including inorganic and organic devices. The latter has time scales that place it within the Beyond-CMOS device concepts.

Neuromorphic computing can be implemented, in principle, in a number of different physical systems, from CMOS circuits to self-assembled molecular networks. It might provide the necessary tools to develop the robotics area, associative learning, efficient image processing, just to mention a few examples. Needless to say, in any of these applications, the interfacing to other technologies will be of utmost importance and this will have to be addressed along the full evolution chain of this development. Neuromorphic computing must address dissipation, co-firing and fan- out. Scalability bounds need to be defined. Much can be done to build a theoretical framework, to develop new architecture concepts and to optimise inter-connectivity at neural level thereby improving the understanding of processes related to learning and transfer of training. The plasticity aspect can probably be tackled also by working on the pulse shape rather than on the material, in order to obtain more states with a controlled potential.

II. State of the Art and Limitations

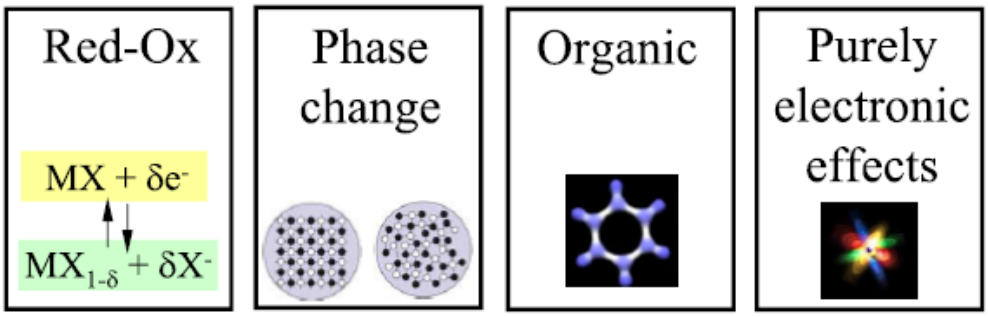
Quantum computing has been heralded as a future technology for generic quantum information processing since the 1980s, without physical limits and able to extend the range of soluble problems well beyond those that classical computing can tackle.

However, no quantum computer exists at present and efforts focus mostly on simulations of static and dynamical properties of small physical and chemical systems with useful accuracy as well as on experiments involving only a few qubits. Nevertheless, important progress has been achieved within last years in the US and in Europe, in experiments involving several qubits using a Josephson Junction approach, allowing a measurement-based state initialization and measurement-based feedback. These experiments required cryogenic temperatures, which may not be a serious issue but one needing a paradigm shift. The possibility to implement a solid state QC concept at a room temperature using defect structures or quantum dots in diamonds and in III-V semiconductors is also a promising approach. A simple utilization of CMOS-based technology to implement QC is unlikely. The most promising approach seems to be based on integration with focus on hybrid systems combining processing, memory and

communication functions. The main strength of this approach consists in an enormous number of parallel computation, which may be performed taking advantage of the quantum nature of qubits and superposition. Besides, a potential technological scalability may allow for future development of the realistic QC systems. On the other hand, important and difficult problems do not yet allow a technical implementation of the QC systems. For example, the feasibility of implementation of quantum computation in systems operating at room temperature is the key obstacle and the coherence time is still too short to produce meaningful computation/simulation. Furthermore, solid-state realisations lag behind other QC implementations like ion traps and there is no generic computational functionality. Thus, there is a need to elaborate new algorithms to broaden the applicability of QC to broader domains. QC has to be still considered as a basic science, however, the next few years are expected to be decisive for future development of this, otherwise, very promising technique. A recent development on a SOI based platform for quantum optical interferometry has demonstrated the prospects of room temperature Si-compatible quantum chips for quantum computation[9].

In conventional computers logic and memory functions are located in different parts of the circuit and each computing unit is only connected to a handful of neighbouring units. In contrast, the brain has neurons connected to each other by synapses, which act as reconfigurable switches that can form pathways linking thousands of neurons. This large connectivity equips biological systems with energy-efficient highly parallel processing power that allows learning and is very suitable for certain tasks such as pattern recognition. The key element in this process is the adjustable synaptic weight between two neurons. In recent advances in neuromorphic computing, this role is played by a two-terminal device termed memristive device, the conductance of which can be continuously tuned.

The realisation of memristive devices at the nanoscale took off with the work of the IBM labs in Zurich in 2000. In general, all resistive switching devices are memristive devices and can be classified under four types as shown in Figure 11:



(i) (ii) (iii) (iv)

Figure 11: Four types of memristive devices considered as resistive switches. (i) Red-Ox where resistance changes are due to several processes including ionic motion and thermal effects[10]. (ii) Phase change[11], which together with Red-Ox these kinds are mainly defect mediated. (iii) Organic memristive devices with the potential for additional functionalities (e.g., light) are based on bottom-up self-organization and present high density. (iv) Purely electronic-based memristive devices with no change in structure of the device. These include spin devices with a multi-tunnel junction using spin-torque effects (multi-state switching already demonstrated by Chanthbouala et al[12] and the ferroelectric memristive device[13].

[9] D Bonneau et al, New J of Phys, http://arxiv.org/abs/1201.6537
[10] M-J Lee et al, Nat Mat 2011; Ag Aono Adv. Mat. 2012
[11] Kuzum et al Nanolett 2011
[12] A Chanthbouala et al, Nature Nano 2011
[13] J. Grollier, https://www.fp7- nanotec.eu/node/560.

Applications of memristive devices to date include demonstration as digital memory, logic and neuromorphic functions. Large improvements have been achieved in memristive memories in terms of switching speed (10ns with less than 1pJ power consumption), reliability (10^{11} cycles) and OFF/ON ratio (10^{7}). Logic functions and reconfigurable architectures have been demonstrated and with higher ON/OFF ratios memristive device can be used as latches. There is no demonstration yet of operational mixed memristive/CMOS cognitive chip, however, small demonstrators exist. A hybrid crossbar/CMOS system can reliably store complex binary and multilevel 1600 pixel bitmap images using a new programming scheme and emulation of the Spike Timing Dependent Plasticity has been achieved.

III. Benchmarking and SWOT analysis

The speed of quantum computers is estimated as 2^{N}, while the energy consumption calculations will need to take a system approach.

With respect to architecture and integration potential the target is to maintain current de-coherence rate and implement corrections with a reasonable increase in the number of qubits. The timeline to reach between 10 to 100 qubits is expected to be less than 10 years.

Memristive devices were benchmarked for two kinds of devices:

(i) Memristive devices as digital memories
(ii) Memristive devices as analog memories, examples of which are artificial synapses.

If massive parallel architecture became possible then speed would not be important. The same would apply to retention time.

While inorganic memristive devices for neuromorphic computing are CMOS-compatible, the organic memristive devices are seen as Beyond CMOS in terms of time scales. Nevertheless, the original term “memristor” is controversial in terms of its definition, even the claim of being the 4^{th} element in electronic circuits. It seems that much remains to be understood among memristor experts themselves. However, independent of its description by the theory of nonlinear dynamic systems researcher have to work on the microscopic understanding of memristive mechanisms of these devices, in order to enable a better comparison of the different types and allow function optimization.

IV. Recommendations

Recommendation 1

New computing paradigms are required for information processing including, for example, quantum computing, neuromorphic computing, chemical and molecular computing, biocomputing. Present effort on unconventional information processing is fragmented and many approaches are developed in parallel, independently and uncoordinated. A well-defined need was identified, translated into a recommendation to set up a future transversal research project (IP-cluster; super “IP”), which will favour multi-disciplinary cooperation and coherent problem definitions and outcomes of unconventional information processing. A cross-disciplinary “super IP”, funded to the tune of, say, 10-20 MEuro/year for a period of 5 + 5

years, is essential as targeted R&D project, instead of a loosely organised program. Within such a "super-IP", quantum computing and neuromorphic computing should be embedded in digital environments via digital-analogue hardware and software interfaces, in order to create useful hybrid systems to, e.g., interact with human users and be capable of adaptive learning. Such a "super IP" should pave the way for important commercial applications in 5-10 years.

Recommendation 2

The contributors highlighted the importance to analyse, benchmark and develop application areas where solutions to computationally hard problems may be possible. The focus should be on research areas that unconventional computing could solve or give a more efficient answer in terms of energy and time. Research areas could include unsolved mathematical problems and/or applications that address the societal challenges of health, energy, security and environment. Examples of such applications include:

- Image recognition characterised by the complexity of an image, time and energy required to perform the task;
- Data-mining of complex big data that are currently gathered by distributed smart systems (here, e.g., the combinatorial efficiency of quantum computing or associative learning of neuromorphic computing could be very useful);
- Finding repeated patterns in sequence of events (e.g., in monitoring internet activity);
- Creating meaningful outputs from input sequences (e.g., stream of words or musical patterns).

In all cases special attention must be paid to the chain: theory-design-systems-applications.

Recommendation 3

Concerning neuromorphic computing using memristive devices, the material and physical changes required for operation need to be studied with respect to defect tolerances, reproducibility and the reversibility of the thermodynamic processes involved. Furthermore:

- New architecture concepts will be needed in order to take into account that each memristive device will vary and therefore can process information differently. New architecture will also be needed to optimise inter-connectivity at neural level thereby improving the understanding of processes related to learning and transfer of training.
- At present, for switching functionality, the I-V loops indicate large dissipation. Therefore, local heating, which impacts power consumption, needs to be addressed, as well as co-firing and fan-out and scalability bounds need to be defined. Highly non-linear processes are involved, which requires an adequate theoretical framework.
- The plasticity aspect can probably be alternatively tackled by working on the pulse shape rather than on the material, in order to obtain more states with a controlled potential. For this, active memristive devices will be needed to test algorithms and their transferability.

Potential technologies for Beyond CMOS devices not covered in the NANO-TEC workshops

J. Ahopelto (VTT)

Not all potential candidate technologies for Beyond CMOS were discussed in the workshop series. Below are a few examples of rather disruptive approaches, all of them belonging into the category of non-charge based devices for information processing. They all have in common long term approaches and in most cases the concept have been barely demonstrated.

The *quantum cellular automata* (QCA) concept was developed at the University of Notre Dame in early 90's. [14] The structure and a configuration for an inverter are shown schematically in Figure 12. Electrostatic interaction between the four or five quantum dot building units transfer the signal with no charge transfer between the units, leading to very low energy consumption. Different logical functions can be designed by combining the basic units. Logic functions such as OR, AND and, for example, a full adder have been outlined. Realisation of the devices has proven to be very challenging and only a few reports are available in the literature.[15]

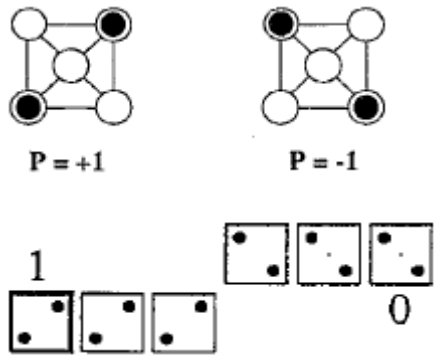


Figure 12. Basic building block of a quantum cellular automata and an outline for an inverter [from Ref. 15].

QCAs and logic operations have also been realised using nanomagnets[16]. An example of such a realisation is shown in Figure 13.[17] The advantage of nanomagnet QCAs is that the circuits operate at room temperature, are low power and are still relatively fast, working in the GHz range.

Thermal computation uses temperature as state variable. Diodes[18] and three terminal devices, thermal transistors,[19] have been envisaged and at least diodes have been realised.[20] A more advanced approach is based on phonons and magneto acoustics to control the polarisation of the phonons, following the ideas for optical computing but replacing the photons by phonons.

[14] C. S. Lent, P. D. Tougaw, W. Porod and G. H Bernstein, Nanotechnology **4** (1993) 49-57.
[15] C. Single, R. Augke, F. E. Prins, D. A. Wharam and D. P. Kern, Superlattices and Microstructures 28 (2000) 229-334.
[16] R. P. Cowburn and M. E. Welland, Science 287 (2000) 1466-1468.
[17] A. Imre, G. Csaba, L. Ji, A. Orlov, G. H. Bernstein, W. Porod, Science **311** (2006) 205-208.
[18] Baowen Li, Lei Wang, and Giulio Casati, Phys. Rev. Lett. 93 (2004) 184301.
[19] Lei Wang and Baowen Li, Phys. Rev. Lett. 99 (2007) 177208.
[20] W. Kobayashi, Y. Teraoka, and I. Terasaki, Appl. Phys Lett. 95 (2009) 171905.

Several logical gates have been designed and prospects for efficient computation look promising.[21]

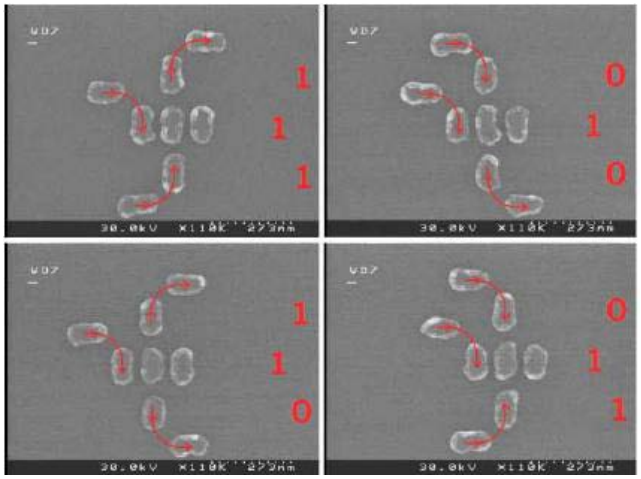


Figure 13. Three input majority gates for logical operation using nanomagnets. The gates can act as two input NAND or NOR gate depending on the input configuration [from Ref. 17].

Even more exotic state variables are water droplets on superhydrophobic surfaces and realisation of *droplet logics*.[22] On a superhydrophobic surface the droplets can collide and bounce or coalesce depending on the collision parameters. In Figure 14 are shown the schematics and realisation of a configurable AND/OR gate. Inverters and Flip-Flop memories have also been demonstrated.

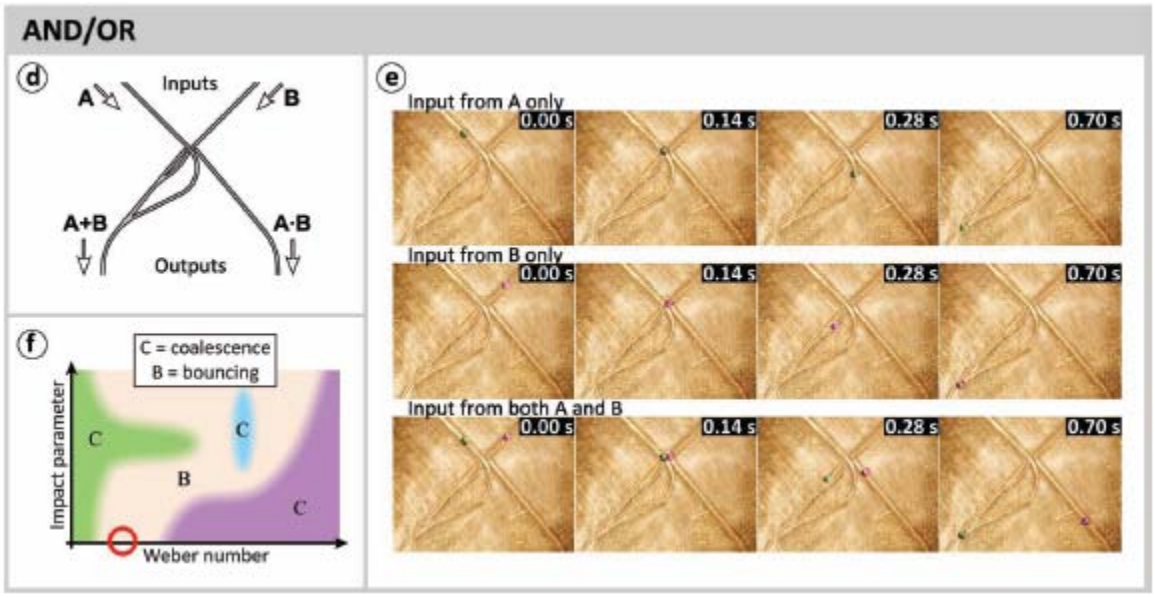


Figure 14. d) A schematic showing the AND/OR logic gate connections. The two inputs are situated at the top of the image and outputs at the bottom. e) A series of images demonstrating the AND/OR gate operation. The droplets have been colored via image editing for clarity. The corresponding video is available in Supporting Information (Video S4). f) The selected collision conditions (red circle) are shown qualitatively in the Weber number/impact parameter diagram [from Ref. 22].

[21] S. Sklan, J. C. Grossman, in *Son et Lumière: from microphotonics to nanophononics*, Les Houches, France, from September 17th to 28th, 2012.
[22] H. Mertaniemi, R. Forchheimer , O. Ikkala and R. H. A. Ras, Adv. Mat. **24** (2012) 5738–5743.

Recommendation 1

It is recommended to continue the exploration of novel computation approaches in general. In particular a comparative and dynamic analysis of the interaction between design and the emerging technologies as an integral part of the R&D efforts would provide Europe with a valuable and probably decisive advantage.

The ecosystem technology in beyond CMOS in Europe

Rapporteurs: A Cappy (CNRS) and T Swahn (Chalmers University)

Abstract

This chapter deals with the ecosystem technology for 'beyond CMOS' in Europe. In 'Beyond CMOS technologies', Europe is suffering from the absence of a global and consistent R&D approach associated with a sometimes fuzzy role of the three main types of players: academia, research organizations and industry. Thus, the dispersed nature of the R&D activities in Europe continues to set limits to the creation of a visible effective impact, to encourage non-constructive competition and the concomitant waste of resources. This section puts the proceeding technology sections into a birds-eye perspective, points out discrepancies and gives recommendations to catalyse cooperation within Europe. The critical issue in 'Beyond CMOS' research is the availability and access to advanced technologies. The technological European landscape is rich with many academic-like medium-size facilities and industry-compatible large-scale facilities in research organisations. However, access to these facilities should be improved by more efficient networking at the European level. The ecosystem would benefit from structuring and promoting regional ecosystems as well as intra-European mobility of researchers and entrepreneurs. Active networking promotes this as well as the spread of best practices. We therefore propose suitable and long-term financial support to European open-access programmes, among smaller infrastructures as well as access to the large-scale facilities. [23] In addition, industry should contribute more efficiently to the identification, through system-driven practices, of relevant long-term fundamental research topics needed in the value chain. Finally, the creation of a multidisciplinary 'Beyond CMOS' Erasmus Mundus programme to train a new generation of student in 'Beyond CMOS' technologies is recommended. Altogether, this contributes to European integration and competitiveness.

I. Introduction

A critical issue in nanoelectronics is the availability of, and future access to, advanced technology. In respect to this, a clear definition of the roles of the respective players is needed in order to avoid a situation of non-constructive competition and waste of resources.

In general, the ecosystem technology (Figure 15) has three types of players:

- Academia, with a R&D horizon > 6 years and technology readiness levels (TRL) 1 to 4, i.e., *basic understanding*, test and validation of innovative architectures, materials and processes *for future ICT*.
- Research Institutes (RIs, Integration Centres), with a R&D horizon between 3 and 6 years and TRL 3 to 7, i.e., Technology *implementation* and the assessment towards Production Equipment; *development* of high performance components
- Industry, with a R&D horizon < 3 years and TRL 6 to 9), i.e., technology *research, innovation and exploitation*; process introduction and continuous improvement with innovative approaches (yield, reliability,…).

[23] *Representatives from the NANO-TEC project have together with other European partners submitted several proposals to the EU open consultation initiative: "Topic proposal for integrating and opening existing national research infrastructures". These proposals were coordinated, to different extent, and submitted by RENATEC, Myfab, NorFab, and the TRAIN^2-project group through CNRS-LAAS.*

A relatively large number of academic and national laboratories can provide single device and circuits of little complexity, as well as sophisticated characterisation techniques for nanoscience and nanotechnology, including nanoelectronics. However, with only a few exceptions, academic laboratories are unable, or not sufficiently motivated, to integrate their process steps into a reliable and reproducible device fabrication process flow, or to combine their characterisation expertise with manufacturing know-how. This does not mean that academic laboratories cannot be involved with industry in high TRL projects. Strong interactions between academia and industry in high TRL projects are frequent and the input of academia is often significant. It should also be noted that even if academic facilities are numerous and spread out over most regions in Europe, regional clustering takes place between academic facilities. These clusters could simplify interaction between regional, national infrastructures of remote/smaller countries and the large institutes.

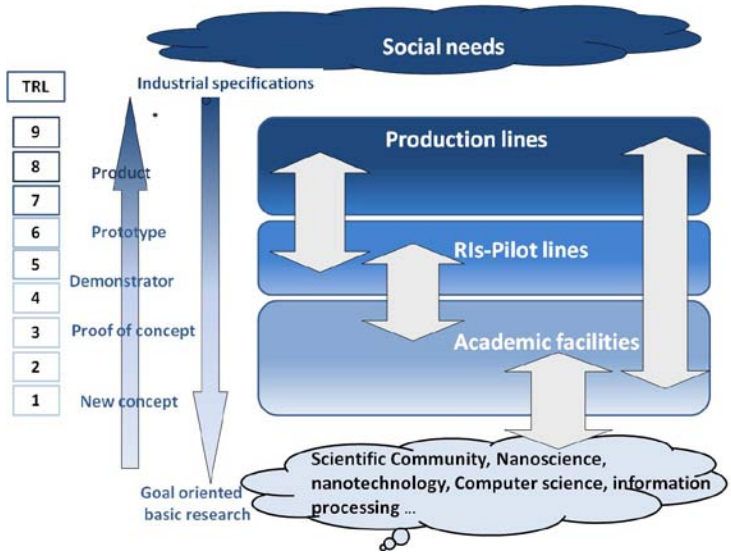


Figure 15. Ecosystem technology in Europe, showing on the left the technology readiness levels (TRLs).

Research institutes could play a pivotal role by providing cost-effective technological/design infrastructures for nanoelectronics R&D to academia and industry. They also could take into account the need for focused experiments aimed at gaining basic knowledge of material/device properties and their use in stable state-of-the-art fabrication technologies. This requires early validation of new concepts in collaboration with academia and industry.
Industry needs to introduce innovations that involve new process steps or materials only after they have been fully proven, and then needs to do so in a fast and efficient way in order to satisfy time-to-market and cost-to-market constraints.

In Beyond CMOS technologies, the players are mainly academia and research institutes since non-conventional approaches are investigated, probably limiting the motivation of industry to get involved. However, the role of industry is important:

- To define expectations for ultimate CMOS technology, applications and services (> 2015),
- To contribute to the identification, through system driven practices, of relevant long-term fundamental research topics needed in the value chain and
- To provide critical feedback to research institutes and academia.

II. Technology landscape in Europe

Below Academic-like small, medium and large facilities with clean rooms of typically 500-2000 m^2 capable of handling up to 6'' wafers for nanoelectronics R&D are listed.

1. Austrian Institute of Technology (AIT, www.ait.ac.at), Austria
2. Catalan Institute of Nanotechnology (www.icn.cat), Spain
3. Cavendish Laboratory, University of Cambridge (www.phy.cam.ac.uk/), England
4. Danchip/DTU (www.danchip.dtu.dk/English.aspx), Denmark
5. EPFL NanoLab (www.nanolab.epfl.ch/), Switzerland
6. Forschungszentrum Jüelich (FZ-Jüelich, www.fz-juelich.de), Germany
7. IMB-CNM (www.imb-cnm.csic.es/), Spain
8. IMEL/NCSR Demokritos (www.imel.demokritos.gr/index.shtml), Greece
9. INL and INESC NM, Portugal
10. Institute of Electron Technology (www.ite.waw.pl/en/), Poland
11. Myfab, the Swedish Research Infrastructure for Micro and Nano Fabrication (www.myfab.se)
12. NorFab (www.norfab.no/), Norway
13. NanoLabNL (http://www.nanolabnl.nl/), The Netherlands
14. Spanish Nanofabrication Network NANOLITO (http://www.unizar.es/nanolito/), Spain
15. RENATECH (www.renatech.org), France
16. Royal Institute of technology (KTH) (www.kth.se/en), Sweden
17. RWTH Aachen (www.fh-aachen.de), Germany
18. SINTEF (www.sintef.no/home/), Norway
19. Tyndall Institute (www.tyndall.ie) Ireland,
20. UC Louvain (www.uclouvain.be), Belgium
21. University of Glasgow (www.gla.ac.uk), UK
22. University of Southampton, England
23. Technical Research Centre of Finland VTT (www.vtt.fi), Finland

Research Institutes with large size clean room of several 1000's m^2 with 200-300 mm lines:

1. IMEC (www.imec.be), Belgium,
2. LETI (www.leti.fr) France,
3. Nanocenter Dresden (includes the Fraunhofer Institutes IPMS and IZFP) (www.nanodresden.de), Germany

III. How to improve the ecosystem technology

Or strengths and weaknesses of the ecosystem technology.

Whilst European R&D is generally very active in Beyond CMOS technologies, it is generally agreed that the transition from ideas arising from basic research to competitive products is a weak link in the European nanoelectronic value chain.

This situation, namely the gap between basic knowledge generation and the subsequent commercialisation in marketable products, has been commonly identified across Europe and is known in broad terms as the "Valley of Death" issue (Figure 16).
This “Valley of Death” has also been identified in several countries, including the USA, China and Taiwan. These countries have established coordinated programmes in strategically important areas that cover the full innovation chain addressing basic and applied research, demonstrators, standardization measures, deployment and market access. Thus, in Europe, targeted instruments addressing all technology readiness levels of competing technological approaches, from basic science through proof-of-concept and prototypes, to large-scale demonstration actions and public procurements will help to overcome the “Valley of Death” and enhance deployment.

Crossing the “valley of death” in Beyond CMOS technologies in Europe requires the delivery of solutions to the three successive pillars involved in this crossing.

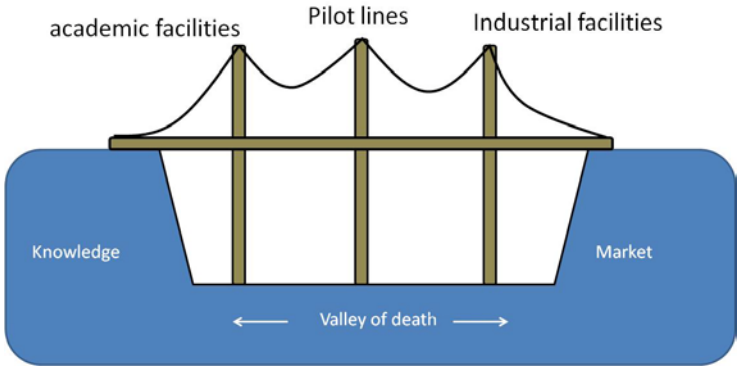


Figure 16. Valley of death problem showing the position of the three pillars relevant ot the nanoelectronic ecosystem technologies.

For Beyond CMOS technologies, which are by definition technologies of the future with a potential huge impact, to identify the foreseeable difficulties in crossing the ‘valley of death’ and to propose actions to reduce of suppress them, is mandatory if Europe is to play a role in this domain.

The first pillar, **academic facilities**, consists of taking best advantage of European scientific excellence and infrastructure in transforming the ideas arising from fundamental research into competitive technologies. These should be both shown through proofs of concept and be proprietary, that is, protected by patents. It is these patents that will guarantee the future freedom to exploit these technologies by European industry.

The second pillar, **Pilot lines**, allows the use and exploitation of these beyond CMOS advanced technologies to make innovative and performing European process and product prototypes competitive at world level. This requires first putting in place pilot lines having technology prototyping facilities to enable the fabrication of innovative product prototypes.

The third pillar, **Industrial facilities**, should allow, starting from product prototypes duly validated during the demonstration phase, the creation and maintenance of attractive economic environments in EU regions, based on strong eco-systems and globally competitive industries.

IV. Recommendations

The dispersed nature of the R&D activities in Europe generally limits the creation of visible effective impact. Especially in nanoelectronics, Europe is suffering from the absence of a global and consistent R&D approach.

Furthermore, for more than twenty years, numerous initiatives (CATRENE, ENIAC, AENEAS, PRINS, SINANO, ENI2…) were developed in order to organise, optimise, coordinate and structure the nanoelectronic research community. As a consequence, the landscape is rather complicated and none of these initiatives include Beyond CMOS technologies as such. Thus, it is vital to identify the key players, to reinforce alliances among them and to organise collaborative research programmes with access to the best technological infrastructures in Europe.

In Beyond CMOS research, the needs are manifold:

- Access to specific equipment (lithography, deposition, etching, metrology…) to demonstrate the proof of concept of a beyond CMOS device,
- Access to modelling and design tools and
- Access to pilot line to demonstrate the CMOS compatibility of, eg, new switches.

One important consideration is that, contrary to More Moore research, research in Beyond CMOS requires access to more flexible facilities, which allow the introduction of materials considered 'exotic' in a CMOS line.

Recommendation 1

The first recommendation concerns *a European infrastructure network*, to coordinate all the advanced academic technological facilities having a significant activity in beyond CMOS research, in a European network with one and only one entry point in each country. Each entry point would have as part of its mission to represent/structure its national facilities (figure 17)[24]. Through common access rules and similar organisation, the rationale is to take advantage of the complementarities of the 'beyond CMOS' research infrastructures and to capitalize on the fields of highest expertise of each member.

In order to avoid a new structure, this network should be coordinated by an existing initiative. This network will be complementary to the facilities of the RTO and tightly linked to them in order to allow a smooth crossing of the 'death valley'.

[24] *See previous note on the EU open consultation.*

Figure 17. European network of academic nanofabrication for nanoelectronics facilities.

Recommendation 2

The second recommendation concerns education and training and is to create a multidisciplinary 'Beyond CMOS ' Erasmus Mundus programme to educate a new generation of student in future information processing concepts: theory of information, binary and non-binary information processing, quantum computing, neuromophic computing, etc. In fact the curricula have to have strong physics and chemistry contents.

Recommendation 3

The little or no *feedback from industry* is a weakness in Europe. It is recommended that industry defines more clearly the expectations for ultimate current technology, future needs and roadmaps of long-term research. This feedback would augment the human resources carrying out research on subjects that are considered as strategic by industry in the long term and avoid dispersion of efforts in less relevant subjects.

Technology and design for information processing in Beyond CMOS.

Rapporteur: R Popp, W. Rosenstiel (EDA Centrum GmbH)

Abstract

This chapter is about the design of 'Beyond CMOS' technologies, the development of which suffers today from the design-technology gap. This gap results from the different traditions of these two communities who hardly communicate. Hence, a design of 'Beyond CMOS' is, for all intent and purposes, non-existent. Starting from a description of the character of CMOS design, the current situation of 'Beyond CMOS' design, its demands and opportunities, this chapter ends with recommendations to improve the situation of 'Beyond CMOS' design: Although many aspects of CMOS design can be learnt for the 'Beyond CMOS' side, a rethinking of the design process has to take place, probably leading to a new design paradigm. As this enormous effort cannot be taken by a single academic group or single companies, a complete new and open infrastructure for design research and development has to be established, to includes experts from different fields of science and engineering coming from academia and industry.

I. Introduction

Before talking about 'Beyond CMOS', it should be mentioned that it took 50 years and several hundred billion dollars to go from a few transistors to the present CMOS complexity. Despite this effort, design is still a limiting factor in CMOS integration density. We now examine the research on new 'Beyond CMOS' technologies in order to identify a path that leads to those technologies and devices that are unlikely to happen in the CMOS world at all.

Due to the design-technology gap, today we are confronted with a situation where two communities, one coming from the technology and the other from the design side, are hardly being able to understand each other's main issues. While the "Beyond CMOS inventor" is curious how his/her findings of new devices with promising opportunities work in a design, the CMOS designer is overstrained by their uncertainties and variability and packed with enough CMOS design problems. Nevertheless, a well-established interaction between both communities is strongly needed and recommended by the NANO-TEC project, which has started to pave the way to bring together both communities.

II. The current situation in design

But what does "design" mean? In the CMOS domain every circuit being designed today follows a specific sequence. (i) It starts with a computational model at a high level of abstraction; (ii) it then goes through a sequence of synthesis and optimization transformations, (iii) this is followed by rigorous digital simulation and prototyping, and (iv) it is subjected to formal and semi-formal verification, before it is finally manufactured via advanced lithographical and chemical processes.

In order to be able to design efficiently, an automation process (Electronic Design Automation, EDA) has been established. This came out of one of the earliest inter-disciplinary collaborations: Computer scientists and engineers in EDA collaborated successfully with electrical engineers to derive various levels of circuit models, physicists and

chemists worked together to find manufacturing models, theoretical computer scientists conducted various kinds of complexity analyses, applied mathematicians and optimization experts improvised highly scalable simulation and synthesis algorithms and while application domain specialists develop intellectual property (IP) libraries. In the end, the cooperation of these research experts yielded a design process. Thus, to bring an application to a chip implementation, a system and circuit design needs:

(i) Suitable algorithms,
(ii) Their implementation in a computational model using a behavioural language
(iii) An architecture consisting of functional blocks,
(iv) The architecture should contain logic gates
(v) The architecture can be implemented by circuits
(vi) The circuits are built out of devices that are made of specific materials
(vii) The circuit implementation is guided by a certain structure following the laws of physics and chemistry.

The following illustrates the different levels on the left side:

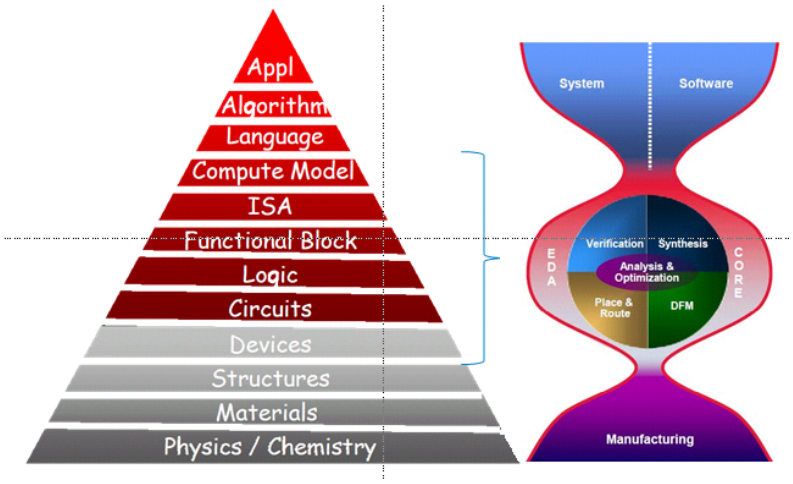


Figure 18. Abstraction Levels of the (CMOS) Design Process (left) and the appropriate tools (right)[25]

Such a standard CMOS design process of a high-performance microelectronic system, like a microprocessor, incorporates hundreds of tools and many experts to work on it. As this design process between application and device is well established in the middle stages, the difficulties are to be found at the top, between system and application, and at the bottom, between circuit and device al illustrated on the right side of figure 10.

As mentioned earlier this design process currently remains a limitation in CMOS integration density, due to the steadily growing complexity met only by the introduction of hierarchy and because of the growing number of constraints, e.g. due to energy consumption. While design runs at different levels of abstraction, certain constraints and conditions are assumed, set and some times even neglected. Due to scaling or other technological progress in CMOS, the neglected constraints could become essential some years later, but then they hardly can be

[25] R. Cavin, W. Joyner, W. Rhines, R. Rutenbar, "The Brave New Old World of Design Automation Research", National Science Foundation Workshop on Electronic Design Automation –Past, Present, and Future, June 2009, Arlington, Virginia, USA

reconsidered. A good example for this was the issue of reliability: It took many years to incorporate reliability issues into the CMOS design process. Hence, the necessary abstraction on different levels of design leads to immobility with respect to efficiency in scaling and to emerging technologies. As many physical effects and aspects have not been considered during the creation of the CMOS design process itself, a "creaky infrastructure" has been developed which is hardly able to cover today's CMOS design problems[26]. Independently of emerging technologies, a solution must be found.

III. The path between emerging nanodevices and design

To find a path between new devices, which show magnificent opportunities, and the possibility to be built into a useful system, an interaction between the communities of design and technology has to be established. Its goal has been called "systemability", defined as the ability to design and manufacture economically reliable systems based on the interaction of devices fabricated in a given technology[27].

The gap to 'systemability', which has to be bridged here, is one arising from physical effects to engineering practices[28]. There is consensus that while emerging devices have very attractive properties, the design needed to enable their use in large scale and in mass production, to compete with classic circuit design, is a "completely different story". For example, there exists ability to simulate molecular structures and charging effects for a small number of atoms but it is far away from simulating realistic systems. At present:

(i) A variety of nanodevices can be reliably fabricated using various materials, technologies and processes.
(ii) Several open questions still exist concerning the mode of operation of such devices.
(iii) Modelling and simulation can provide important answers for better understanding of these devices.
(iv) A multi-scale approach is needed in order to describe real systems.
(v) Novel circuits, architectures and design methodologies are going to be needed for a full exploitation of nanodevices.
(vi) Research and development cooperation between distributed teams is not appropriate for progress.
(vii) Education is far away from teaching a new generation of designers about nanodevices and related technology.

Concurrently, a 'Beyond CMOS' device has to meet several demands with respect to the function of a system that is built from it. Such demands can be related to *computation, storage, interconnects and I/O including analogue and digital aspects*. For every 'Beyond CMOS' contender several things have to be valid:

(i) It must add value to one or more of the four system functions mentioned above and should be compatible with the others.
(ii) All-in throughput/Watt and/or transactions/Joule must beat CMOS at time of manufacturing at equivalent or lower cost.

[26] S. Tiwari, "Devices, Technology & Applications: A Critique of New Proposals",3rd NANO-TEC workshop on SWOT analysis of emerging devices, May 2012, Lausanne, Switzerland
[27] D. Verkest, "Benchmarking CMOS Devices",2nd NANO-TEC workshop on Benchmarking of emerging devices, Oct. 2011, Athens, Greece
[28] P. Lugli, during a panel at the 3rd NANO-TEC workshop on SWOT analysis of emerging devices, May 2012, Lausanne, Switzerland

(iii) System level manufacturability, reliability and relevant tests must beat ultimate CMOS solutions.
(v) Device variability must be mitigated and modelled and cost efficient error resilient design solutions must be available.
(vi) Design methods and tools must be in place supporting design from device to system and design tool development time is 3x the technology development time.

For any 'Beyond CMOS' device and applications room temperature operation is desirable. The big challenge to the 'Beyond CMOS' devices arises from *the lack of understanding of the physics of the operation, large variance of the properties and irreproducibility*. Moreover, *interconnects and contacting nanoscale objects*, not to speak about other state variables than charge, pose a huge challenge both for design and technology.

To design for future applications using new 'Beyond CMOS' technologies several points have to be addressed:

(i) The need for models and abstractions at all levels of the design process as a key issue
(ii) The need for compatibility to existing industry design standards of high-level behavioural languages if the technology should be connected with CMOS.
(iii) The need for powerful new, physically aware, system-level design science and methodologies at the top of the design process to increase the productivity of designers, otherwise efficient use cannot be made of advanced devices and materials.
(iv) The need for robust optimization methodologies in the middle of the design process, to provide guaranteed performance of integrated systems composed of devices, the characteristics of which are highly variable, operate in several different physical domains and have uncertain reliability.
(v) The need for a revamped, systematic, and greatly improved interface to manufacturing (Design for Manufacturing) at the back end, as well as throughout the flow, to support the design of high-yield systems that obtain maximum utilization of a technology and to assure that products can be produced using new technologies.
(vi) The need for design tools for the 'Beyond CMOS' devices, which have multi-physics and multi-scale characters. Without proper tools the true exploitation of the emerging devices in ICT will become extremely difficult or even impossible.

IV. Design in Beyond CMOS

At present, some structures and devices, which are definitely different from CMOS, can be designed in a certain way[29] but a real design as a construction of an architecture of them is currently hardly possible.

[29] There exist some approaches to do some design on 'Beyond CMOS' devices as follows:
[a] Research directions in beyond CMOS computing, George I. Bourianoff, Paolo A. Gargini, Dmitri E. Nikonov, Elsevier, Solid-State Electronics 51 (2007) 1426-1431
[b] TAMTAMS: A flexible and open tool for UDSM process-to-system design space exploration, M Vacca, M Graziano, D Demarchi and G Piccinini; ULIS 2012, Proc 13th Int Conf on Ultimate Integration on Silicon, pp 141-144. D.O.I. 10.1109/ULIS.2012.6193377
[c] Design and simulation of 2-D 2-dot quantum-dot cellular automata logic, LR Hook, SC Lee - Nanotechnology, IEEE Transactions on, 2011
[d] TCAD: present state and future challenges, T Ma, V Moroz, R Borges, L Smith - Electron Devices Meeting, 2010
[e] Variable temperature Raman microscopy as a nanometrology tool for graphene layers and graphene-based devices, I. Calizo, F. Miao, W. Bao, and C. N. Lau, A. A. Balandina, APPLIED PHYSICS LETTERS 91, 071913 (2007)
[f] Beyond CMOS Nanodevices for Adding Functionalities to CMOS, http://www.nanofunction.eu

Although there are common aspects in different applications, the design challenges mostly depend on the given application. As each application has its own specific requirements, it is clear, that this leads to different design optimization criteria. While there are criteria like real-time, energy efficiency, productivity, reliability and robustness, safety and security are also mandatory, and all these are of different importance for different applications. Especially the energy challenge and the application challenge due to the changing society could trigger investment in new tools that could break the heavy legacy of present design tools.

Approaching the end of the CMOS roadmap the need for a new technology will trigger the development for appropriate new tools and methods. Hence, a design methodology and tools for a specific technology may become a reality. Therefore, design tools will definitely be the discriminating factor for the success of one specific technology, because of the difficulties mentioned before which have to be overcome by design tools. This is because the design tool is the codification of a design process and it is its mathematical translation which itself makes the difference.

In this context, universities, ideally supported by public authorities, should take the initiative to work on design for 'Beyond CMOS' technologies while their educational mission will train a new kind of young scientists and engineers.

Moreover, the current situation in CMOS design, which continuously approaches and overcomes new barriers with respect to physics or manufacturing, could be a good starting point on how to deal with 'Beyond CMOS' technologies [30]. To this extent it could be good to start with design for 'Beyond CMOS' by extending the current procedure in order to gain more insight. Therefore,

(i) the design of the system (top-to-bottom) and of the device (bottom-to-top) must meet half-way before attempting a "brute-force" design,
(ii) compact models must connect multi-physics to transient electrical properties and
(iii) interconnects, e.g. transport, parasitics issues, have to be included in the design flow.

Furthermore, to develop the ability to design 'Beyond CMOS' devices, scientists and engineers need to rethink the design process and technology, including the way things are approached. In this manner, for example, a contact could not be a contact the way it is understood in CMOS and therefore there is a strong need for new ideas that lead to new design tools and methods. Especially in 'Beyond CMOS', design starts from the physics and the chemistry and the nanostructures need to be modelled to understand how they work. In order to create architectures based on those nanostructures and devices, the need for modelling becomes increasingly essential. All these makes up a highly creative process, which cannot be done by one person or even a single team and therefore it requires extended R&D cooperation.

It is quite obvious that it will be very difficult to replace a chip with 100 million CMOS transistor devices by using the currently discussed Beyond CMOS technologies. The investigation of a sensible use of Beyond CMOS technologies is therefore an essential research task. One important question in this respect is "the level" at which such a replacement is going to happen (see figure 18).

[30] P. Lugli, "Design Tools for Beyond CMOS technologies",4th NANO-TEC workshop, Nov. 2012, Barcelona, Spain

In our view it might not be advantageous to replace the current CMOS technology at device level, i.e., replace a CMOS transistor by the corresponding Beyond CMOS device, and leave the rest of the design pyramid unchanged. The current implementations in Beyond CMOS technologies show that it is very hard to implement a realistic functionality by Beyond CMOS devices. Currently, only very limited functionality with tens or conceivably hundreds but not millions of Beyond CMOS devices can be implemented.

We therefore have to analyse carefully if a higher level, like the functional block level or the compute model level, or even the algorithm level, might be a better correspondence for such a replacement. As the investment in existing software is huge, it is difficult to believe that Beyond CMOS technologies will reach higher levels than the computer architecture. But a transition of technology at another abstraction level than the device one has to be taken into account. The corresponding computing architecture might need to be redesigned with respect to Beyond CMOS technology[31]. This can be illustrated by an example:

There are at least two reasons why the "von Neumann" architecture, with all its disadvantages, survives for more than 50 years. One of these reasons is that many inventions like pipelining, caches, out of order executions, compiler optimizations, multi core or multi threading have brought great progress in these last fifty years. The other reason is that the current CMOS technology fits very well this architecture. The best example is the current, although not really "natural", separation of computation and storage of information: CMOS technology optimizes computation (fast, small and expensive) and storage (large and cheap) individually resulting in a maximum of performance as we see it today. Many alternatives have been proposed in the last 50 years, none of them succeeded mainly because of the technological CMOS evolution. Beyond CMOS technologies might throw a different light on the question of which computer architecture will be an optimum for a given Beyond CMOS technology and which "transition" with respect to the abstraction level will be best for that new technology[32].

A hint on this could be taken from neuromorphic computing which could lead to a new computing paradigm[33], because it offers a very powerful way to process information following a kind of natural intelligence, which is much faster, than the ordinary CMOS approach based on the "von Neumann" architecture.

Furthermore computing models and architecture could be successful, if they would take the possibility of occurring errors into account. An approach that is able to "live" with errors could take advantage of errors to get robustness in the presence of uncertainty from all the different sources. This would lead to more powerful computing, than the deterministic approach of CMOS[34].

The tremendous task of rebuilding the design process and to push design tools for new technologies cannot be done even by the three large EDA companies that dominate the EDA-Industry, a small 4 billion $ market, with no real new investments in new areas. Furthermore, design companies or system and chip manufacturers will not do design for the new technologies on their own because they have to bring products to the market. Therefore, the

[31] W. Rosenstiel, "Design Tools for Beyond CMOS technologies",4th NANO-TEC workshop, Nov. 2012, Barcelona, Spain
[32] W. Rosenstiel, "Design Tools for Beyond CMOS technologies",4th NANO-TEC workshop, Nov. 2012, Barcelona, Spain
[33] S. Thorpe, "Neuromorphic computing as a new computing paradigm",4th NANO-TEC workshop, Nov. 2012, Barcelona, Spain
[34] S. Tiwari, "Design Tools for Beyond CMOS technologies",4th NANO-TEC workshop, Nov. 2012, Barcelona, Spain

only way around this is to bring all kinds of people together in order to make decisions how the things shall be done and then people would work on it. Probably this development will be led only by new companies, which will come with a new technology together with its design tools.

In the end, the objective of design now and in the future is efficiency: Non-specialists, with sufficient training, should be able to design reliable and robust systems first-time right without knowing details of the technology. In particular, in analogue design for example, we are far off such a situation. Additionally, design approaches should also balance efficiencies and effectiveness and be open to new scientific breakthroughs.

In this context the easiness of the use of the designing tools is important as well as the understanding of the underlying physics. The phenomena arising from the decreasing dimensions need more complex physical models, moving from continuum models to quantum mechanics to ab-initio models, but combining these with design tools is not straightforward. Therefore, a new, simple and open infrastructure for design is needed[35], which connects people and things. To build such a structure will be an international-scale problem that crosses frontiers of many disciplines, like solid state physics, biotechnology, chemistry, mathematics and the applied sciences. This needs a cooperative effort, probably world-wide, and in particular in Europe, with much thinking at its start and long project duration under a unified leadership.

Key to this and in fact to the development of design is the connection of the technology and the design community. Of course this will happen at some point in time because of the need for a specific application, which will involve the design community automatically. But to keep the initiative and to enforce a certain development, both communities have to strive actively to be connected and to engage in regular exchanges. The NANO-TEC project initiated first professional contacts and discussions but this work must continue. Specifically, simulation and modelling of emerging devices has to be implemented in order to encourage designers to do their exercises in examining emerging devices with respect to builders of circuits and architectures.

V. Conclusions and Recommendations

Basically, two overall conclusions can be drawn. Both, the need to *rethink design processes* and the need of a *new open infrastructure* for the development of 'Beyond CMOS' design clearly emerge.

Recommendation 1
As a first step to meet these needs, motivation and support to facilitate communication and cooperation between design and technology actors from academia and industry are crucial. Mechanisms should be put in place in the form of text-book example style projects addressing the methodology to meet a technology-design challenge in Beyond CMOS, selecting one or two technologies and specific applications.

Recommendation 2
It is recommended that a simple and open infrastructure for design is set up connecting people and things. Such infrastructure could have an international character beyond EU borders,

[35] P. Lugli, during a panel at the 3rd NANO-TEC workshop on SWOT analysis of emerging devices, May 2012, Lausanne, Switzerland

addressing problem cutting across frontiers of many disciplines, like solid state physics, biotechnology, chemistry, mathematics and the applied sciences. This cooperative effort, with much thinking at its start and long-term vision should run under a unified leadership. From the resulting exchanges of knowledge, the "systemability" of 'Beyond CMOS' devices has to be proven. For this to happen, modelling and simulation of 'Beyond CMOS' devices and circuits have to be developed to gain sustainable knowledge.

Recommendation 3

Education strategies must be devised in order to enrich the training of young scientists and engineers in 'Beyond CMOS' technologies and the associated but to be determined, design needs.

Summary of Recommendations

The recommendations arrived at in a process which combined presentations, consultation, analysis, discussions and documentation, as part of the Coordination Action NANO-TEC activities, are embedded in the quest for continued economic competitiveness of Europe in the strategic field of information and communication technologies which, if successfully oriented, translates into economic growth and the creation of high-tech jobs. While the main industrial actors concentrate in a R&D horizon with products emerging within five years, the views presented and summarised here have a longer time line.

A sustainable and continued generation of knowledge is a condition sine qua non for future economic success. The NANO-TEC consortium does not claim to have a crystal ball, instead it has attempted to involve as large a section of the Beyond CMOS researchers in Europe to find out what Europe is best at, what roadblocks we face and what is seen as essential for future research.

The NANO-TEC consortium was fortunate to count with the support of the European Commission and the active participation in various capacities from leading experts from academia and industry coming from the USA, Japan and, mainly, Europe.

The recommendations from the preceding sections in this report are summarised below.

Recommendations concerning R&D in *state variables*:

- Concerning *all state variables*, be these charge-based or not, it is recommended that research towards a better theoretical understanding of the underlying physics and material science of nano-scale devices is supported towards potential breakthroughs. In particular, the large variance in physical and electronic properties of the concepts and technologies discussed, requires that in addition to a higher level of knowledge, the design and emerging devices communities must work together to assess and exploit the full potential of this device- and system-relevant research area.
- Furthermore, *for most state variables*, the interconnect challenge at the nano scale, i.e., connecting to and from nano-devices, is a common one to be overcome theoretically, experimentally and technologically as it affects not only performance, interconnects and architectures but also, and perhaps more importantly, reliability and temperature stability.
- Considering *charge-based state variables*, and in particular *nanowires*, it is recommended that a combination of nanowires technology with III-V compounds and or alternative architecture be explored with view to integrate III-V compound nanowire devices on a Si platform. In the area of *graphene*, emphasis should be placed on the suitability of fabrication and integration constraints in a combined Si-graphene new ICT technology, going beyond sensors and single components. Along the lines of two-dimensional systems, *layered materials* could be explored as alternatives as they exhibit an energy gap. In the light of recent progress, *topological insulators* should be considered earlier rather than later in a targeted research effort. The field of *molecular electronics* would benefit from strong collaborations between physicists and chemists on the one hand, with the technology and design communities on the other. Concerning *memristive devices*, local heating, which impacts power consumption, needs to be addressed, as well as co-firing, fan-out and scalability bounds. Since

highly non-linear processes are involved, work towards an adequate theoretical framework is mandatory.

- Concerning *non-charge-based state variables*, and starting with spin, it is recommended to support research in spin logic as this constitutes a field, potentially able to deliver low power devices towards non-dissipative information processing. Any future program on *NEMS* should include a strong element on understanding contact physics, friction and wear at the nano-scale, all three factors being essential for the development of active power management and logic applications; further miniaturisation of NEMS through technology development and especially improved design and simulation tools to include several aspects of physics.

Recommendations concerning R&D in *new computation paradigms*:

- New computing paradigms are required for information processing including, for example, *neuromorphic computing*, *quantum computing*, chemical and molecular computing, quantum computing by molecular spin clusters and bio-inspired computing, among others. A practical recommendation in this field is to support research in a "super integrated project" or similar in which solid-state quantum computing and neuromorphic computing could become embedded in digital environments via digital-analogue hardware and software interfaces. The target would be to create useful hybrid systems to, e.g., interact with human users and be capable of adaptive learning. The research could be on fields in which unconventional computing could solve or give a more efficient answer in terms of energy and time. Such a "super IP" should pave the way for important commercial applications in 5 to10 years.
- It is recommended to continue the exploration of *novel computation approaches in general*. In particular, a *comparative and dynamic analysis of the interaction between design and the emerging computation technologies* as an integral part of the R&D efforts would provide Europe with a valuable and probably decisive advantage.

Recommendations on the *Design-Technology interaction*

- This interaction is a challenging one. The consortium finds that strong motivation and support are needed in order to facilitate *communication and cooperation between design and technology actors* from academia and industry. These communities have very different cultures and during the project progress has been made to establish communication and find some common terminology. Bearing this in mind, the consortium recommends that a couple of pilot projects are launched addressing explicitly not only the technical aspects but, above all, methodological aspects of this interactions with one or two well defined examples of novel state variables and a specific application each. The methodology lessons of such projects would be a starting point on the practicalities of meeting the technology-design challenge in Beyond CMOS research.
- A second recommendation is the setting up of a *simple and open infrastructure* for design connecting people and things. Such infrastructure could have an international character beyond EU borders to allow free exchange of knowledge, where the "systemability" of 'Beyond CMOS' devices is a formidable challenge. Furthermore, modelling and simulation of 'Beyond CMOS' devices and circuits have to be developed to gain sustainable knowledge to feed in the design processes.

Recommendation concerning the *involvement of industry*

- At present the willingness of non-European industry to enter in discussions on Beyond CMOS research has a higher profile than that of European ones. It is recommended that industry and researchers in beyond CMOS intensify their interactions to define more clearly the expectations for future Beyond CMOS technologies, future needs and roadmaps of long-term research. An example of this would be a reactivation of the Scientific Community Council towards an exchange of views to strengthen the overall European nanoelectronics research, to include technology readiness levels closer to the proof of concept one.

Recommendations concerning *research infrastructures and education*

- The consortium recommends that measures are implemented to foster the *coordination of all technological facilities* having a significant activity in Beyond CMOS research, in a European network with a single entry point in each country. Crucial to the proposed modus operandi is common access rules and harmonisation of the organisational procedure. The rationale is to take advantage of the complementarity of the 'Beyond CMOS' research infrastructures and to capitalize on the fields of highest expertise in each country or region.
- Trends in the decreasing number of students in the physical and engineering disciplines did not go unnoticed. The consortium recommends that multidisciplinary *'Beyond CMOS ' Erasmus Mundus programme* be set up to educate a new generation of student in future information processing concepts, including theory of information, binary and non-binary information processing, as well as training the young scientists and engineers in 'Beyond CMOS' technologies and design.

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Trends in Nanoelectronics		
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