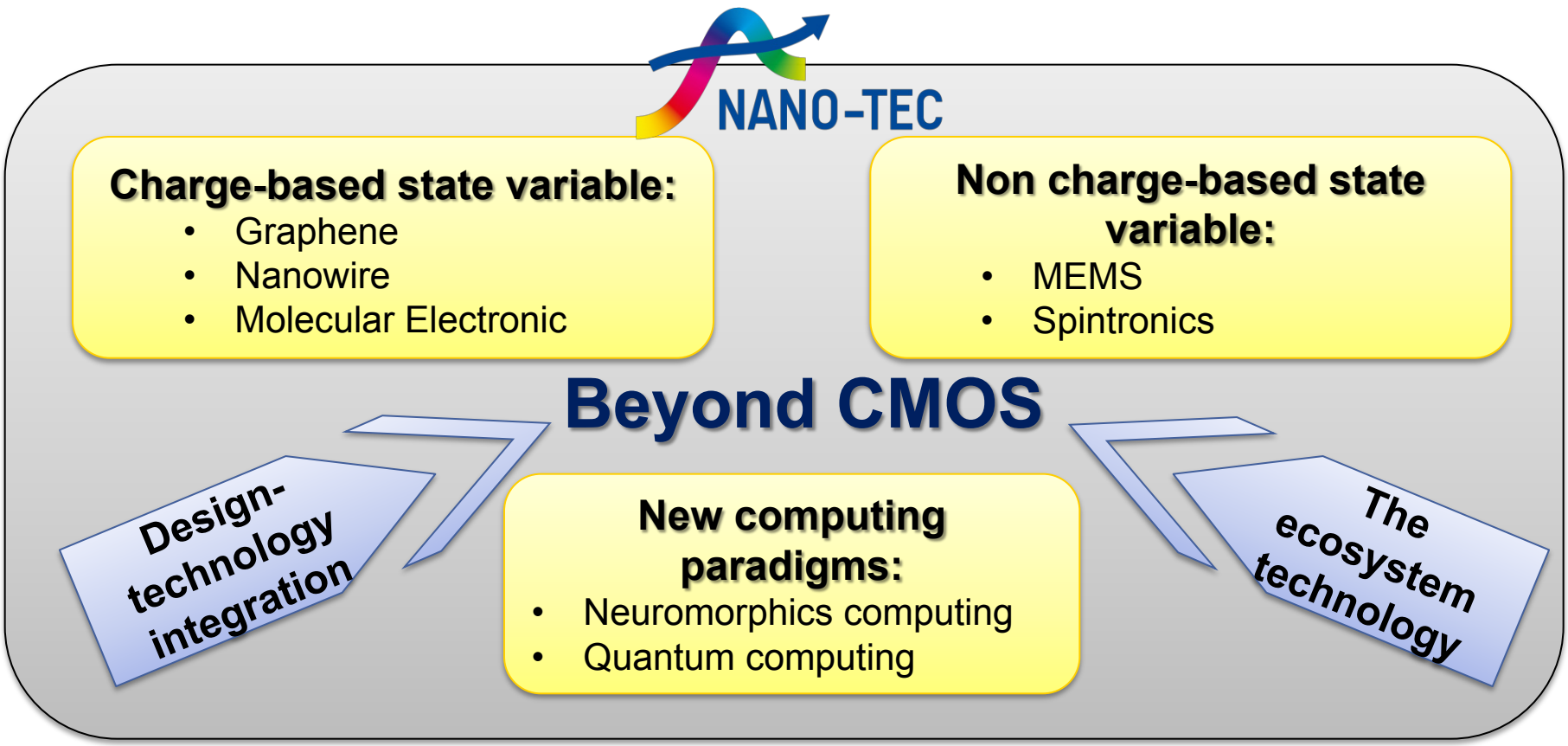
4th Workshop: Elaboration of Recommendations

Charge-based State Variable

Rapporteurs:
Mart Graef (TUDelft) and Guilhem Larrieu (CNRS-LAAS)

INPUTS FROM:


NANO-TEC
Charge-based state variable:
• Graphene
• Nanowire
• Molecular Electronic
Non charge-based state variable:
• MEMS
• Spintronics
Beyond CMOS
Design-technology integration
New computing paradigms:
• Neuromorphics computing
• Quantum computing
The ecosystem technology

INPUTS FROM:

Based on workshop presentations, discussions, working group and rapporteur reports

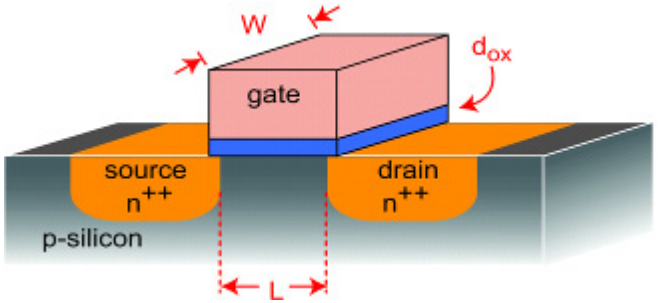
- **Topic:** Nanowires
  - **WS2 Speaker** Dr. Heike Riel, *IBM Research Zurich*
  - **WS3 Speaker** Dr. Heike Riel, *IBM Research Zurich*

- **Topic:** Graphene
  - **WS1 Speaker** Dr. Jeong-Sun Moon, HRL Laboratories LLC
  - **WS2 Speaker** Dr. Jari Kinaret, *Chalmers Univ Tech*
  - **WS3 Speaker** Dr. Max Lemme, KTH

- **Topic:** Molecular electronics
  - **WS1 Speaker** Prof. Göran Wendin, Chalmers University of Technology
  - **WS2 Speaker** Dr. Dominique Villaume IEMN
  - **WS3 Speaker** Prof. Dr. Sense Jan van der Molen, Leiden University

Scaling limitations of the MOSFET

Finite # of dopants
→ device variability



d_{ox} is reduced
→ Increasing gate leakage

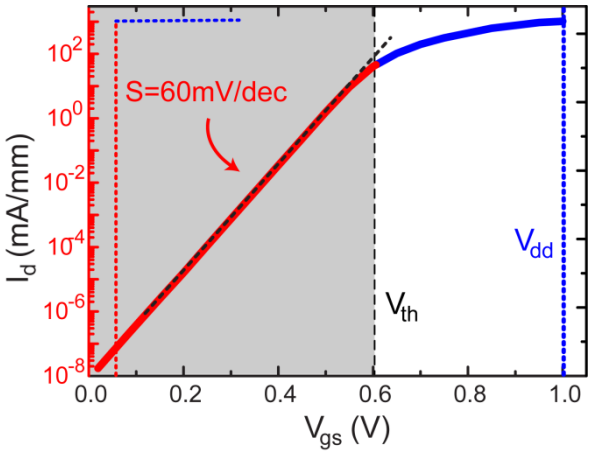
L is reduced → fraction of Q controlled by gate decreases

V_T shift, DIBL, and increased inverse subthreshold slope

► Minimum inverse sub-threshold slope ***S*** limited by thermally broadened Source Fermi function:

$$S_{\min} = \frac{k_B T}{q} \ln(10) = 60\text{mV/dec} \quad @\ \text{RT}$$

► Limit for *any* transistor/switch technology based on thermal emission

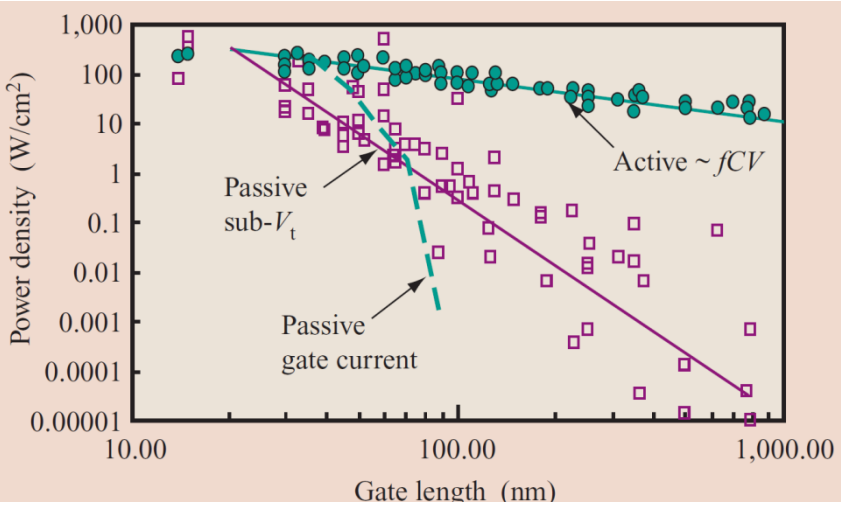


From H. Riel - Workshop Nano-Tec October 13-14, 2011 Athens

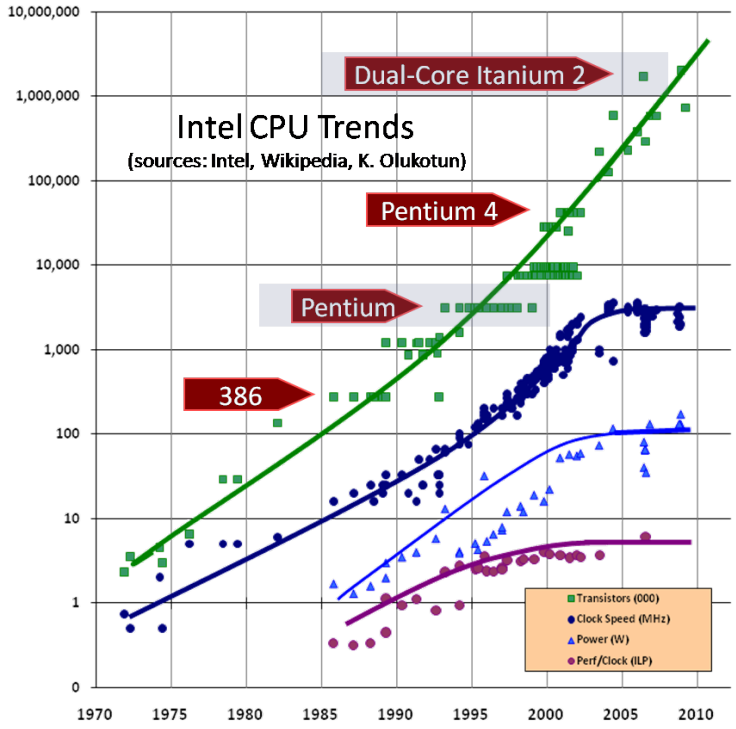
Power Challenge

Power per chip continues to increase.

- Leakage power dominates in advanced technology nodes.
- Voltage scaling slowed: 90nm = 1.2V, 45nm = 1V, 22nm = 0.8V
- Huge thermal dissipation (CPU generate 100W/cm^2)



W. Haensch et al., IBM Journal of Research and Dev.,50 p. 339, 2006



From H. Riel - Workshop Nano-Tec October 13-14, 2011 Athens

INTRODUCTION

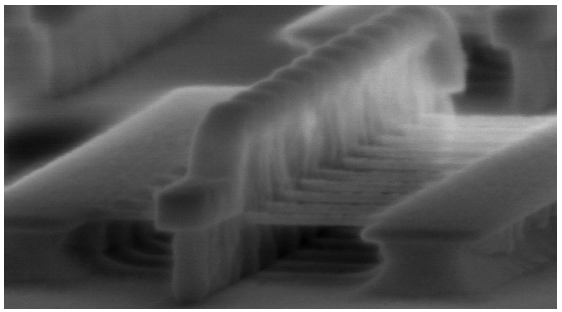
Charge-based state variable for beyond CMOS need:

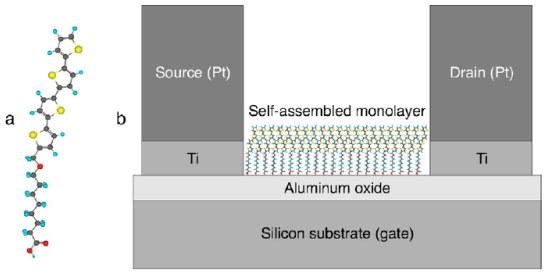
- Low operation voltage/ low off current (power challenge)
- CMOS/Si platform compatible

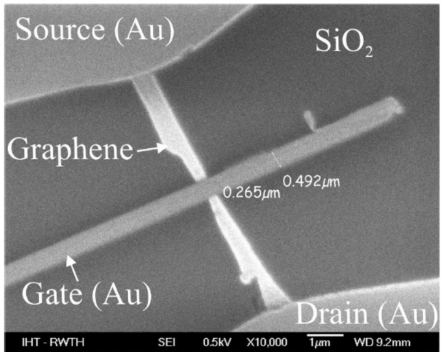
NEW channel architecture/material concept:

- Architecture : ultra thin layer (graphene , mol elec), 1D (nanowire)
- Material: graphene, molecule, compound semiconductor.

But CMOS-compatible technology

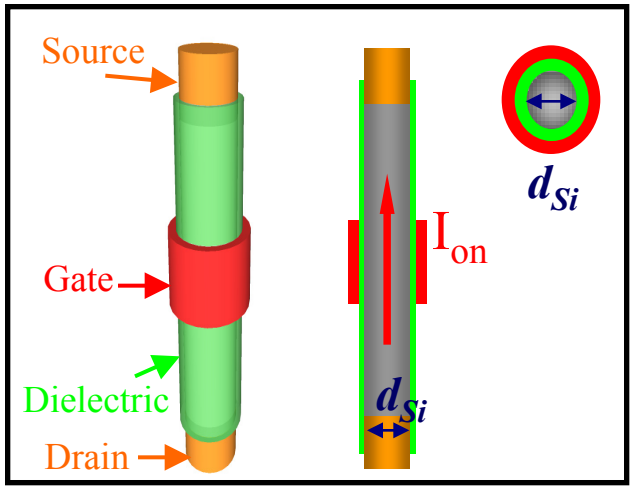






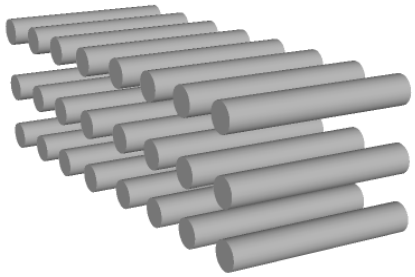
NW-based transistors with Gate All Around (GAA)

- **Excellent electrostatic control of the gate over the channel**

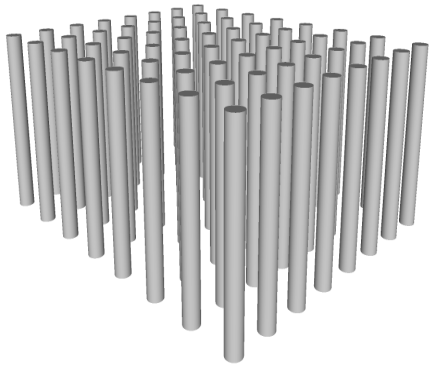


- Transistor implemented on single NW with narrow diameter (d_{Si}) :
  Drive current: **I_{on} very low**
- On state current increase, Ion
  Need to address **multi** NWs

Horizontal or vertical integration



Horizontal structure

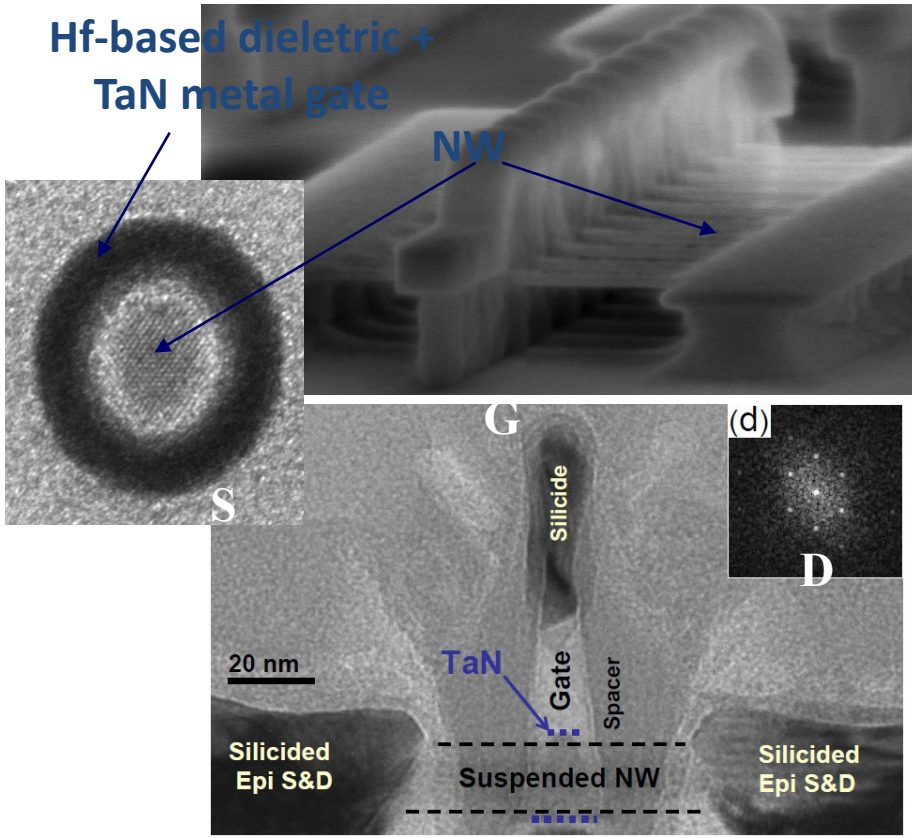


Vertical structure

- Fabrication - **Conformality** issues on high aspect ratio nanowires
- Limited volume of silicon >> large **access resistance** (fabrication strategy dependent, vertical vs. horizontal)
- Larger inner and outer **fringing capacitances** (limits f_T)

Top-down NWs – planar integ.

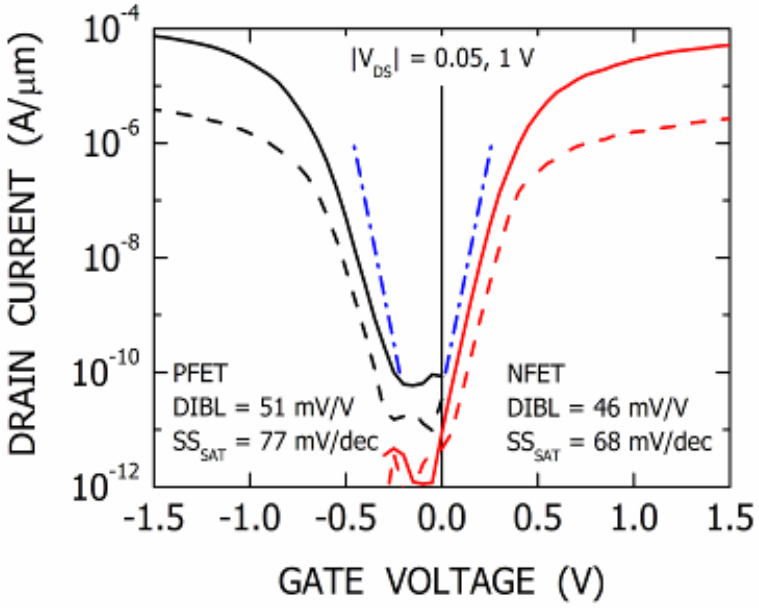
Multiple planar NW channels

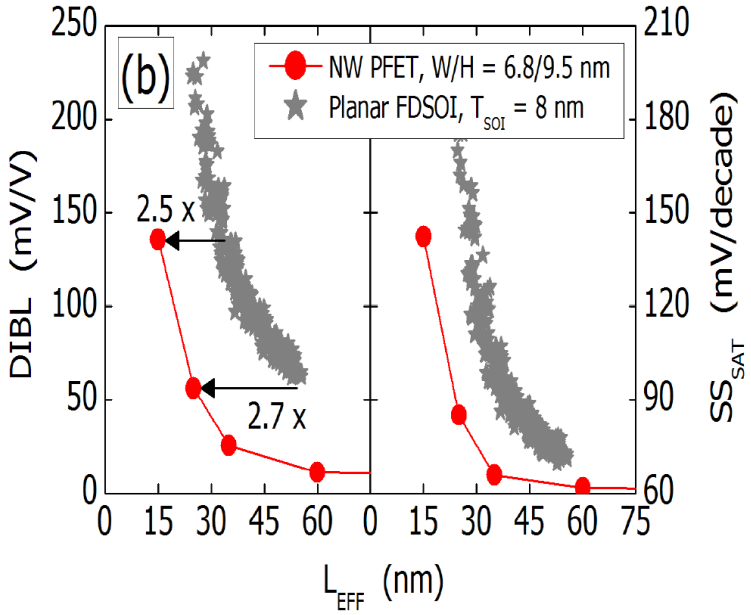


- Pattern density (nanowire (fin) pitch)
- Strain relaxation in strained substrates after nanowire patterning

S. Bangsaruntip et al., IEDM Tech. Dig., 297 (2009) (IBM)

Top-down NWs – planar integ.





S. Bangsaruntip et al., IEDM Tech. Dig., 297 (2009) (IBM)

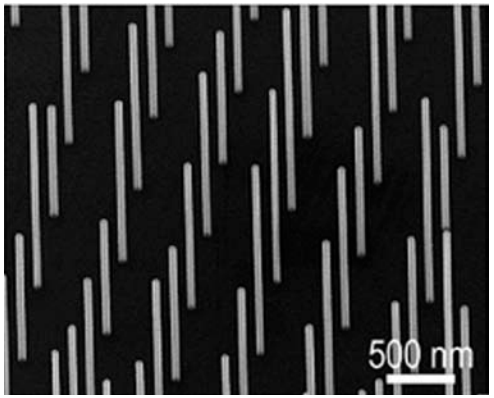
Significantly improved scaling behavior compared to planar fully depleted devices

- GAA geometry ~ 2.5 x LEFF benefit at constant short-channel effects
- ***GAA FET – the ultimately scaled device!***

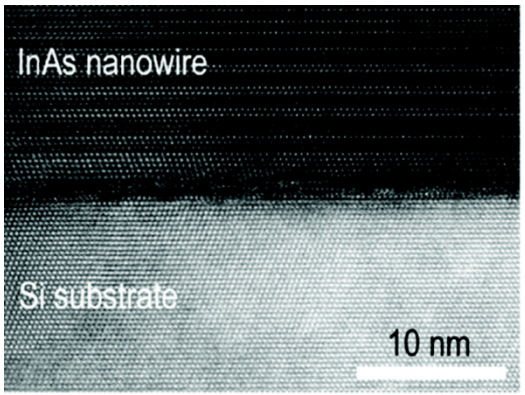
Bottom-up NWs – vertical integ.

Growth of III-V Materials on Si Platform:

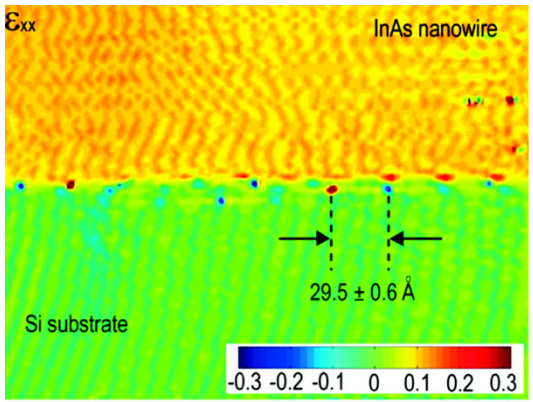
- Small NW cross section enables epitaxial growth of lattice mismatched systems
- Allows direct integration of III-V materials on Si
- III-V heterostructures can be grown
- "Catalyst-free / self-catalyzed" position-controlled growth is possible



catalyst-free InAs growth on Si



Sharp InAs-Si interface

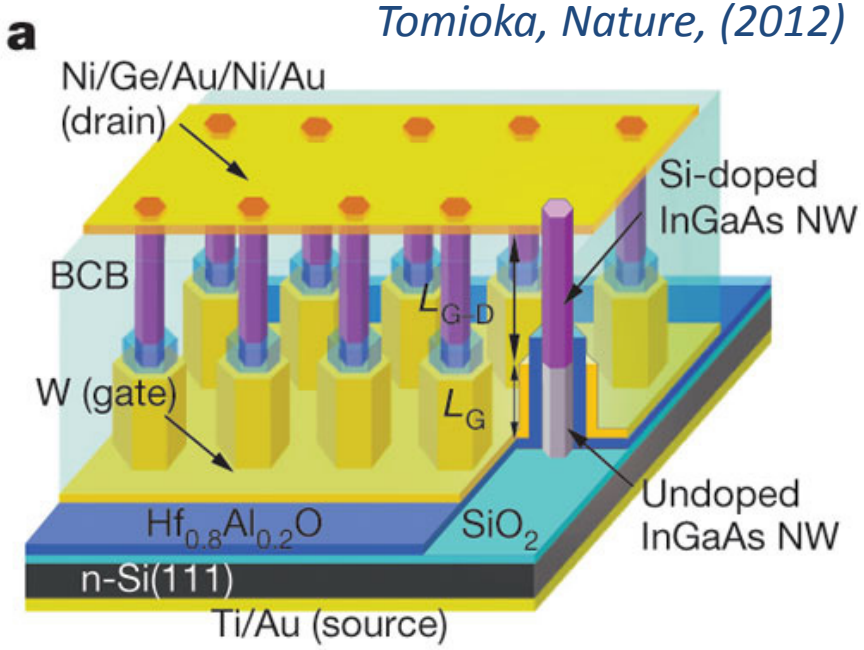


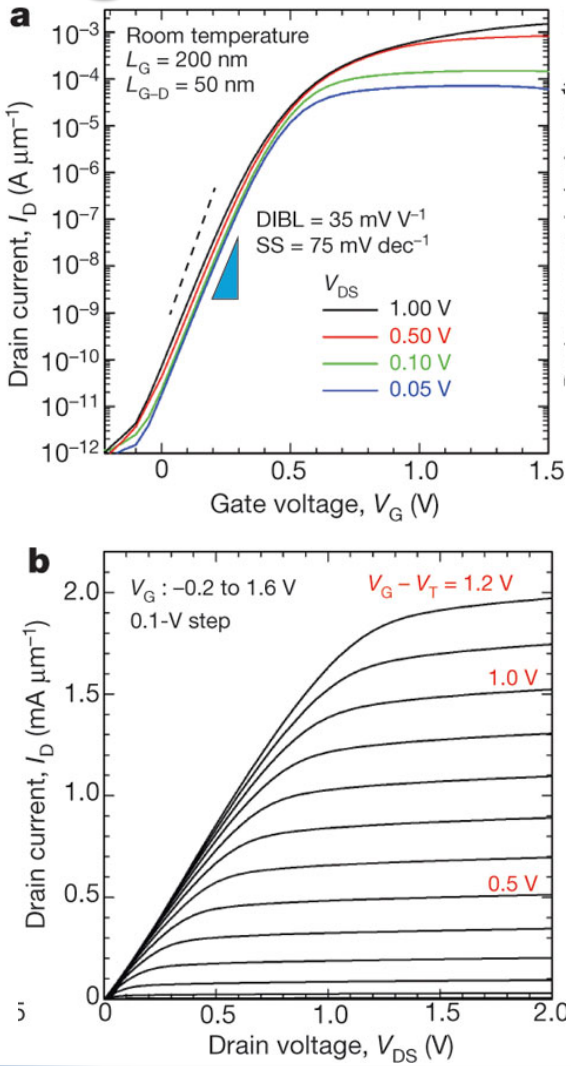
Tamioka, Nano Lett., 2008

- Minimum nanowire diameter not competitive with top-down approach
- Nanowire density might not be competitive with top-down (insulation, contacts, BEOL...)
- How to make it compatible with the top-down approach within the same process flow?

Bottom-up NWs – vertical integ.

Tomioka, Nature, (2012)





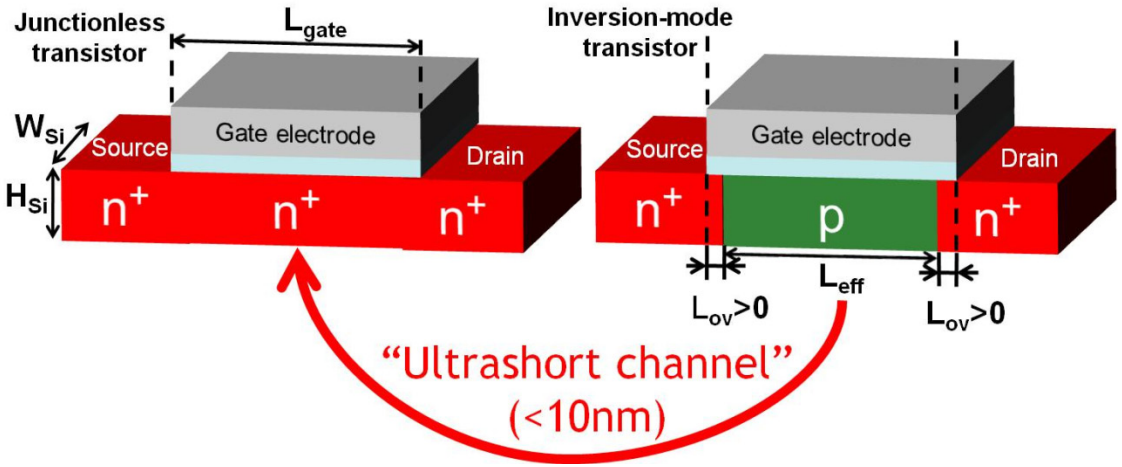
High-electron-mobility transistor structure (InGaAs)

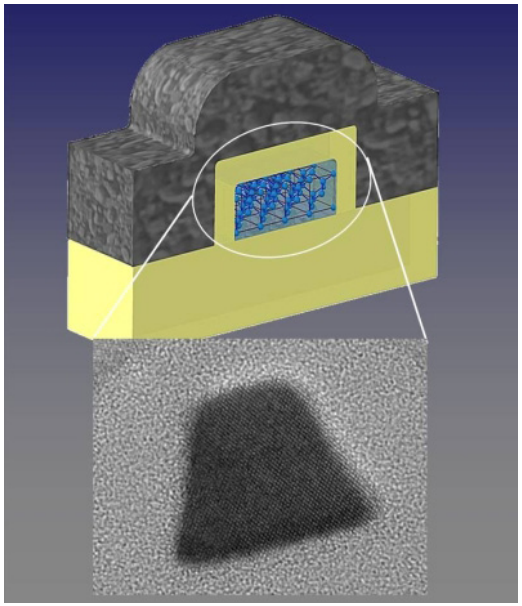
- greatly enhance the on-state current and G_m
- keeping good gate controllability

NANO-TEC

SEVENTH FRAMEWORK PROGRAMME

Junctionless nanowire transistors





JLT: no junctions and no doping concentration gradients
(made of a semiconductor layer that is thin and narrow enough to allow for full depletion of carriers when the device is turned off.)

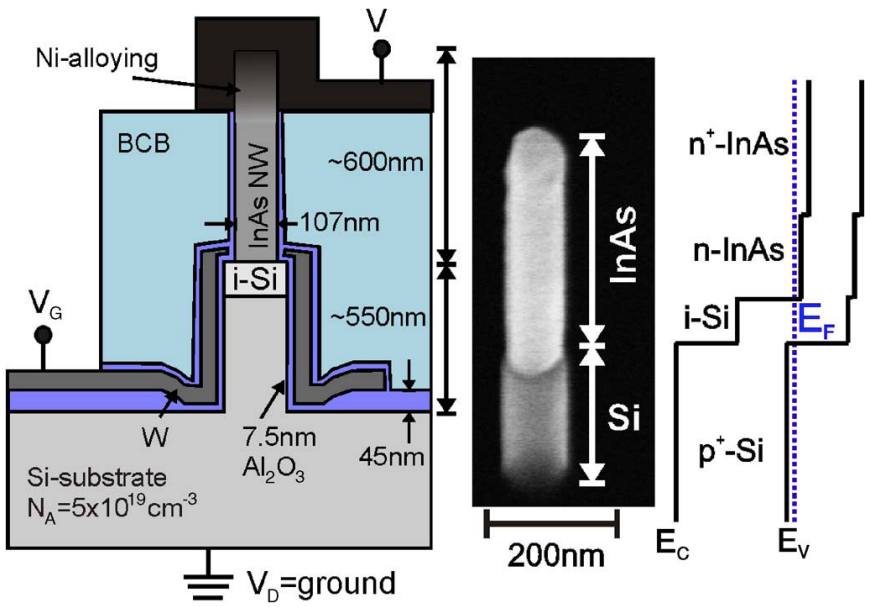
- Low I_{off}
- Bulk conduction i.e. less sensitive to surface roughness.

Tunnel nanowire FETs

Steep sub-threshold slope switch

- Tunnel FET is the most promising small swing switch for V_{dd} scaling
  → S < 60mV/dec possible (principle of operation)
- Disadvantage: I_{on} depends on tunneling probability

InAs–Si NW heterojunction TFETs,



Moselund, EDL 2012. (IBM)

Graphene based transistors

Graphene:

- is a mono -layer material with very good mobility (up to 200 000 cm^2/Vs at room temperature in vacuum), high saturation velocity (4×10^5 m/s).
  - At device level, it is observed that the mobility is dependent on host substrate as well as on the gate oxide used (charged impurity scattering largely degrade the mobility),

- Production quality material : CVD appears as the most promising technique because it is scalable, transferable, is rapidly developing
  - the presence of defects in CVD graphene sheet lead to relatively low mobility values (10^3 cm^2/Vs)

- Electrical contacts: Contacting graphene device is more difficult than Si device, where one order of magnitude accuracy better than silicon is needed
  - graphene-metal ohmic contacts with contact resistance below 100 Ω µm (Moon et al. Appl. Phys. Lett. 100, 203512 (2012))

Graphene based transistors

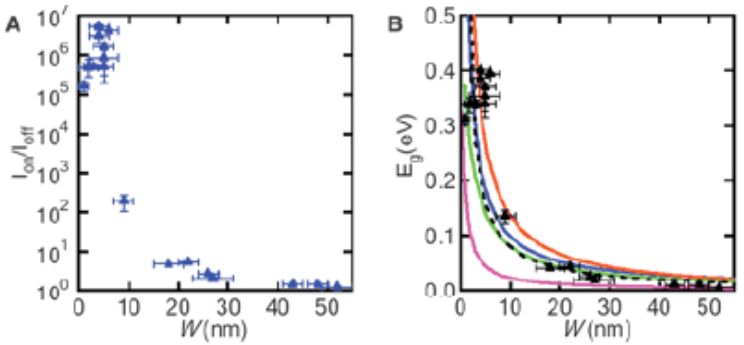
Challenge: absence of a band gap makes it hard to turn the devices off

1- Old thinking: create a gap

– Graphene nanoribbons (GNR)

Eg ≈ 0.8 eV nm/W

- Lithographically: hard, need width 2-5 nm, good edges
- Chemical synthesis: on metals, hard to position, no transport measurements exist yet
- Unzipping of CNTs or synthesis inside a CNT

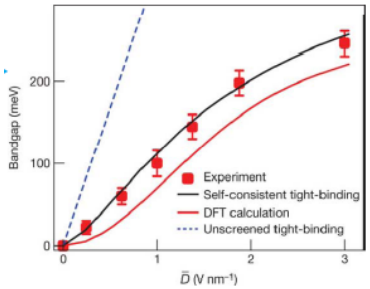


X.Li *et al.*, Science **319**, 1229 (2008)

– Implement strain in large-area graphene (global uniaxial strain exceeding 20%)

– Bilayer graphene with electric field:
gap 100-200 meV, required V_{bg} ~100 V

– Chemical modification (e.g., nitrophenyl), gap 0.4 eV
(S. Niyogi et al., Nano Lett. 10, 4061 (2010))



Y. Zhang *et al.*, Nature **459**, 820 (2009)

From J. Kinaret - Workshop Nano-Tec October 13-14, 2011 Athens

Graphene based transistors

Challenge: absence of a band gap makes it hard to turn the devices off

1- Old thinking: create a gap

2- New thinking: under research

- BiSFET, tunnel FET … : predicted to have very low switching energies, but they have not been demonstrated experimentally

- Graphene base transistor (BGT) in vertical structure (W. Mehr et al, IEEE EDL, 33(5), 2012)

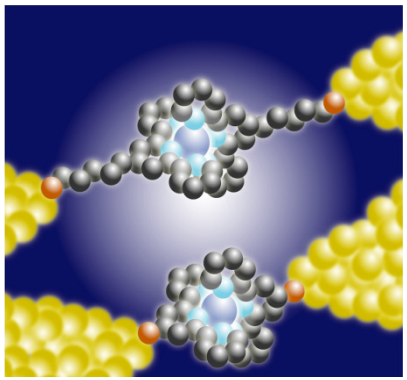
More than Moore area should have a higher potential than logic graphene transistors

(i) Optoelectronics, where optical applications range from ITO replacement (absorption 2.3% per layer), through solar cells to lasers.
(ii) NEMS, low mass and large Young's modulus are promising characteristics for high frequency NEMS
(iii) Spintronics, using large spin coherence lengths, pure spin currents and large resistance signal for spin-dependent transport in spin-based logic devices.

Molecular electronics

Molecular device offer **natural nanometer scale**, **programmable functionalities** activated by light, E-field and temperature, and should be a **low-cost technology**.

Single molecule electronics

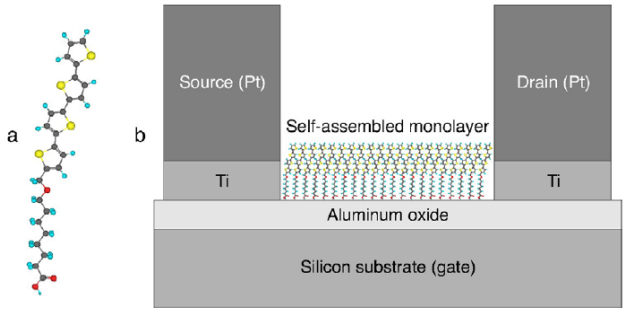


L < a few nm
t < a few nm

Basic science
knowledge development

No foreseen applications
In a reasonable time-scale

Self-assembled molecular electronics

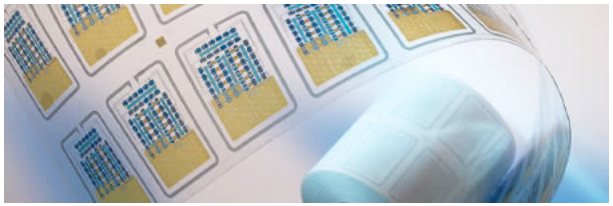


L < tens nm- µm
t < a few nm

Basic science
knowledge development

possible application foreseen

Thin-film molecular electronics



L > µm
t > few 10 nm

Plastique electronics (OLED, OFET …)

Some products already commercialized

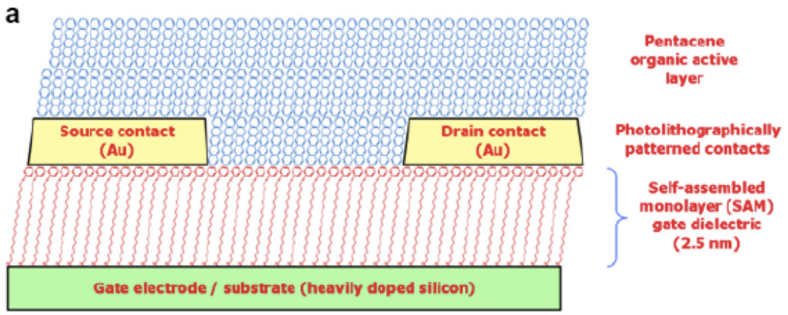
From D. Villaume - Workshop Nano-Tec October 13-14, 2011 Athens

Molecular electronics

Self-Assembled Monolayers (SAM) electronics for switch.

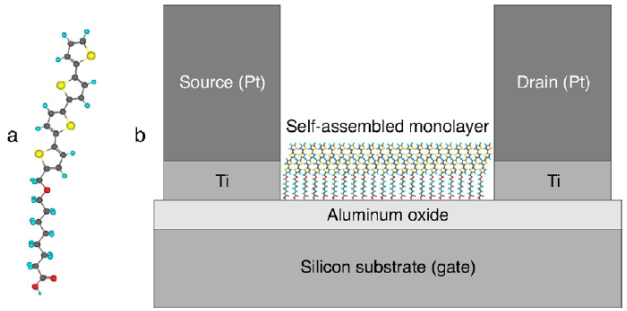
- Self-assembled molecular electronics was further divided into device families in which the self-assembled monolayers (SAM) act (i) as dielectric, (ii) as an active channel or (iii) as a non-linear switch.

SAMs is to use them as gate dielectrics combined with organic conducting polymers



$\mu=0.6 cm^2V^{-1}s^{-1}$
1.5 to 3V
<1nW/logic gate

SAMs as an active channel



$\mu=3.5\ 10^{-3} cm^2V^{-1}s^{-1}$
I_{on}/I_{off} ~ 1800 (V_D=---0.5V)
Mooaghi et al., adv.Func.Mater.(2007)

Molecular memories and switches.

- Principle 1: charge storage on a redox molecule
- Principle 2: change of molecular conformation, conductance switching.

Molecular electronics

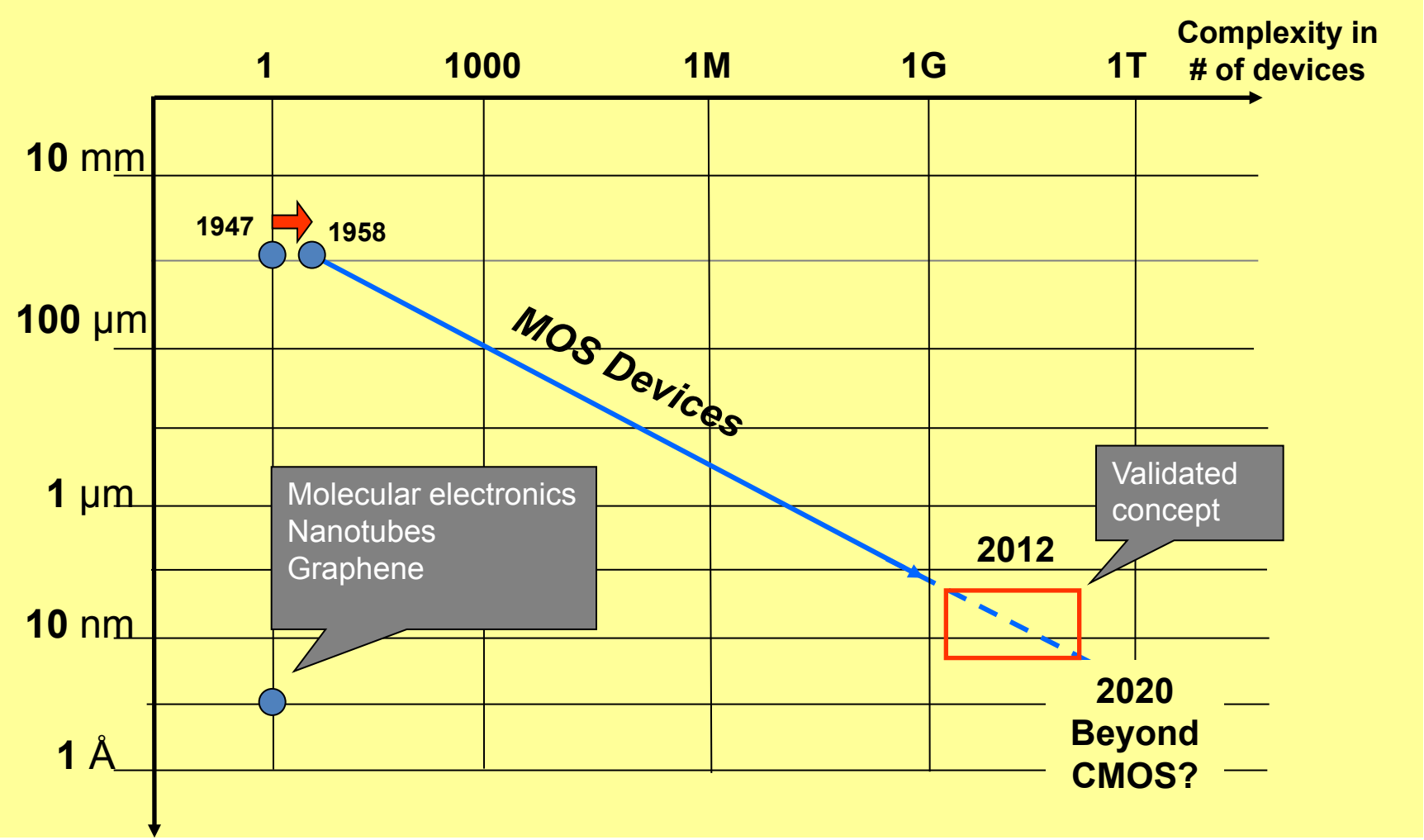
Issues associated to M.E.

- Transistor behavior has been demonstrated at reasonable drain voltages but the drain current levels are still small, due to the low conductance per molecule, leading to requirement of relatively large devices.
- Simple logic gates have also been demonstrated with reasonable gain and low switching energy but performance are very low when compared to silicon MOSFET.
- In a SAMFET, where the SAMs form the channel of the FET, true saturation appears difficult to reach.
- Electrodes define true dimensions
- The stability at room temperature remains very poor.

From S. Molen – SWOT analysis - Workshop Nano-Tec May 30-31, 2012Lausanne

Open Issues

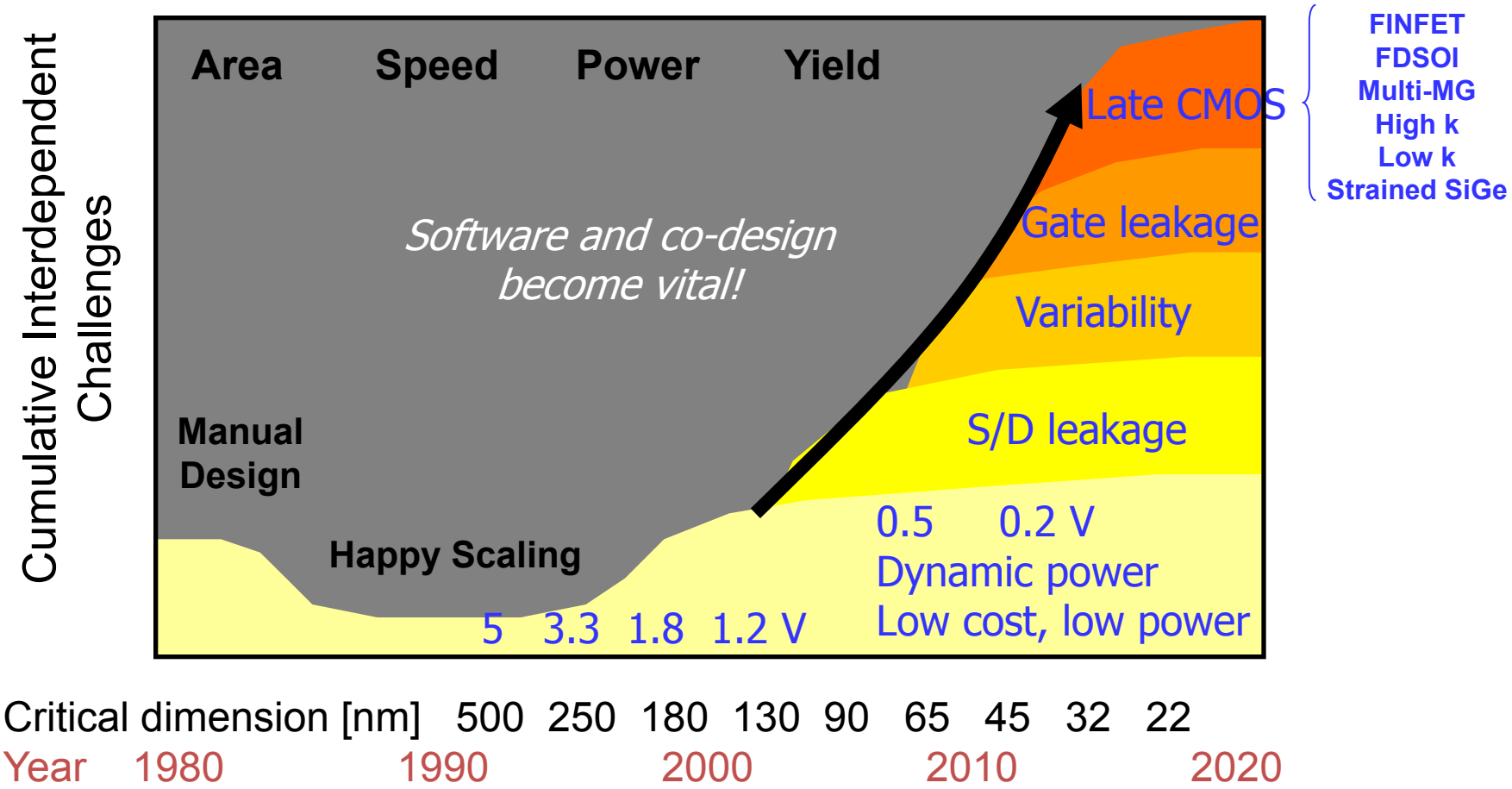
Reaching dimension/complexity limits



Source: STMicroelectronics

Design factors

More Moore: Increasing complexity



Design factors

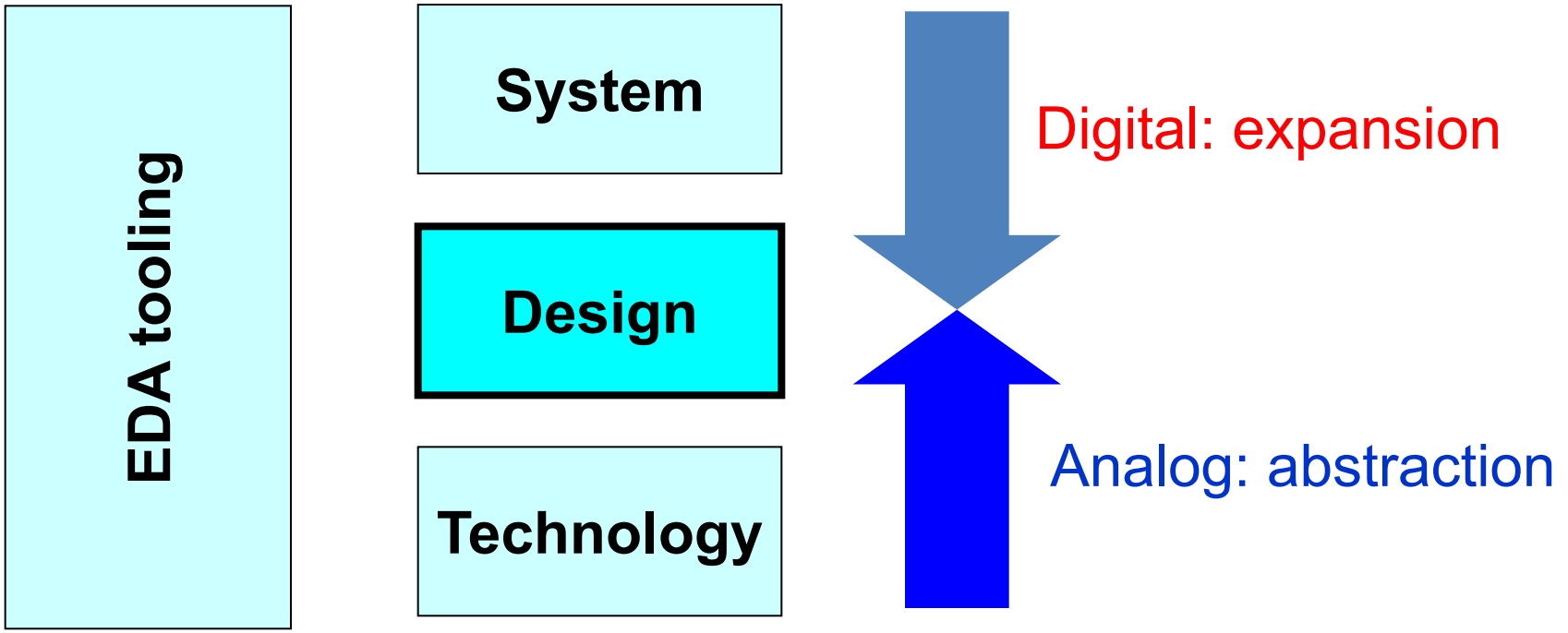
Challenges in design:

Design technologies that enable equivalent scaling (high performance, low power, high reliability, low cost, high design productivity)

- Design for variability
- Low power design (sleep modes, hibernation, clock gating, multi-VDD,...)
- Homogeneous and heterogeneous multicore SoC architectures

Design factors

Design Hierarchy



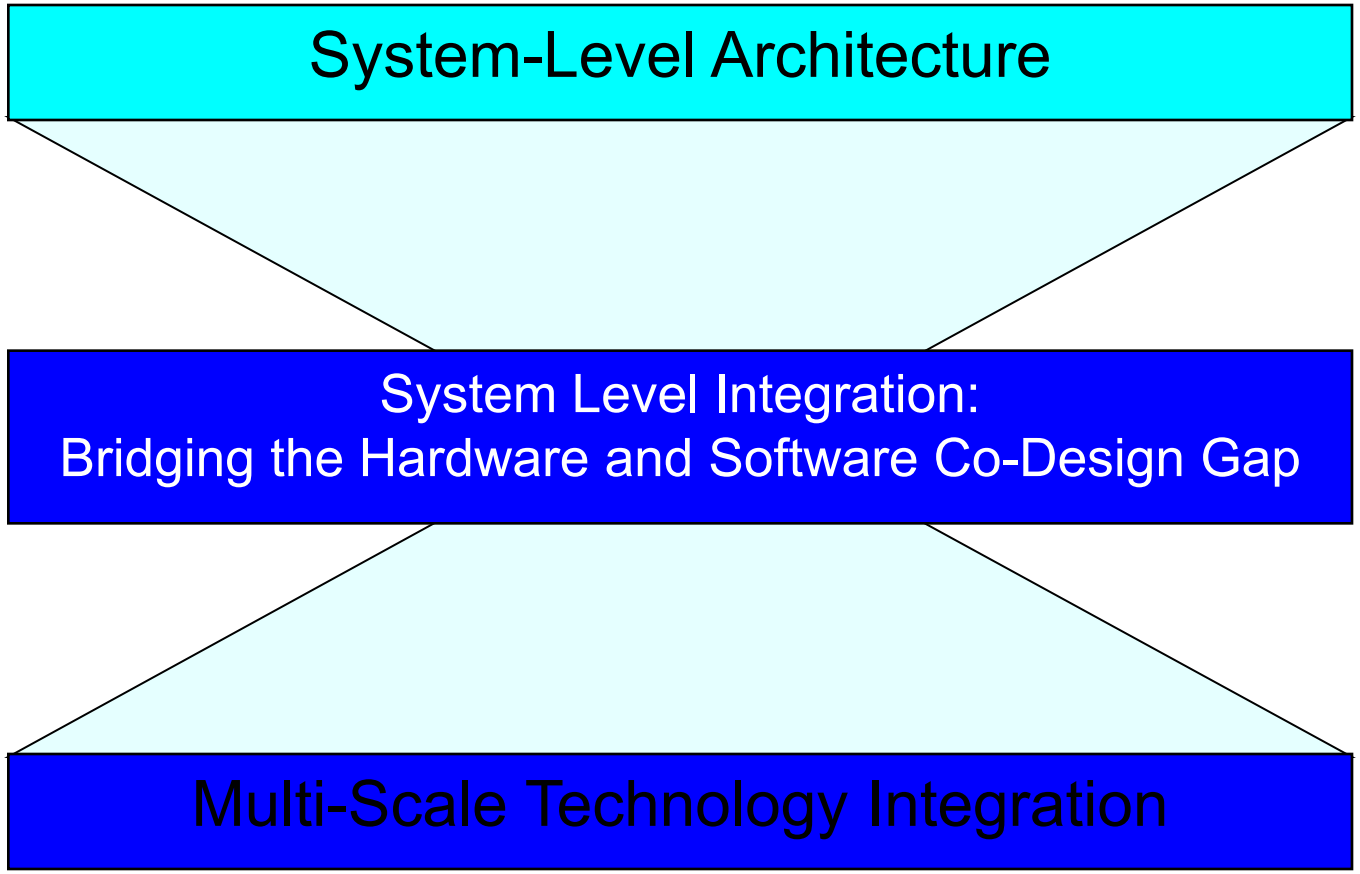
Analog and digital approach design from opposite directions

Mixed-signal: need to “meet in the middle”

Source: Maarten Vertregt, NXP

Design factors

The Co-Design Challenge



Open Issues

Nanowires

- Physics of nanowires: nanostructures, interfaces
- Process technology aspects: bottom-up vs. top-down
- Modeling & simulation tools

Graphene

- Manufacturability of quality material
- Variability of materials and devices
- Long term stability

Molecular electronics

- Low stability at room temperature
- Low conductance at room temperature
- Low performance compared to Si MOSFET

Recommendations

Nanowires, graphene, molecular electronics
Pursue programs on:

- Dense circuit integration aspects
- Physical aspects:
  - Electronic structure
  - Carrier transport
  - Variability control
  - Power efficiency
- CMOS compatibility
- Design aspects

- Industrial-academic cooperation